



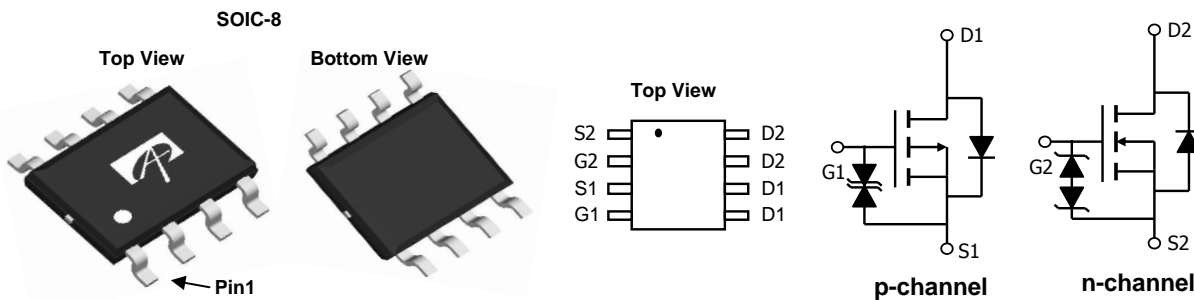
General Description

The AO4613 uses advanced trench technology MOSFETs to provide excellent $R_{DS(ON)}$ and low gate charge. The complementary MOSFETs may be used to form a level shifted high side switch, and for a host of other applications.

Product Summary

N-Channel	P-Channel
V_{DS} (V) = 30V	-30V
$I_D = 7.2A$ ($V_{GS}=10V$)	-6.1A ($V_{GS}=10V$)
$R_{DS(ON)}$ < 24m Ω ($V_{GS}=10V$)	$R_{DS(ON)}$ < 37m Ω ($V_{GS} = -10V$)
< 40m Ω ($V_{GS}=4.5V$)	< 60m Ω ($V_{GS} = -4.5V$)

ESD Protected
100% UIS Tested
100% Rg Tested



Absolute Maximum Ratings $T_A=25^\circ C$ unless otherwise noted

Parameter	Symbol	Max n-channel	Max p-channel	Units	
Drain-Source Voltage	V_{DS}	30	-30	V	
Gate-Source Voltage	V_{GS}	± 20	± 20	V	
Continuous Drain Current ^A	I_D	$T_A=25^\circ C$	7.2	-6.1	A
		$T_A=70^\circ C$	6.1	-5.1	
Pulsed Drain Current ^B	I_{DM}	30	-30		
Power Dissipation	P_D	$T_A=25^\circ C$	2	2	W
		$T_A=70^\circ C$	1.44	1.44	
Avalanche Current ^B	I_{AR}	15	20	A	
Repetitive avalanche energy 0.1mH ^B	E_{AR}	11	20	mJ	
Junction and Storage Temperature Range	T_J, T_{STG}	-55 to 150	-55 to 150	$^\circ C$	

Thermal Characteristics: n-channel and p-channel

Parameter	Symbol	Typ	Max		Units	
			n-ch	p-ch		
Maximum Junction-to-Ambient ^A	$R_{\theta JA}$	Steady-State	n-ch	55	62.5	$^\circ C/W$
Maximum Junction-to-Ambient ^A			p-ch	48	62.5	$^\circ C/W$
Maximum Junction-to-Lead ^C	$R_{\theta JL}$	Steady-State	n-ch	37	50	$^\circ C/W$
Maximum Junction-to-Ambient ^A			p-ch	84	110	$^\circ C/W$
Maximum Junction-to-Lead ^C	$R_{\theta JL}$	Steady-State	p-ch	37	50	$^\circ C/W$

N-Channel Electrical Characteristics ($T_J=25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
BV_{DSS}	Drain-Source Breakdown Voltage	$I_D=250\mu\text{A}$, $V_{GS}=0\text{V}$	30			V
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS}=24\text{V}$, $V_{GS}=0\text{V}$ $T_J=55^\circ\text{C}$			1 5	μA
I_{GSS}	Gate-Body leakage current	$V_{DS}=0\text{V}$, $V_{GS}=\pm 12\text{V}$			10	μA
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS}=V_{GS}$, $I_D=250\mu\text{A}$	1	2	3	V
$I_{D(ON)}$	On state drain current	$V_{GS}=10\text{V}$, $V_{DS}=5\text{V}$	20			A
$R_{DS(ON)}$	Static Drain-Source On-Resistance	$V_{GS}=10\text{V}$, $I_D=7.2\text{A}$ $T_J=125^\circ\text{C}$		20 29	24 35	$\text{m}\Omega$
		$V_{GS}=4.5\text{V}$, $I_D=4\text{A}$		30	40	$\text{m}\Omega$
g_{FS}	Forward Transconductance	$V_{DS}=5\text{V}$, $I_D=7.2\text{A}$	10	18		S
V_{SD}	Diode Forward Voltage	$I_S=1\text{A}$		0.77	1	V
I_S	Maximum Body-Diode Continuous Current				3	A
DYNAMIC PARAMETERS						
C_{iss}	Input Capacitance	$V_{GS}=0\text{V}$, $V_{DS}=15\text{V}$, $f=1\text{MHz}$		522	630	pF
C_{oss}	Output Capacitance			110		pF
C_{rss}	Reverse Transfer Capacitance			75		pF
R_g	Gate resistance	$V_{GS}=0\text{V}$, $V_{DS}=0\text{V}$, $f=1\text{MHz}$		2.1	3	Ω
SWITCHING PARAMETERS						
$Q_g(10\text{V})$	Total Gate Charge	$V_{GS}=10\text{V}$, $V_{DS}=15\text{V}$, $I_D=7.2\text{A}$		11	15	nC
$Q_g(4.5\text{V})$	Total Gate Charge			5.3	7	nC
Q_{gs}	Gate Source Charge			1.9		nC
Q_{gd}	Gate Drain Charge			4		nC
$t_{D(on)}$	Turn-On DelayTime	$V_{GS}=10\text{V}$, $V_{DS}=15\text{V}$, $R_L=2.1\Omega$, $R_{GEN}=3\Omega$		4.7	7	ns
t_r	Turn-On Rise Time			4.9	10	ns
$t_{D(off)}$	Turn-Off DelayTime			16.2	22	ns
t_f	Turn-Off Fall Time			3.5	7	ns
t_{rr}	Body Diode Reverse Recovery Time	$I_F=7.2\text{A}$, $di/dt=100\text{A}/\mu\text{s}$		15.7	20	ns
Q_{rr}	Body Diode Reverse Recovery Charge	$I_F=7.2\text{A}$, $di/dt=100\text{A}/\mu\text{s}$		7.9	10	nC

A: The value of $R_{\theta JA}$ is measured with the device mounted on 1in² FR-4 board with 2oz. Copper, in a still air environment with $T_A=25^\circ\text{C}$. The value in any given application depends on the user's specific board design. The current rating is based on the $t \leq 10\text{s}$ thermal resistance rating.

B: Repetitive rating, pulse width limited by junction temperature.

C: The $R_{\theta JA}$ is the sum of the thermal impedance from junction to lead $R_{\theta JL}$ and lead to ambient. $R_{\theta JL}$ and $R_{\theta JC}$ are equivalent terms referring to thermal resistance from junction to drain lead.

D: The static characteristics in Figures 1 to 6 are obtained using 80 μs pulses, duty cycle 0.5% max.

E: These tests are performed with the device mounted on 1 in² FR-4 board with 2oz. Copper, in a still air environment with $T_A=25^\circ\text{C}$. The SOA curve provides a single pulse rating.

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P-Channel Electrical Characteristics (T_J=25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
BV _{DSS}	Drain-Source Breakdown Voltage	I _D =-250μA, V _{GS} =0V	-30			V
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} =-24V, V _{GS} =0V T _J =55°C			-1 -5	μA
I _{GSS}	Gate-Body leakage current	V _{DS} =0V, V _{GS} =±12V			10	μA
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D =-250μA	-1	-1.7	-3	V
I _{D(ON)}	On state drain current	V _{GS} =-10V, V _{DS} =-5V	30			A
R _{DS(ON)}	Static Drain-Source On-Resistance	V _{GS} =-10V, I _D =-6.1A T _J =125°C		28 39	37 48	mΩ
		V _{GS} =-4.5V, I _D =-4A		45	60	
g _{FS}	Forward Transconductance	V _{DS} =-5V, I _D =-6.1A		12.5		S
V _{SD}	Diode Forward Voltage	I _S =-1A, V _{GS} =0V		-0.77	-1	V
I _S	Maximum Body-Diode Continuous Current				3	A
DYNAMIC PARAMETERS						
C _{ISS}	Input Capacitance	V _{GS} =0V, V _{DS} =-15V, f=1MHz		1040	1250	pF
C _{OSS}	Output Capacitance			179		pF
C _{rss}	Reverse Transfer Capacitance			134		pF
R _g	Gate resistance	V _{GS} =0V, V _{DS} =0V, f=1MHz		5	10	Ω
SWITCHING PARAMETERS						
Q _{g(10V)}	Total Gate Charge (10V)	V _{GS} =-10V, V _{DS} =-15V, I _D =-6.1A		16.8	22	nC
Q _{g(4.5V)}	Total Gate Charge (4.5V)			8.7	12	nC
Q _{gs}	Gate Source Charge			3.4		nC
Q _{gd}	Gate Drain Charge			5		nC
t _{D(on)}	Turn-On DelayTime	V _{GS} =-10V, V _{DS} =-15V, R _L =2.5Ω, R _{GEN} =3Ω		9	12	ns
t _r	Turn-On Rise Time			5.7	11	ns
t _{D(off)}	Turn-Off DelayTime			22.7	30	ns
t _f	Turn-Off Fall Time			10.2	20	ns
t _{rr}	Body Diode Reverse Recovery Time	I _F =-6.1A, di/dt=100A/μs		21.7	27	ns
Q _{rr}	Body Diode Reverse Recovery Charge	I _F =-6.1A, di/dt=100A/μs		13.6	18	nC

A: The value of R_{θJA} is measured with the device mounted on 1in² FR-4 board with 2oz. Copper, in a still air environment with T_A=25°C. The value in any given application depends on the user's specific board design. The current rating is based on the t ≤ 10s thermal resistance rating.

B: Repetitive rating, pulse width limited by junction temperature.

C. The R_{θJA} is the sum of the thermal impedance from junction to lead R_{θJL} and lead to ambient. R_{θJL} and R_{θJC} are equivalent terms referring to thermal resistance from junction to drain lead.

D. The static characteristics in Figures 1 to 6,12,14 are obtained using 80 μs pulses, duty cycle 0.5% max.

E. These tests are performed with the device mounted on 1 in² FR-4 board with 2oz. Copper, in a still air environment with T_A=25°C. The SOA curve provides a single pulse rating.

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N-CH TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

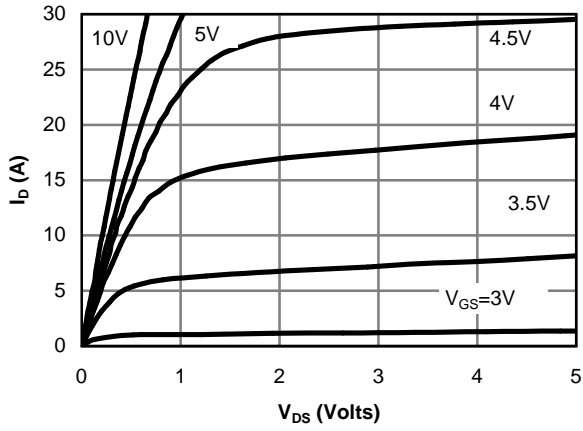


Fig 1: On-Region Characteristics

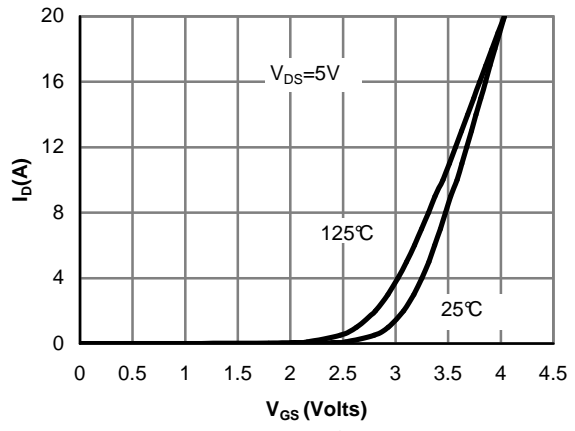


Figure 2: Transfer Characteristics

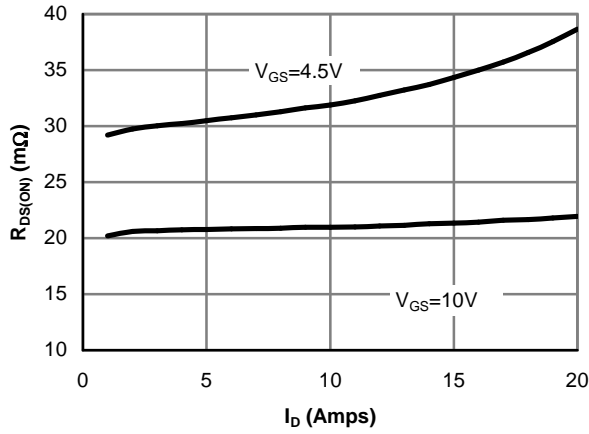


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

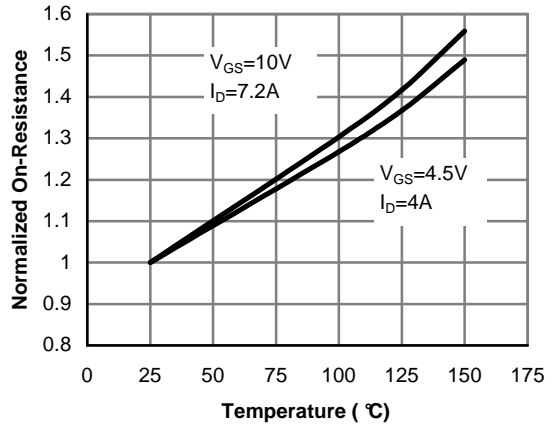


Figure 4: On-Resistance vs. Junction Temperature

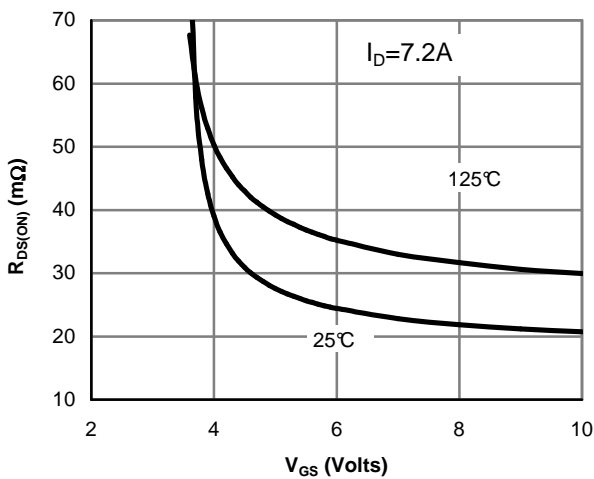


Figure 5: On-Resistance vs. Gate-Source Voltage

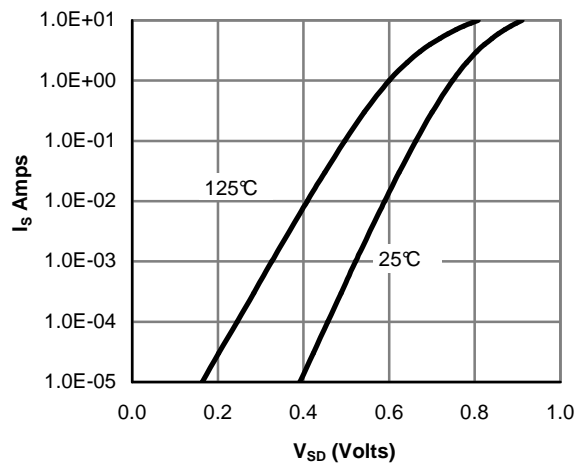


Figure 6: Body diode characteristics

N-CH TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

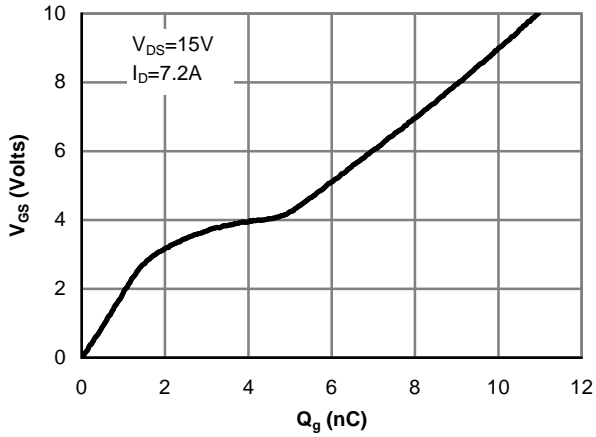


Figure 7: Gate-Charge characteristics

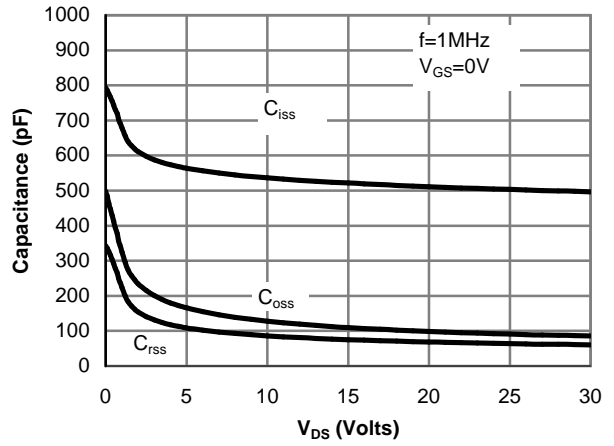


Figure 8: Capacitance Characteristics

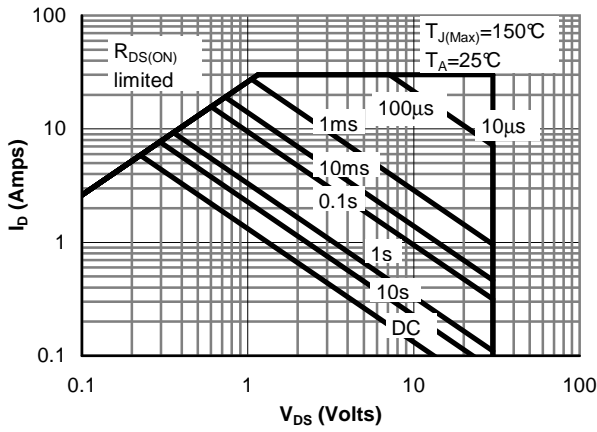


Figure 9: Maximum Forward Biased Safe Operating Area (Note E)

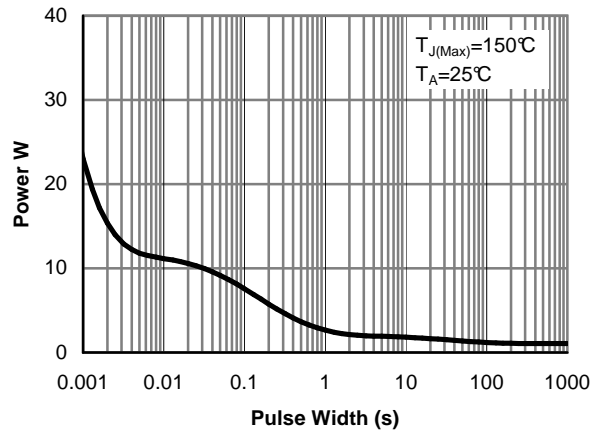


Figure 10: Single Pulse Power Rating Junction-to-Ambient (Note E)

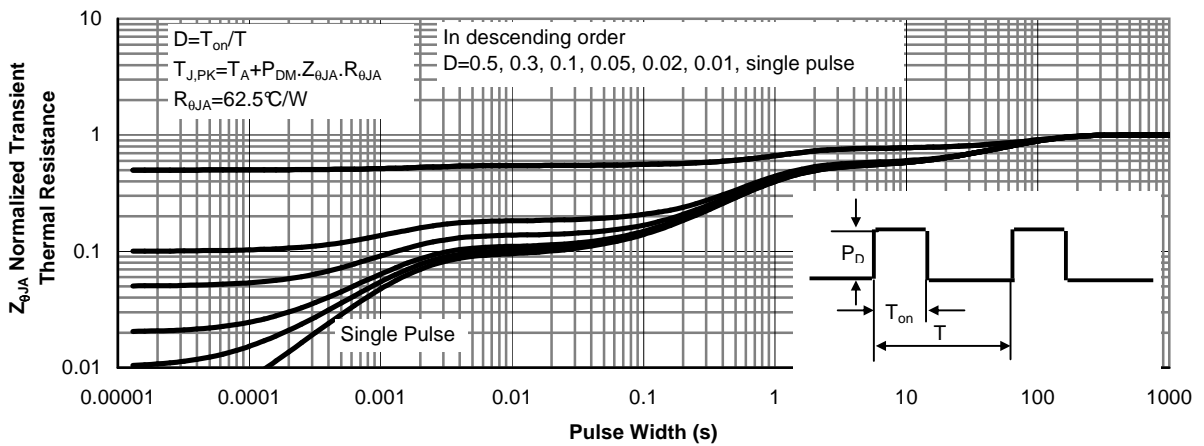


Figure 11: Normalized Maximum Transient Thermal Impedance

P-CH TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

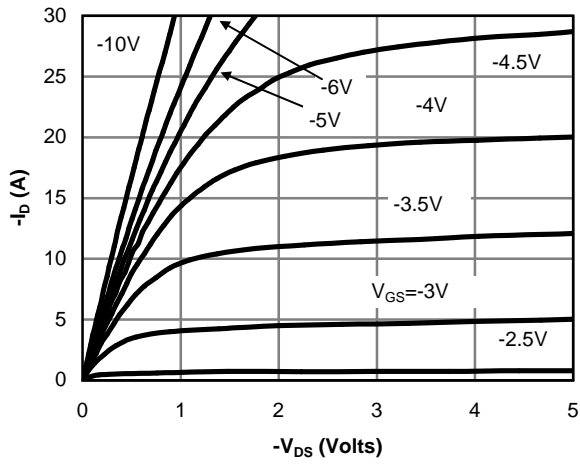


Fig 1: On-Region Characteristics

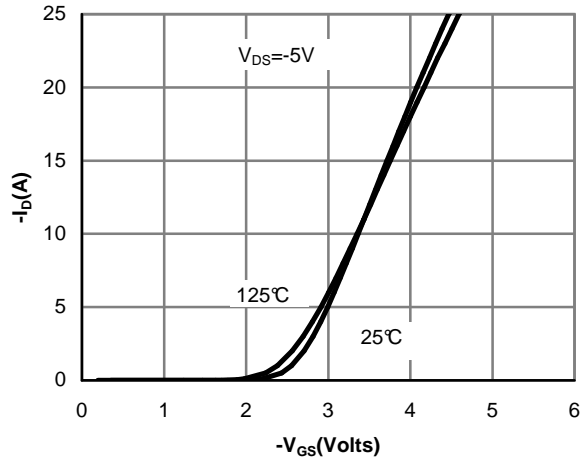


Figure 2: Transfer Characteristics

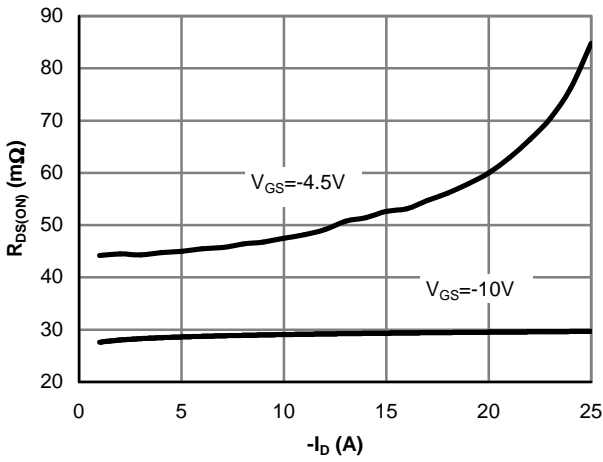


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

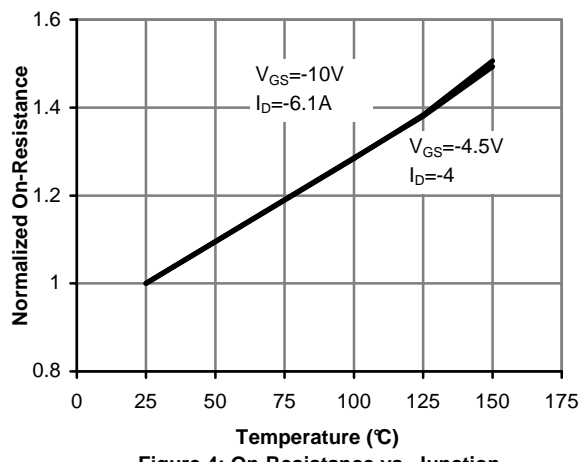


Figure 4: On-Resistance vs. Junction Temperature

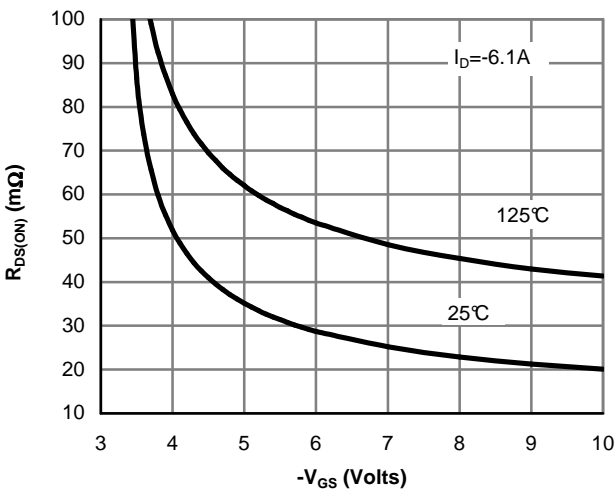


Figure 5: On-Resistance vs. Gate-Source Voltage

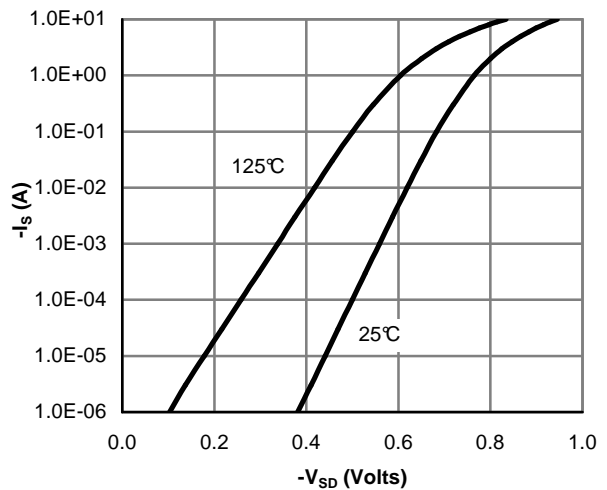


Figure 6: Body-Diode Characteristics

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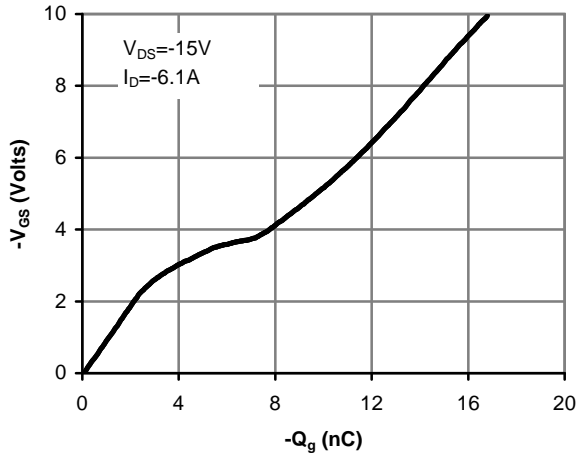


Figure 7: Gate-Charge Characteristics

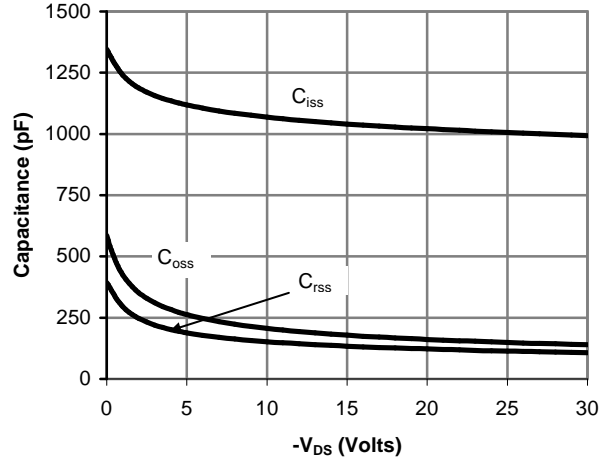


Figure 8: Capacitance Characteristics

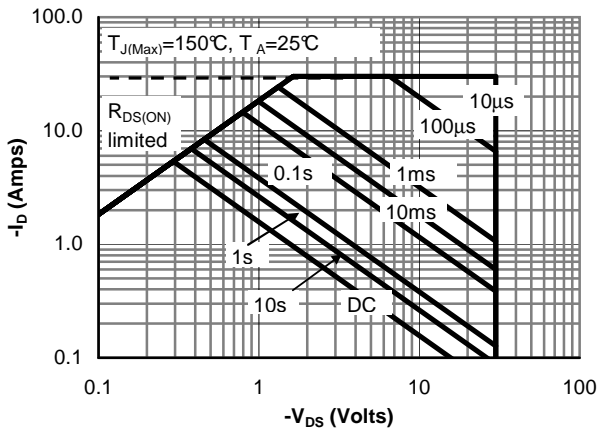


Figure 9: Maximum Forward Biased Safe Operating Area (Note E)

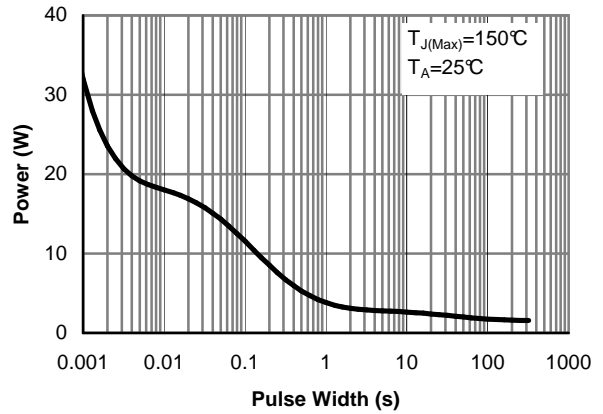


Figure 10: Single Pulse Power Rating Junction-to-Ambient (Note E)

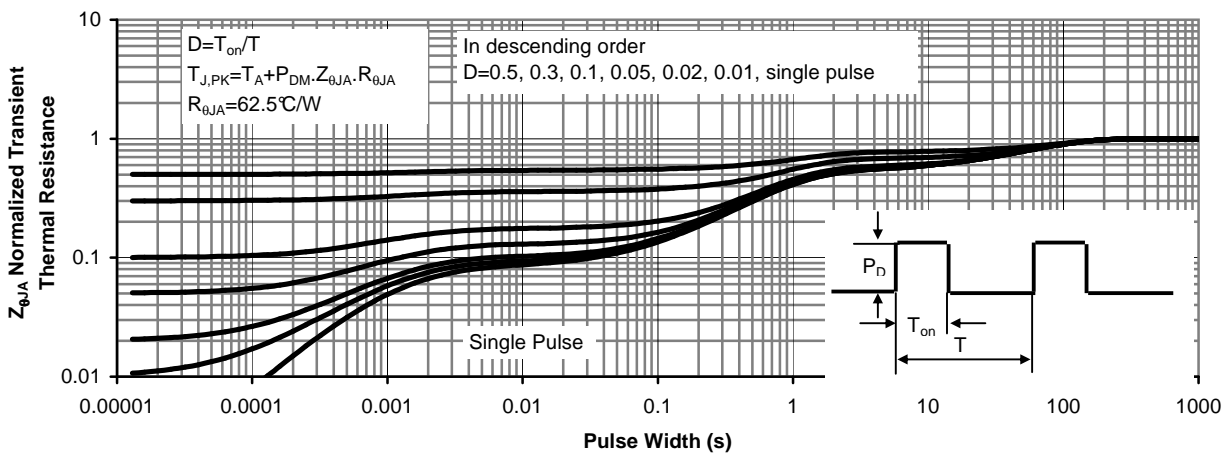


Figure 11: Normalized Maximum Transient Thermal Impedance