HIGH POWER SP4T SWITCH GaAs MMIC

■ GENERAL DESCRIPTION

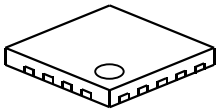
The NJG1809ME7 is a high power SP4T switch MMIC suitable for LTE-U / LAA, WLAN, and LTE applications.

This switch features very low insertion loss and high isolation up to 6GHz and excellent linearity performance with 1.8V control voltage. This switch achieves high speed switching time for WLAN application.

Integrated ESD protection device on each port achieves excellent ESD robustness. No DC Blocking capacitors are required for all RF ports unless DC is biased externally.

The small and thin EQFN18-E7 package is adopted.

■ PACKAGE OUTLINE



NJG1809ME7

■ APPLICATIONS

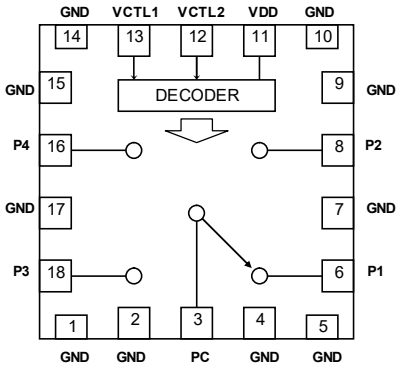
LTE-U / LAA, WLAN (802.11a/b/g/n/ac), LTE multi-mode applications
General purpose switching applications

■ FEATURES

● Low voltage logic control	1.35 to 5.0V
● Low insertion loss	0.40dB typ. @f=2.7GHz, 3.5GHz, P_{IN}=+27dBm
	0.50dB typ. @f=5.85GHz, P_{IN}=+27dBm
● High isolation	27dB typ. @f=2.7GHz, P_{IN}=+27dBm
	25dB typ. @f=3.5GHz, P_{IN}=+27dBm
	30dB typ. @f= 5.85GHz, P_{IN}=+27dBm
● $P_{-0.1dB}$	+32dBm min.
● High speed switching time	250ns typ.
● Small and thin package	EQFN18-E7 (2.0x2.0x0.397mm typ.)
● RoHS compliant and Halogen Free, MSL1	

■ PIN CONFIGURATION

(TOP VIEW)



Pin connection

1. GND	10. GND
2. GND	11. VDD
3. PC	12. VCTL2
4. GND	13. VCTL1
5. GND	14. GND
6. P1	15. GND
7. GND	16. P4
8. P2	17. GND
9. GND	18. P3

Exposed PAD: GND

■ TRUTH TABLE

"H"=$V_{CTL(H)}$, "L"=$V_{CTL(L)}$

VCTL1	VCTL2	Path
L	L	PC-P1
H	L	PC-P2
L	H	PC-P3
H	H	PC-P4

NOTE: Please note that any information on this datasheet will be subject to change.

■ ABSOLUTE MAXIMUM RATINGS

(T_a=+25°C, Z_s=Z_l=50Ω)

PARAMETER	SYMBOL	CONDITIONS	RATINGS	UNITS
RF Input Power	P_{IN}	V_{DD} =2.75V, V_{CTL}=0/1.8V	+33	dBm
Supply Voltage	V_{DD}	VDD terminal	5.0	V
Control Voltage	V_{CTL}	VCTL1, VCTL2 terminal	5.0	V
Power Dissipation	P_D	Four-layer FR4 PCB with through-hole (101.5x114.5mm), T_j=150°C	1400	mW
Operating Temp.	T_{opr}		-40 to +105	°C
Storage Temp.	T_{stg}		-55 to +150	°C

■ ELECTRICAL CHARACTERISTICS 1 (DC)

(General conditions: T_a=+25°C, V_{DD}=2.75V, $V_{CTL(H)}$=1.8V, $V_{CTL(L)}$=0V, with application circuit)

PARAMETERS	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage	V_{DD}	VDD Terminal	2.5	2.75	5.0	V
Operating Current	I_{DD}	No RF input	-	350	700	μA
Control Voltage (LOW)	$V_{CTL(L)}$	VCTL1, VCTL2 Terminal	0	-	0.45	V
Control Voltage (HIGH)	$V_{CTL(H)}$	VCTL1, VCTL2 Terminal	1.35	1.8	5.0	V
Control Current	I_{CTL}	$V_{CTL(H)}$=1.8V	-	4	10	μA

■ **ELECTRICAL CHARACTERISTICS 2 (RF)**

(General conditions: T_a=+25°C, Z_s=Z_l=50Ω, V_{DD}=2.75V, $V_{CTL(H)}$=1.8V, $V_{CTL(L)}$=0V, with application circuit)

PARAMETERS	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Insertion Loss 1	LOSS1	f=0.7GHz, P_{IN}=+27dBm		-	0.35	0.55	dB
Insertion Loss 2	LOSS2	f=2.0GHz, P_{IN}=+27dBm		-	0.40	0.60	dB
Insertion Loss 3	LOSS3	f=2.7GHz, P_{IN}=+27dBm		-	0.40	0.60	dB
Insertion Loss 4	LOSS4	f=3.5GHz, P_{IN}=+27dBm		-	0.40	0.60	dB
Insertion Loss 5	LOSS5	f=5.85GHz, P_{IN}=+27dBm		-	0.50	0.75	dB
Isolation 1	ISL1	f=0.7GHz, P_{IN}=+27dBm		32	36	-	dB
Isolation 2	ISL2	f=2.0GHz, P_{IN}=+27dBm		25	28	-	dB
Isolation 3	ISL3	f=2.7GHz, P_{IN}=+27dBm		24	27	-	dB
Isolation 4	ISL4	f=3.5GHz, P_{IN}=+27dBm		22	25	-	dB
Isolation 5	ISL5	f=5.85GHz, P_{IN}=+27dBm	PC-Pn*1	26	30	-	dB
			Pm-Pn*2	20	23	-	
Input Power at 0.1 dB Compression Point	$P_{-0.1dB}$	f=5.85GHz		+32	-	-	dBm
2nd Harmonics 1	2fo(1)	f=5.18GHz, 5.85GHz, P_{IN}=+27dBm		-	-	-70	dBc
2nd Harmonics 2	2fo(2)	f=2.69GHz, P_{IN}=0dBm		-	-	-95	dBc
3rd Harmonics 1	3fo(1)	f=5.18GHz, 5.85GHz, P_{IN}=+27dBm		-	-	-70	dBc
3rd Harmonics 2	3fo(2)	f=1.732GHz, 1.91GHz, P_{IN}=0dBm		-	-	-95	dBc
4th Harmonics	4fo	f=5.18GHz, 5.85GHz, P_{IN}=+27dBm		-	-	-70	dBc
Input 2nd order intercept point	IIP2	f=2.48+2.69GHz, f_{meas}=5.17GHz, P_{IN}=+10dBm each		+100	-	-	dBm
Input 3rd order intercept point	IIP3	f=1.71+2.40GHz, f_{meas}=5.82 GHz, P_{IN}=+10dBm each		+60	-	-	dBm
VSWR1	VSWR1	On-state ports, f=2.7GHz		-	1.2	1.5	-
VSWR2	VSWR2	On-state ports, f=5.85GHz		-	1.3	1.6	-
Switching time	T_{SW}	50% V_{CTL} to 10/90% RF		-	250	400	ns

*1: Pn=P1, P2, P3, P4

*2: Pm=P1, P2, P3, P4. Pn=P1, P2, P3, P4. m≠n

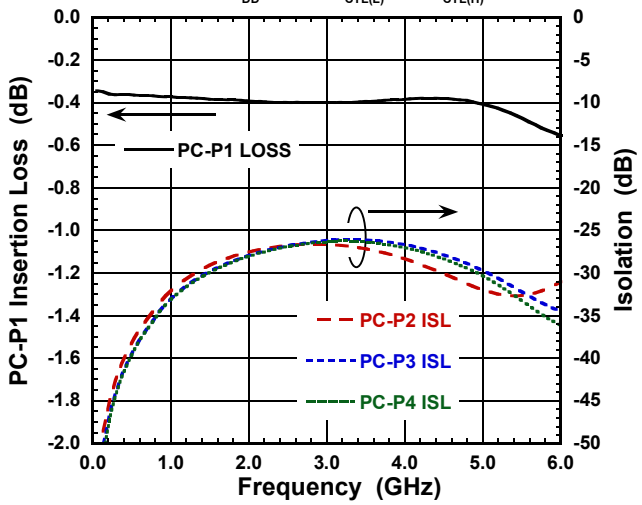
■ **TERMINAL INFORMATION**

No.	SYMBOL	DESCRIPTION
1	GND	Ground terminal. Please connect this terminal with ground plane as close as possible for excellent RF performance.
2	GND	Ground terminal. Please connect this terminal with ground plane as close as possible for excellent RF performance.
3	PC	Common RF terminal. No DC blocking capacitor is required for this port unless DC is biased externally.
4	GND	Ground terminal. Please connect this terminal with ground plane as close as possible for excellent RF performance.
5	GND	Ground terminal. Please connect this terminal with ground plane as close as possible for excellent RF performance.
6	P1	RF terminal. No DC blocking capacitor is required for this port unless DC is biased externally.
7	GND	Ground terminal. Please connect this terminal with ground plane as close as possible for excellent RF performance.
8	P2	RF terminal. No DC blocking capacitor is required for this port unless DC is biased externally.
9	GND	Ground terminal. Please connect this terminal with ground plane as close as possible for excellent RF performance.
10	GND	Ground terminal. Please connect this terminal with ground plane as close as possible for excellent RF performance.
11	VDD	Positive voltage supply terminal. The positive voltage (+2.5 to +5V) has to be supplied. Please connect a bypass capacitor with ground plane for excellent RF performance.
12	VCTL2	Control signal input terminal. This terminal is set to High-Level (+1.35 to +5.0V) or Low-Level (0 to +0.45V).
13	VCTL1	Control signal input terminal. This terminal is set to High-Level (+1.35 to +5.0V) or Low-Level (0 to +0.45V).
14	GND	Ground terminal. Please connect this terminal with ground plane as close as possible for excellent RF performance.
15	GND	Ground terminal. Please connect this terminal with ground plane as close as possible for excellent RF performance.
16	P4	RF terminal. No DC blocking capacitor is required for this port unless DC is biased externally.
17	GND	Ground terminal. Please connect this terminal with ground plane as close as possible for excellent RF performance.
18	P3	RF terminal. No DC blocking capacitor is required for this port unless DC is biased externally.
Exposed Pad	GND	Ground pad of IC bottom side. Please connect this pad with ground plane as close as possible for excellent RF performance.

■ **ELECTRICAL CHARACTERISTICS** (With application circuit, loss of external circuit are excluded.)

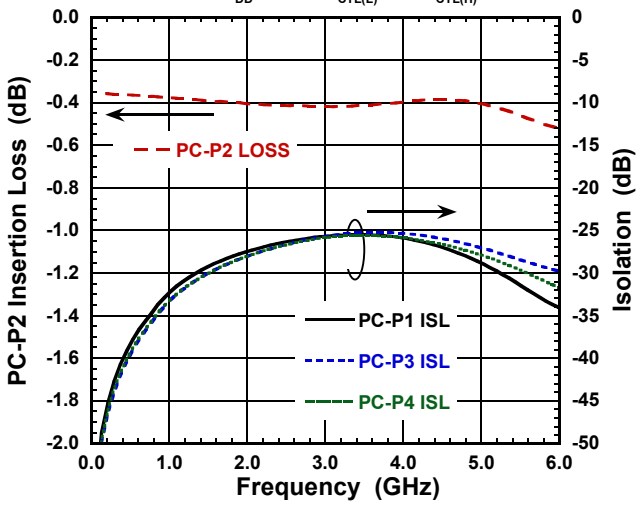
LOSS, ISL vs Frequency

(PC-P1 ON, V_{DD}=2.75V, $V_{CTL(L)}$=0V, $V_{CTL(H)}$=1.8V)



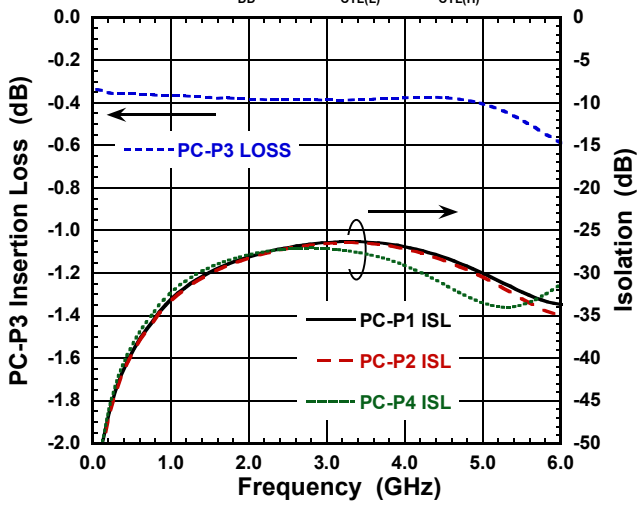
LOSS, ISL vs Frequency

(PC-P2 ON, V_{DD}=2.75V, $V_{CTL(L)}$=0V, $V_{CTL(H)}$=1.8V)



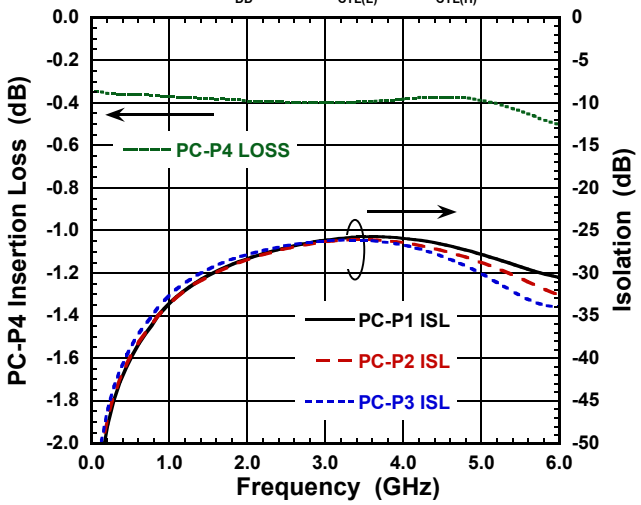
LOSS, ISL vs Frequency

(PC-P3 ON, V_{DD}=2.75V, $V_{CTL(L)}$=0V, $V_{CTL(H)}$=1.8V)



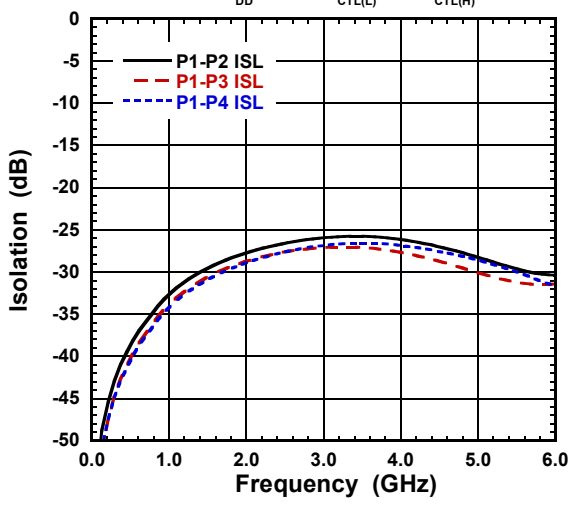
LOSS, ISL vs Frequency

(PC-P4 ON, V_{DD}=2.75V, $V_{CTL(L)}$=0V, $V_{CTL(H)}$=1.8V)



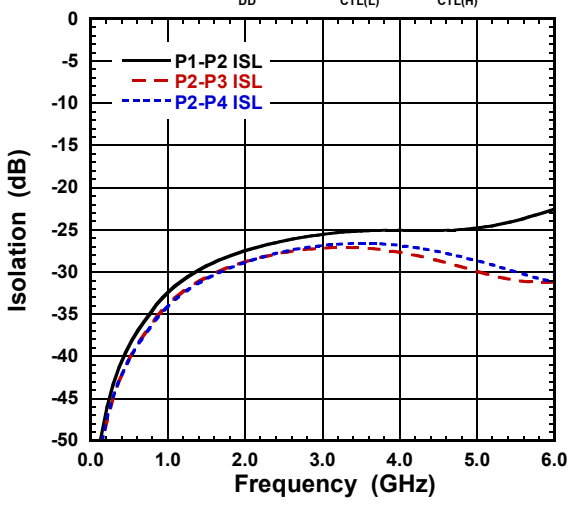
ISL vs Frequency

(PC-P1 ON, V_{DD}=2.75V, $V_{CTL(L)}$=0V, $V_{CTL(H)}$=1.8V)



ISL vs Frequency

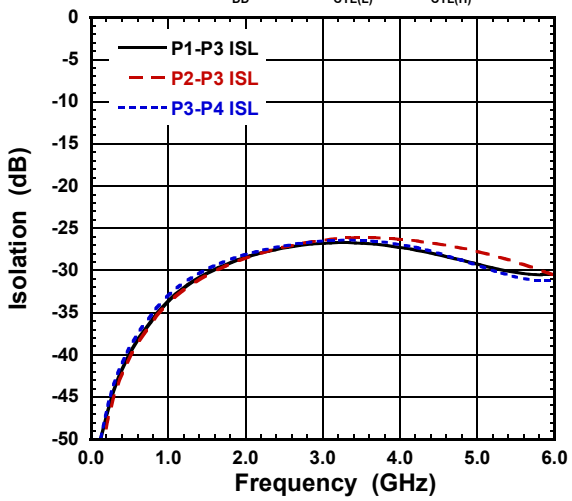
(PC-P2 ON, V_{DD}=2.75V, $V_{CTL(L)}$=0V, $V_{CTL(H)}$=1.8V)



■ **ELECTRICAL CHARACTERISTICS** (With application circuit, loss of external circuit are excluded.)

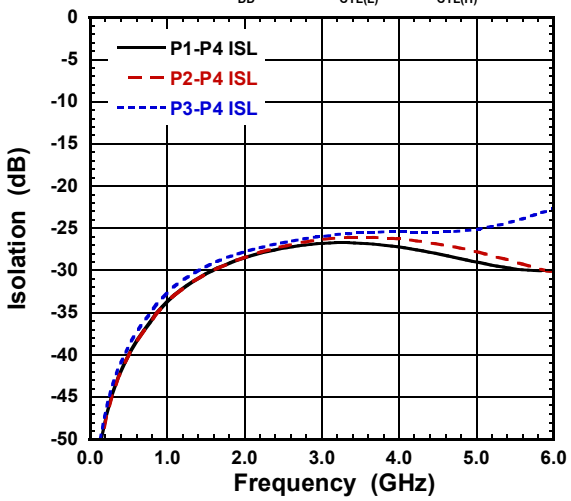
ISL vs Frequency

(PC-P3 ON, V_{DD}=2.75V, $V_{CTL(L)}$=0V, $V_{CTL(H)}$=1.8V)



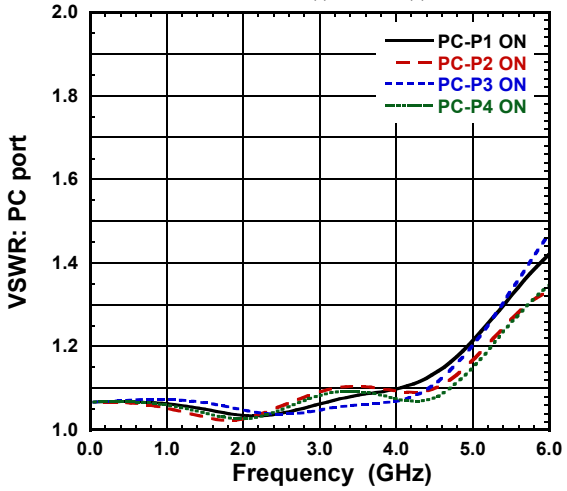
ISL vs Frequency

(PC-P4 ON, V_{DD}=2.75V, $V_{CTL(L)}$=0V, $V_{CTL(H)}$=1.8V)



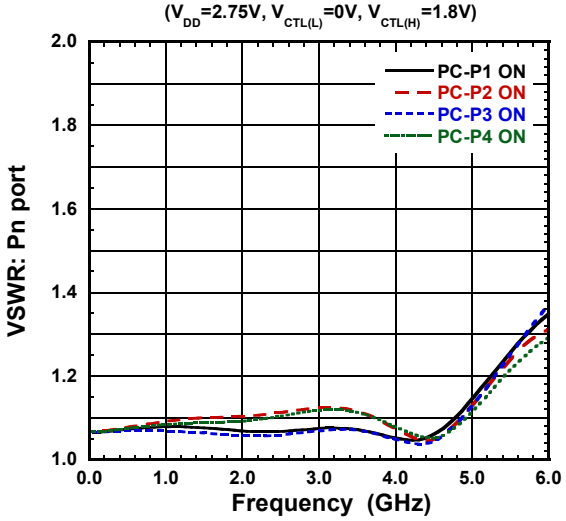
VSWR vs Frequency

(V_{DD}=2.75V, $V_{CTL(L)}$=0V, $V_{CTL(H)}$=1.8V)



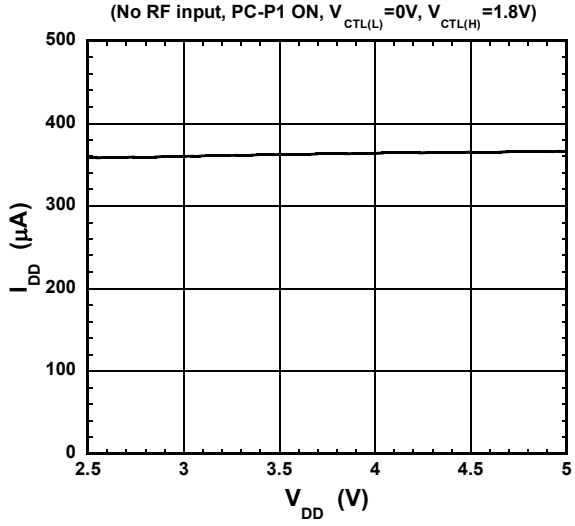
VSWR vs Frequency

(V_{DD}=2.75V, $V_{CTL(L)}$=0V, $V_{CTL(H)}$=1.8V)



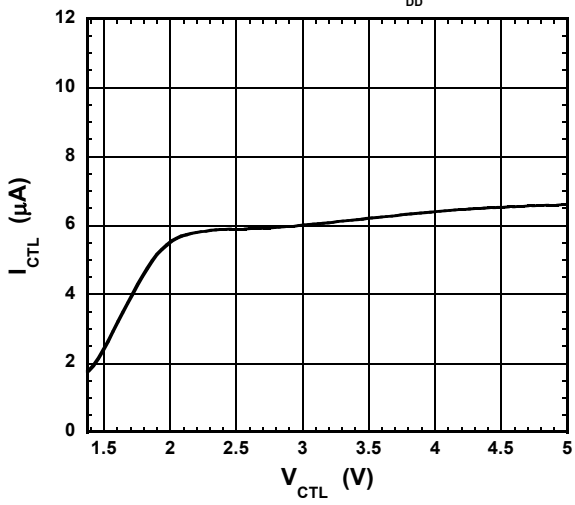
I_{DD} vs V_{DD}

(No RF input, PC-P1 ON, $V_{CTL(L)}$=0V, $V_{CTL(H)}$=1.8V)



I_{CTL} vs V_{CTL}

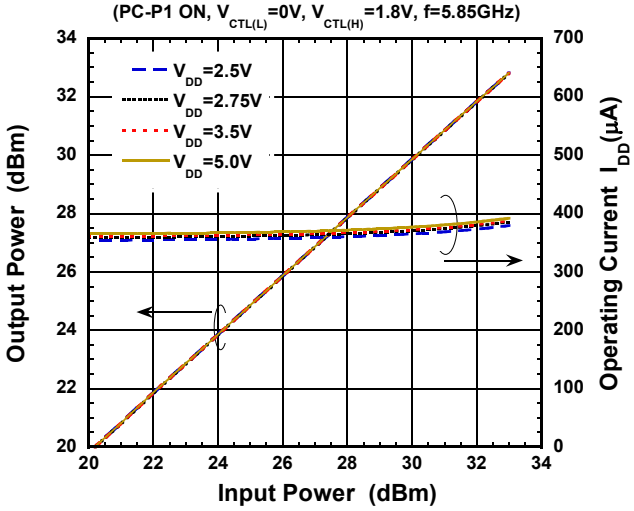
(No RF input, PC-P1 ON, V_{DD}=2.75V)



■ **ELECTRICAL CHARACTERISTICS** (With application circuit, loss of external circuit are excluded.)

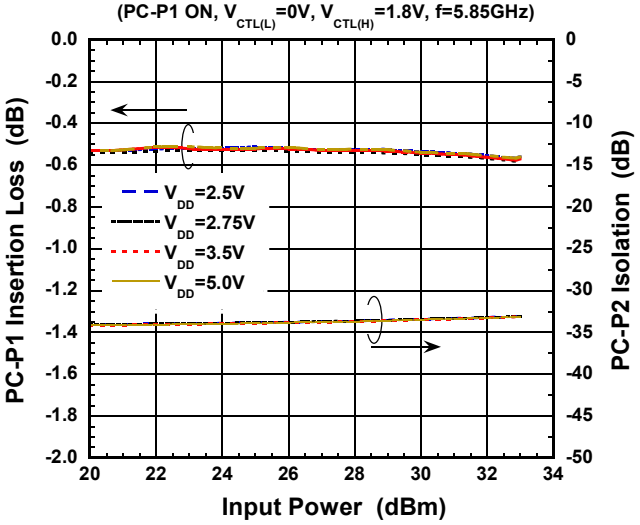
Output Power, I_{DD} vs Input Power

(PC-P1 ON, $V_{CTL(L)}$=0V, $V_{CTL(H)}$=1.8V, f=5.85GHz)



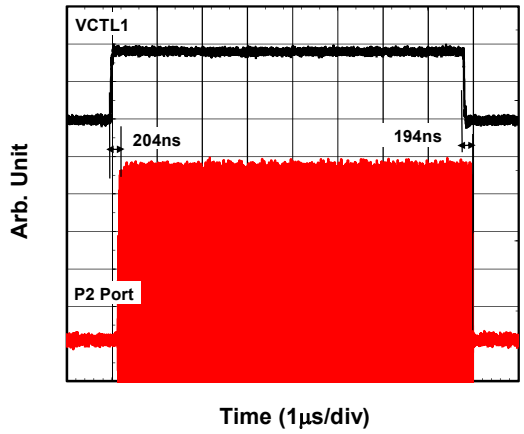
Loss, ISL vs Input Power

(PC-P1 ON, $V_{CTL(L)}$=0V, $V_{CTL(H)}$=1.8V, f=5.85GHz)



Switching Time

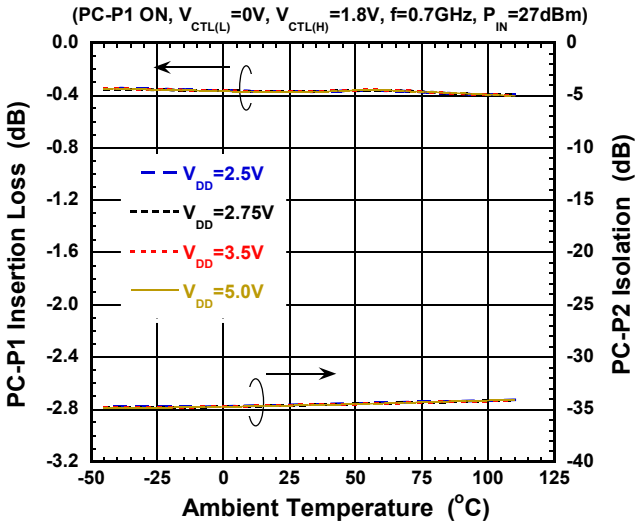
(PC-P1/P2 path, V_{DD}=2.75V, $V_{CTL(L)}$=0V, $V_{CTL(H)}$=1.8V)



■ **ELECTRICAL CHARACTERISTICS** (With application circuit, loss of external circuit are excluded.)

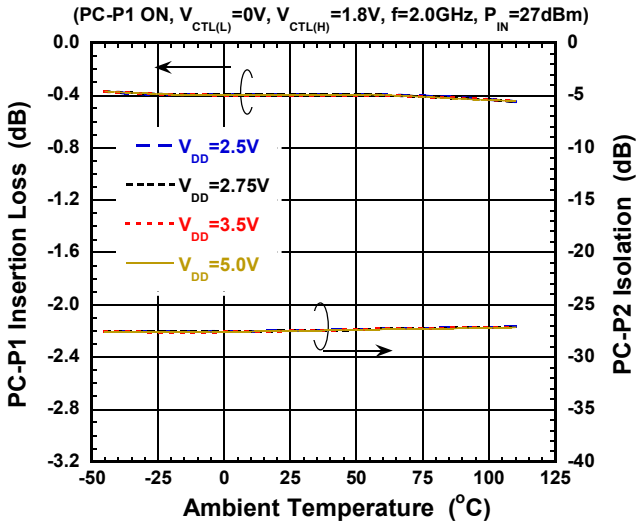
Loss, ISL vs Temperature

(PC-P1 ON, $V_{CTL(L)}$=0V, $V_{CTL(H)}$=1.8V, f=0.7GHz, P_{IN}=27dBm)



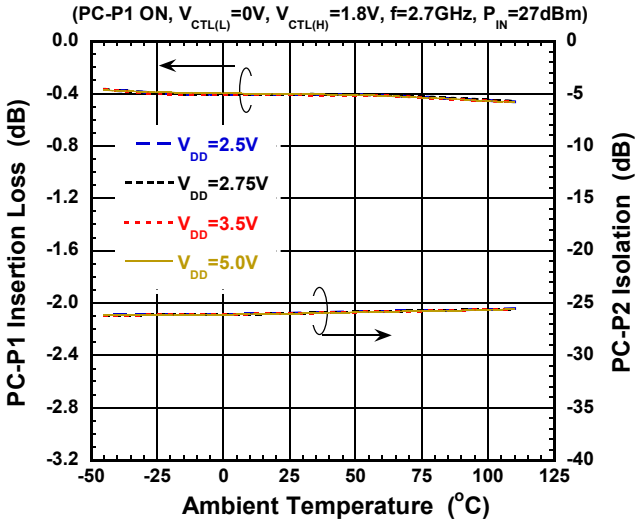
Loss, ISL vs Temperature

(PC-P1 ON, $V_{CTL(L)}$=0V, $V_{CTL(H)}$=1.8V, f=2.0GHz, P_{IN}=27dBm)



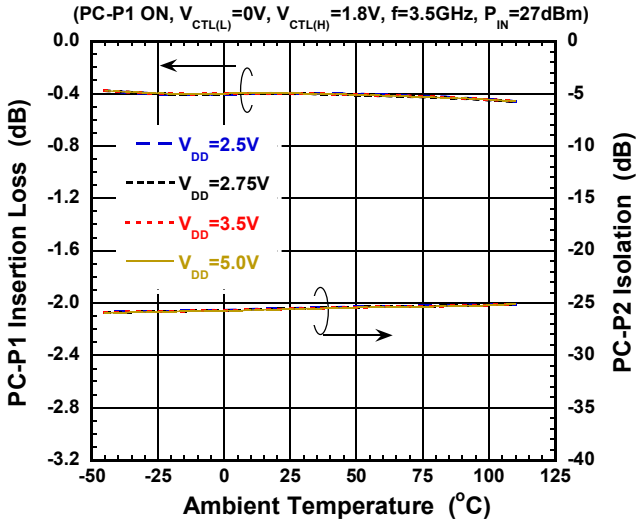
Loss, ISL vs Temperature

(PC-P1 ON, $V_{CTL(L)}$=0V, $V_{CTL(H)}$=1.8V, f=2.7GHz, P_{IN}=27dBm)



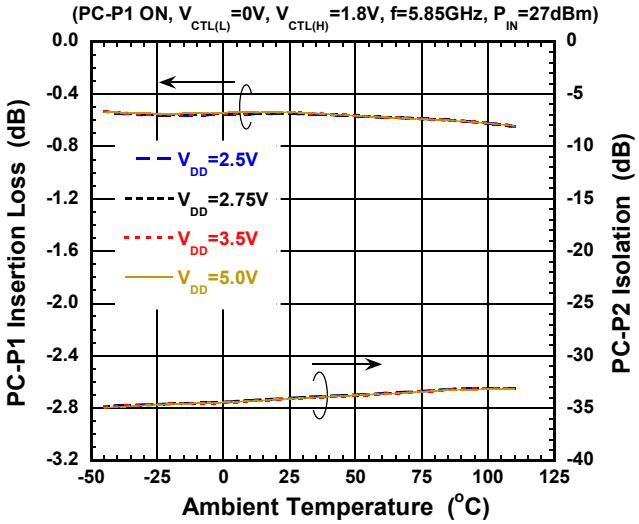
Loss, ISL vs Temperature

(PC-P1 ON, $V_{CTL(L)}$=0V, $V_{CTL(H)}$=1.8V, f=3.5GHz, P_{IN}=27dBm)



Loss, ISL vs Temperature

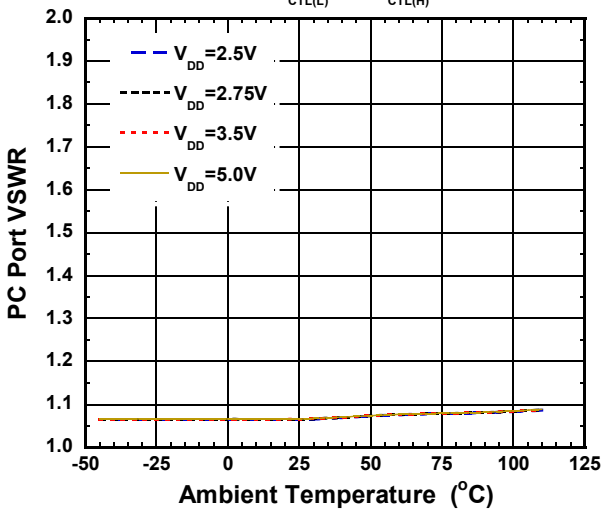
(PC-P1 ON, $V_{CTL(L)}$=0V, $V_{CTL(H)}$=1.8V, f=5.85GHz, P_{IN}=27dBm)



■ **ELECTRICAL CHARACTERISTICS** (With application circuit, loss of external circuit are excluded.)

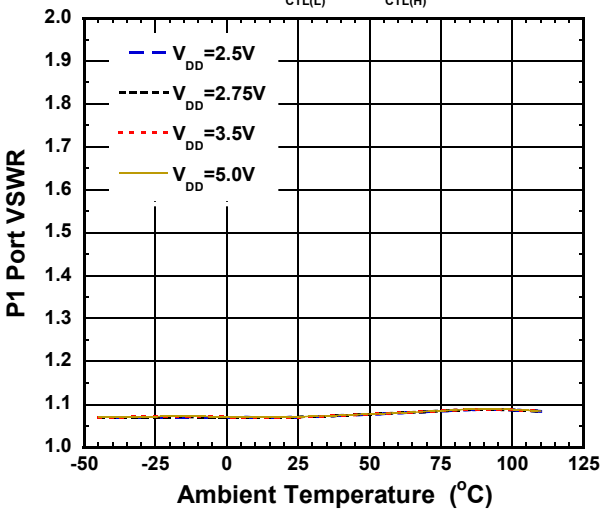
VSWR vs Temperature

(PC-P1 ON, PC Port, $V_{CTL(L)}$=0V, $V_{CTL(H)}$=1.8V, f=2.7GHz)



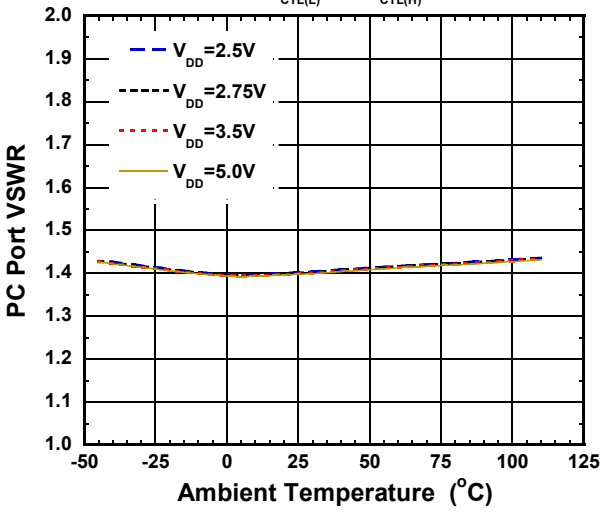
VSWR vs Temperature

(PC-P1 ON, P1 Port, $V_{CTL(L)}$=0V, $V_{CTL(H)}$=1.8V, f=2.7GHz)



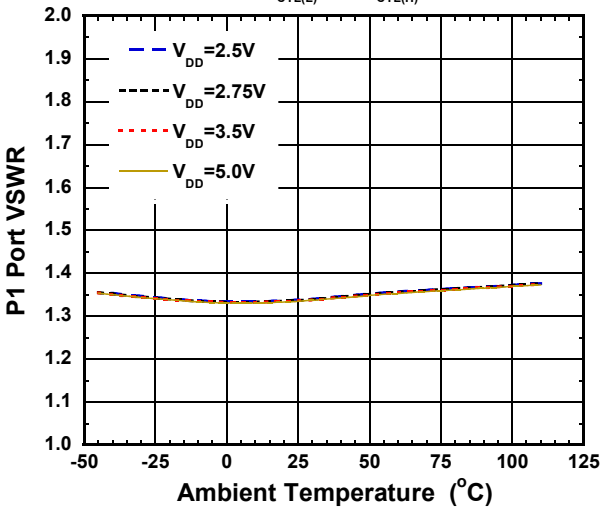
VSWR vs Temperature

(PC-P1 ON, PC Port, $V_{CTL(L)}$=0V, $V_{CTL(H)}$=1.8V, f=5.85GHz)



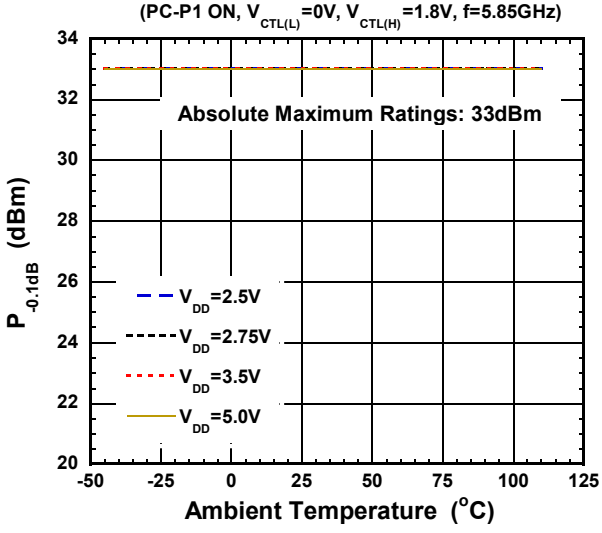
VSWR vs Temperature

(PC-P1 ON, P1 Port, $V_{CTL(L)}$=0V, $V_{CTL(H)}$=1.8V, f=5.85GHz)



$P_{-0.1dB}$ vs Temperature

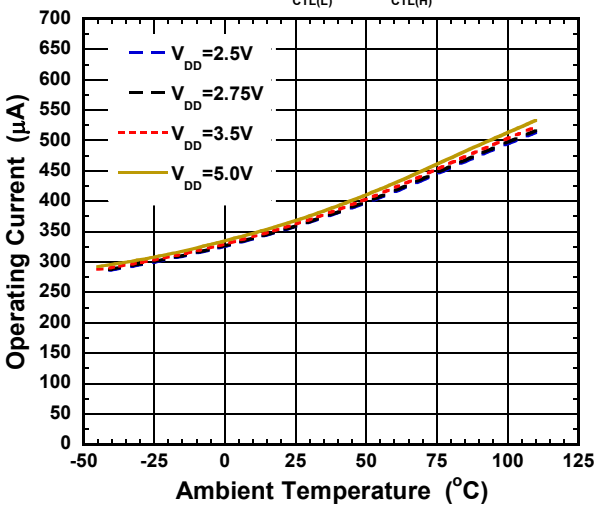
(PC-P1 ON, $V_{CTL(L)}$=0V, $V_{CTL(H)}$=1.8V, f=5.85GHz)



■ **ELECTRICAL CHARACTERISTICS** (With application circuit, loss of external circuit are excluded.)

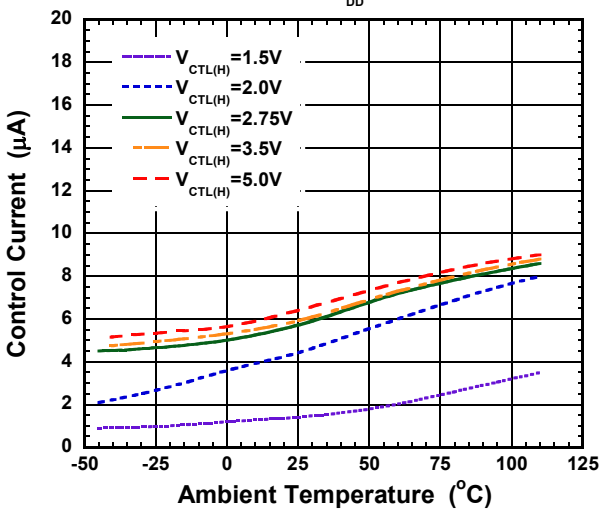
Operating Current vs Temperature

(PC-P1 ON, $V_{CTL(L)}$=0V, $V_{CTL(H)}$=1.8V)



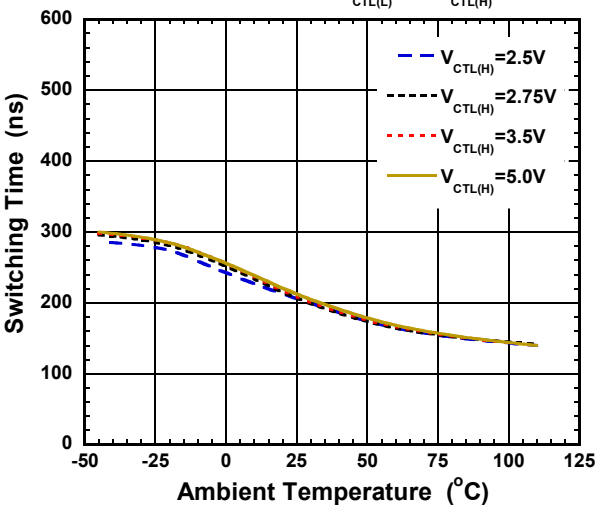
Control Current vs Temperature

(PC-P2 ON, V_{DD}=2.75V)



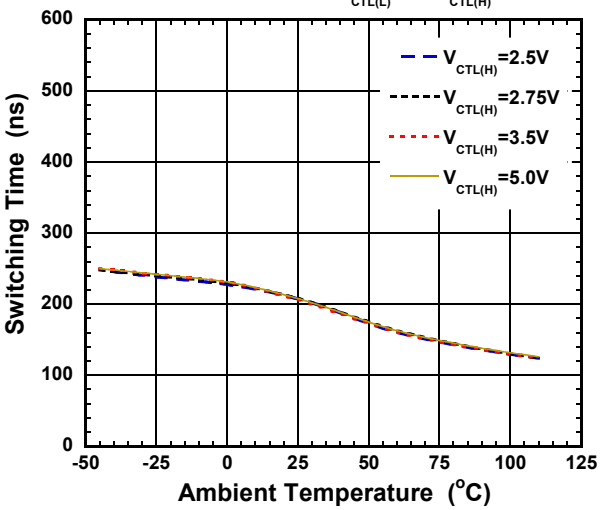
Switching Time(rise) vs Temperature

(PC-P1/P2 path, P2 port, $V_{CTL(L)}$=0V, $V_{CTL(H)}$=1.8V)



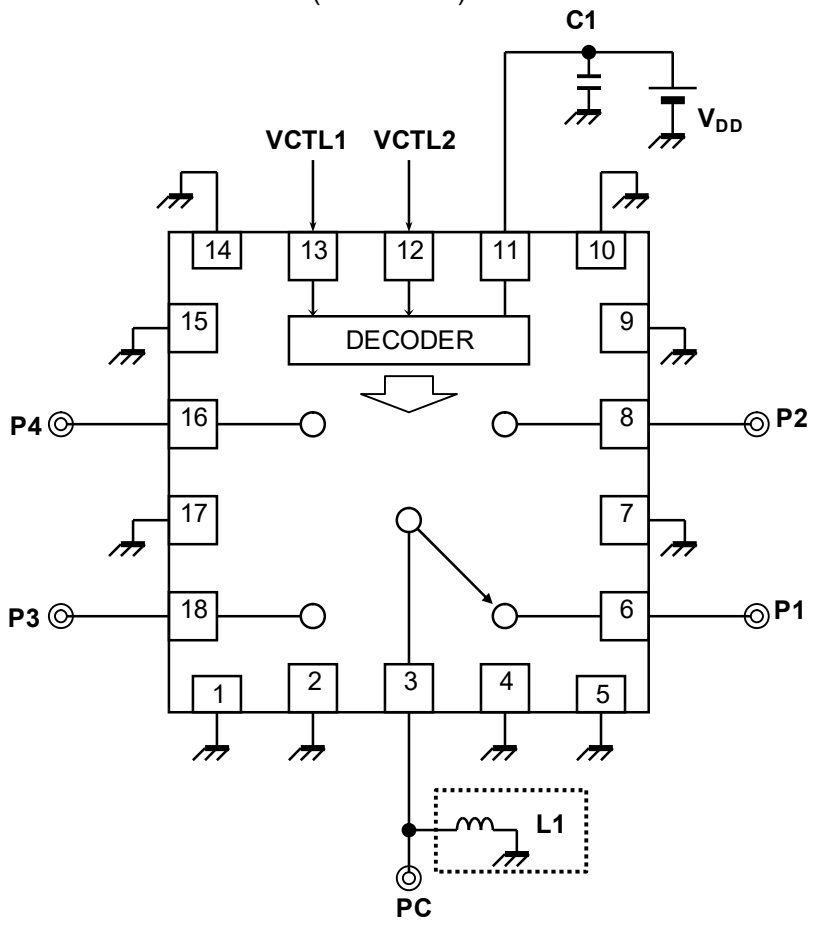
Switching Time(fall) vs Temperature

(PC-P1/P2 path, P2 port, $V_{CTL(L)}$=0V, $V_{CTL(H)}$=1.8V)



■ **APPLICATION CIRCUIT**

(TOP VIEW)



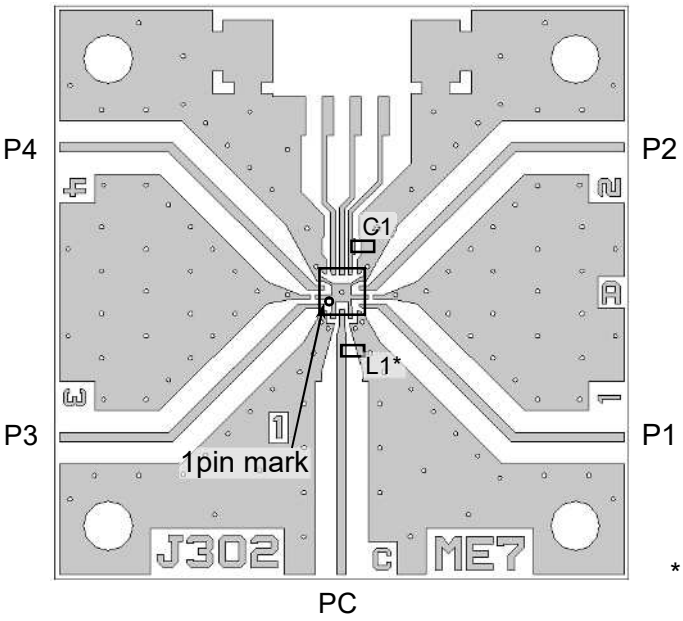
Note:
[1] No DC blocking capacitors are required on all RF ports, unless DC is biased externally.
[2] The inductor L1 is optional in order to achieve enhancing ESD protection level. L1 is also recommended in order to keep the DC bias level of each RF port at ground level tightly.

PARTS LIST

No.	Parameters	Note
C1	1000pF	MURATA (GRM15)
L1	68nH	TAIYO-YUDEN (HK1005)

■ PCB LAYOUT

(TOP VIEW)



PCB:	FR-4, t=0.2mm
Capacitor size:	1005
Strip line width:	0.4mm
PCB size:	26x26mm^2

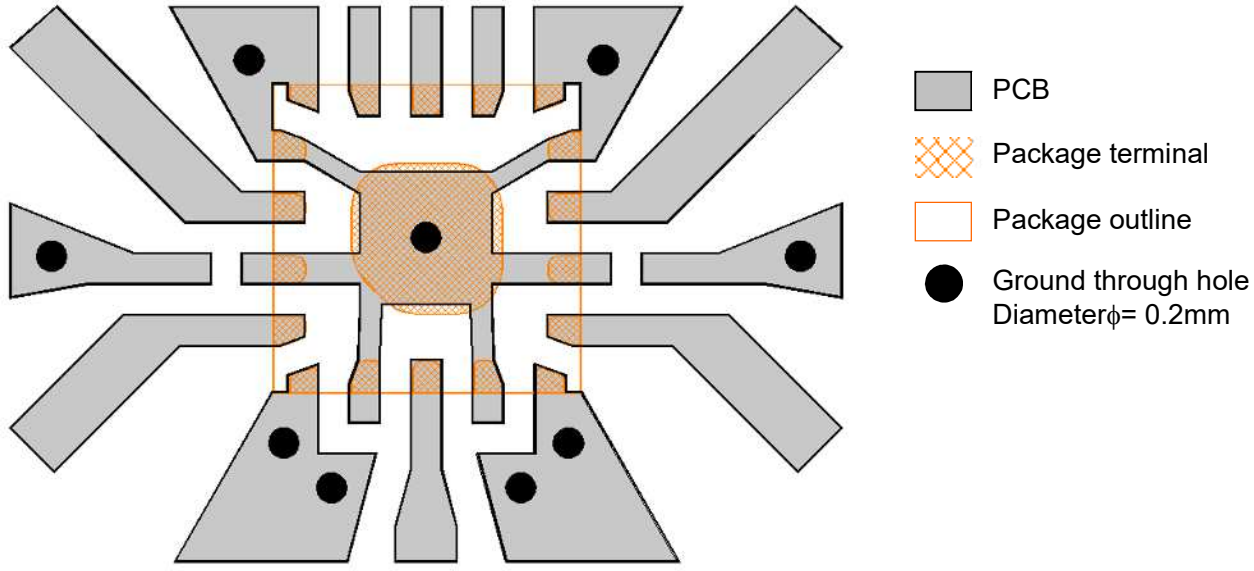
Losses of PCB and connectors, Ta=+25 °C

Frequency (GHz)	Loss (dB)
0.7	0.16
2.0	0.43
2.7	0.56
3.5	0.68
5.85	1.02

* L1 is

<PCB LAYOUT GUIDELINE>

(TOP VEIW)



■ PRECAUTIONS

[1] No DC block capacitors are required for RF ports unless DC is biased externally. When other device biased at certain voltage is connected to the NJG1809ME7, a DC block capacitor is required between the device and this switch IC. This is because the each RF port of this switch is biased at ground level.

[2] For avoiding the degradation of RF performance, the bypass capacitor (C1) should be placed as close as possible to VDD terminal.

[3] For good RF performance, all GND terminals are must be connected to PCB ground plane of substrate, and through holes for GND should be placed near the IC.

[4] Please connect Exposed PAD to PCB ground plane of substrate, and through holes for ground should be placed under the IC.

■ RECOMMENDED FOOTPRINT PATTERN (EQFN18-E7 PACKAGE REFERENCE)

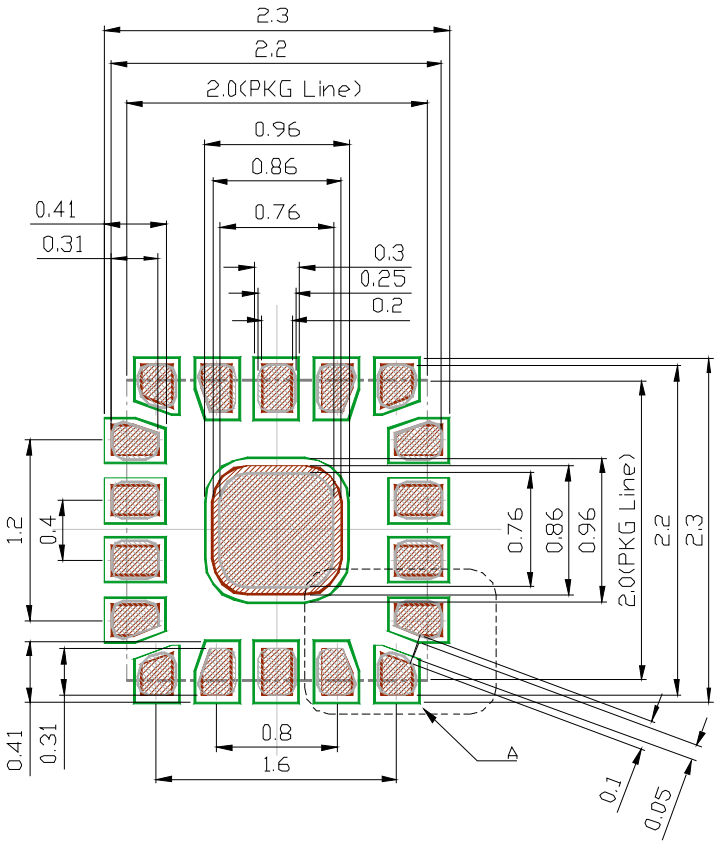
: Land

: Mask (Open area) *Metal mask thickness: 100μm

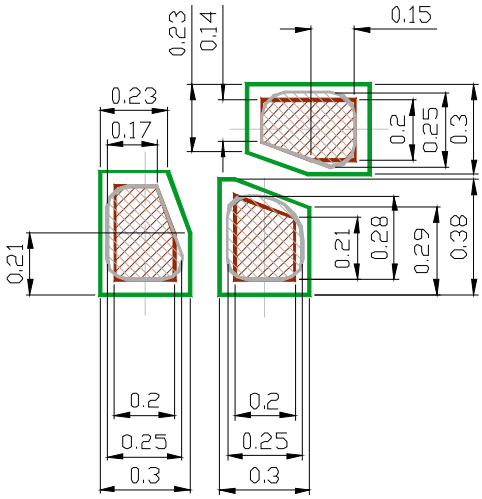
: Resist (Open area)

PKG: 2.0x2.0mm^2
Pin pitch: 0.4mm

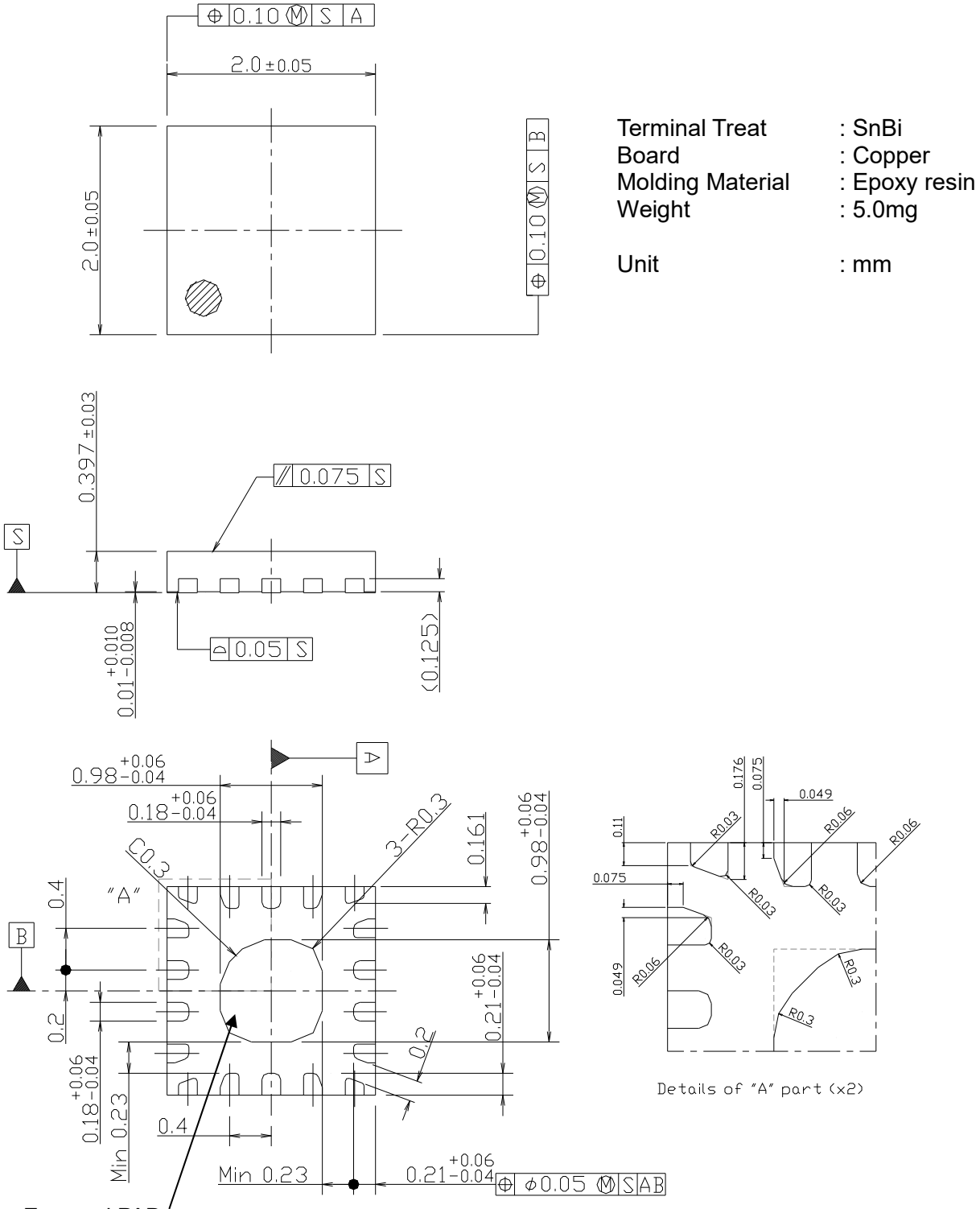
Unit: mm



Detail A



■ PACKAGE OUTLINE (EQFN18-E7)



Terminal Treat	: SnBi
Board	: Copper
Molding Material	: Epoxy resin
Weight	: 5.0mg
Unit	: mm

Cautions on using this product

This product contains Gallium-Arsenide (GaAs) which is a harmful material.

- Do NOT eat or put into mouth.
- Do NOT dispose in fire or break up this product.
- Do NOT chemically make gas or powder with this product.
- To waste this product, please obey the relating law of your country.

This product may be damaged with electric static discharge (ESD) or spike voltage. Please handle with care to avoid these damages.

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    In the case of a product purchased through an authorized distributor or directly from us, the warranty period for this product shall be one (1) year after delivery to your company. For defective products that occurred during this period, we will take the quality warranty measures described in section 8-2. However, if there is an agreement on the warranty period in the basic transaction agreement, quality assurance agreement, delivery specifications, etc., it shall be followed.
    8-2. Quality Warranty Remedies
    When it has been proved defective due to manufacturing factors as a result of defect analysis by us, we will either deliver a substitute for the defective product or refund the purchase price of the defective product.
    Note that such delivery or refund is sole and exclusive remedies to your company for the defective product.
    8-3. Remedies after Quality Warranty Period
    With respect to any defect of this product found after the quality warranty period, the defect will be analyzed by us. On the basis of the defect analysis results, the scope and amounts of damage shall be determined by mutual agreement of both parties. Then we will deal with upper limit in Section 8-2. This provision is not intended to limit any legal rights of your company.
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12. Warning for handling Gallium and Arsenic (GaAs) products (Applying to GaAs MMIC, Photo Reflector). These products use Gallium (Ga) and Arsenic (As) which are specified as poisonous chemicals by law. For the prevention of a hazard, do not burn, destroy, or process chemically to make them as gas or power. When the product is disposed of, please follow the related regulation and do not mix this with general industrial waste or household waste.
13. Please contact our sales representatives should you have any questions or comments concerning the products or the technical information.

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