Version 1.2 2008

# PEX 8505

## *Flexible & Versatile PCI Express® Switch*

### Features

- **PEX 8505 General Features**
  - 5-lane PCI Express switch
    - Gen 1 (2.5Gbps) Integrated SerDes
  - Up to five ports (x1, x2)
  - 15mm x 15mm, 196-ball PBGA pkg.
  - Typical Power: 0.8 Watts
- **PEX 8505 Key Features**
  - **Standards Compliant**
    - PCI Express Base Specification, r1.1
    - PCI Power Management Interface Specification r1.2
  - **High Performance**
    - Cut-thru with low packet latency
    - Max Payload Size of 1024 Bytes
    - Non-blocking internal architecture
    - Full line rate on all ports
  - **Flexible Configuration**
    - Five flexible & configurable ports (x1, x2)
    - Lane and polarity reversal
    - Configurable with strapping pins, EEPROM, $I^2C$ or Host software
  - **PCI Express Power Management**
    - Link power management states: L0, L0s, L1, L2/L3 Ready and L3
    - Device states: D0 and D3hot
  - **Quality of Service (QoS)**
    - One Virtual Channel per port
    - Eight Traffic Classes per port
    - Weighted Round-Robin Ingress Port Arbitration
  - **Reliability, Availability, Serviceability**
    - Three Standard Hot-Plug Controllers supporting PCI SHPC spec r1.0
    - Transaction layer end-to-end CRC
    - Poison bit support
    - Basic and Advanced Error Reporting support
    - Per port error diagnostics
      - Bad DLLPs
      - Bad TLPs
      - CRC errors and more
    - Fatal Error (FATAL_ERR#) signal (legacy SERR equivalent)
    - INTA# signal
    - Port status bits
    - Eight software controllable General Purpose Output (GPO) signals
    - JTAG boundary scan

### Low-Power 5-Lane, 5-Port *ExpressLane*™ PCIe Switch

The PEX 8505 device offers PCI Express switching capability conforming to the PCI Express Base specification revision 1.1. This device enables users to add scalable high bandwidth, non-blocking interconnects at the lowest cost to a wide variety of applications including communications platforms, consumer products, servers, storage systems, blade servers, industrial systems and embedded-control products. The PEX 8505 can be used as a **fan-out**, or **peer-to-peer** switch, and is well-suited for **Control Plane Applications, I/O Expansion, Video Surveillance, Multi-Function Printers, DVRs, Industrial Control Systems, Medical Imaging Systems, Embedded Systems** and **AMC** modules.

### Port Configurations

The PEX 8505 offers five lanes and up to five ports supporting x1 and x2 lane widths. The PEX 8505 features a **flexible central packet memory** that allocates a memory buffer for each port as required by the application or endpoint. This buffer allocation along with the device's **flexible packet flow control** minimizes bottlenecks when the upstream and aggregated downstream bandwidths do not match.

### High Performance

The PEX 8505 architecture supports packet **cut-thru with low latency (138ns).** This, combined with large packet memory **(up to 1024 byte maximum payload size)** and **non-blocking internal switch architecture**, provides **full line rate** on all ports for performance hungry applications such as docking stations, control planes, embedded systems and AMC modules.

### End-to-End Packet Integrity

The PEX 8505 provides **end-to-end CRC** protection (ECRC) and **Poison-bit support** to enable designs that require **end-to-end data integrity**. These features are optional in the PCI Express specification, but PLX provides them across its entire *ExpressLane* switch product line.

### Configuration Flexibility

The PEX 8505 provides several ways to configure its operations. The device can be configured through strapping pins, **$I^2C$ interface**, CPU configuration cycles, or an optional serial EEPROM. This allows for easy debug during the development phase, performance monitoring during the operation phase, and driver or software upgrade.

### Interoperability

The PEX 8505 is designed to be fully compliant with the PCI-SIG PCI Express base specification revision 1.1. Additionally, it supports **auto-negotiation**, **lane reversal**, and **polarity reversal**. The PEX 8505 also undergoes thorough Interoperability testing in PLX's **Interoperability Lab.**

### Low Power with Granular SerDes Control

The PEX 8505 provides **low power capability** that is fully compliant with the PCI Express power management specification. For even lower power, the SerDes physical links can be programmed for desired power or turned off when unused.

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## Port Configurations

The lane width of each port can be individually configured through auto-negotiation, hardware strapping, host software configuration, $I^2C$ interface, or through an optional EEPROM.

The PEX 8505 supports three port configurations:

1) One x1 upstream port and four x1 downstream ports
2) One x2 upstream port and three x1 downstream ports
3) One x2 upstream port, one x2 downstream port, one x1 downstream port

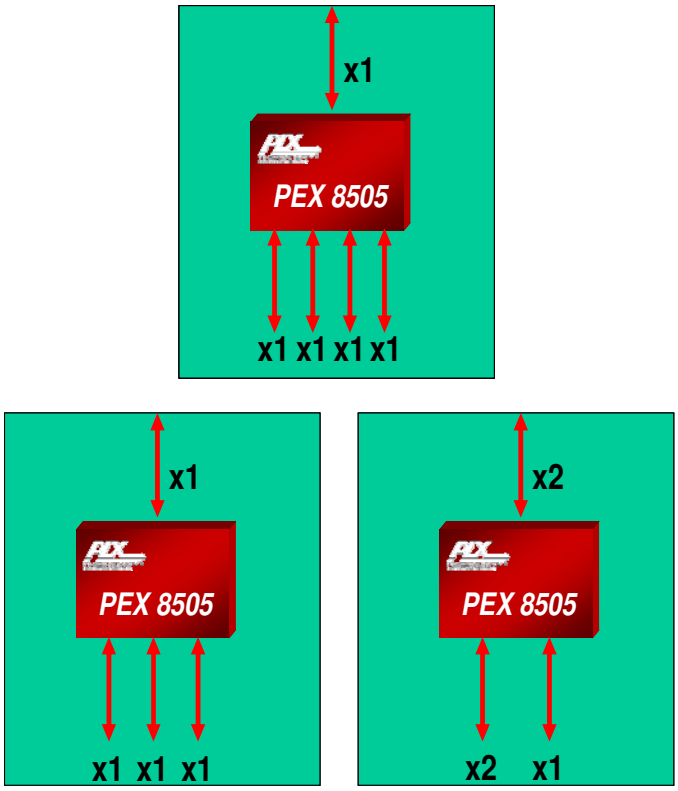



**Figure 1. Port Configurations**

## Hot-Plug for High Availability

Hot-Plug capability allows users to replace hardware modules and perform maintenance without powering down the system. The PEX 8505 **Hot-Plug** capability and **Advanced Error Reporting** features make it suitable for **High Availability (HA) applications**. Ports 1, 2 & 3 include a **Standard Hot-Plug Controller**. If the PEX 8505 is used in an application where one or more of its downstream ports connect to PCI Express slots, Hot-Plug Controllers on the three downstream ports can be used to manage the hot plug event of its associated slot.

## Fully Compliant Power Management

For applications that require power management, the ExpressLane PEX 8505 devices support both link (L0, L0s, L1, L2/L3 Ready and L3) and device (D0 and D3hot) power management states, in compliance with the PCI Express power management specification.

## SerDes Power and Signal Management

The ExpressLane PEX 8505 supports **software control** of the **SerDes outputs** to allow optimization of power and signal strength in a system. The PLX SerDes implementation supports four levels of power – off, low, typical, and high. The SerDes block also supports **loop-back modes** and **advanced reporting of error conditions**, which enables efficient debug and management of the entire system.

## Port Arbitration

The PEX 8505 switch supports hardware fixed and **Weighted Round-Robin Ingress Port Arbitration**. This allows fine tuning of Quality of Service and efficient use of packet buffers and the system bandwidth.

# Applications

Suitable for **control plane applications, multi-function printers, DVRs, industrial control systems, medical imaging systems, embedded systems & AMC modules,** the PEX 8505 can be configured for a wide variety of form factors and applications.

## Control Plane Application

The PEX 8505 is ideal for migrating existing PCI control planes in routers to high-speed PCI Express interface to meet increased packet processing needs. Figure 2 shows a controller card with a PEX 8505 connecting the Control Processor to as many as four devices each via a x1 port. This usage model provides connectivity to multiple devices giving the processor control over multiple devices in mid-range routers.

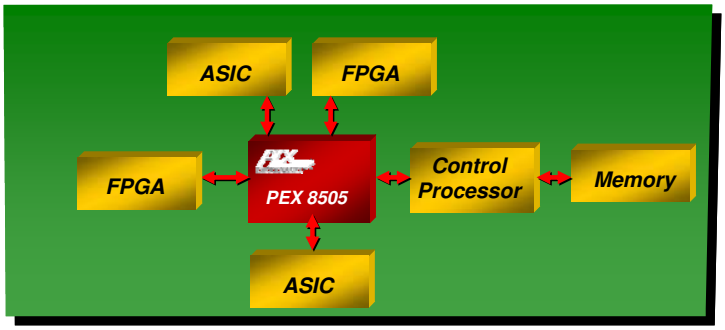



**Figure 2. Control Plane**

## I/O Expansion

The PEX 8505 can be used in I/O expansion applications. Together with a PCI Express-to-PCI bridge, the PEX 8505 is capable of providing legacy PCI I/O expansion support. Each x1 port in the PEX 8505 provides 250MB/s bandwidth per direction and it is more than capable of supporting the various bus widths and bus speeds of legacy PCI. Please visit the www.plxtech.com/bridges for additional information on PLX's PCI Express bridge family.

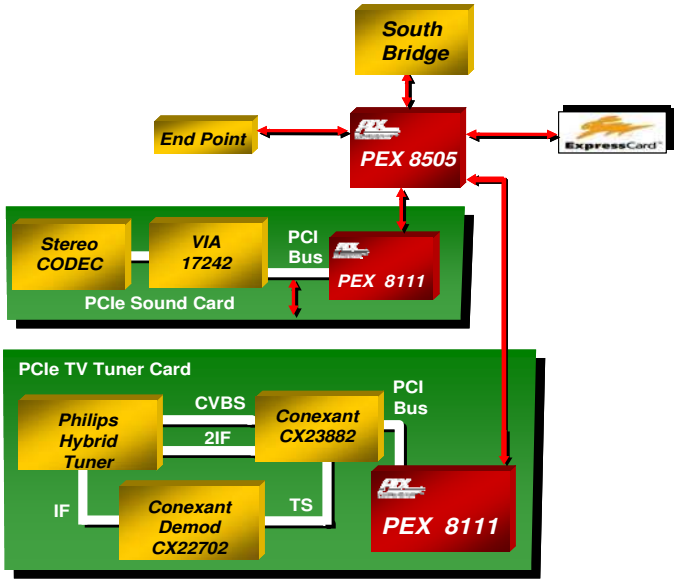



**Figure 3. I/O Expansion**

## Video Surveillance

A video surveillance application is another example for an embedded application. When used together with a PEX 8311, PCI Express-to-local bus bridges, the PEX 8505 can connect to other embedded devices, such as FPGAs. This allows video capture devices to interface to a PCI Express host taking advantage of the PCI Express performance. For more information on the PCI Express-to-Local Bus bridge, please visit PLX's website at www.plxtech.com/bridges.

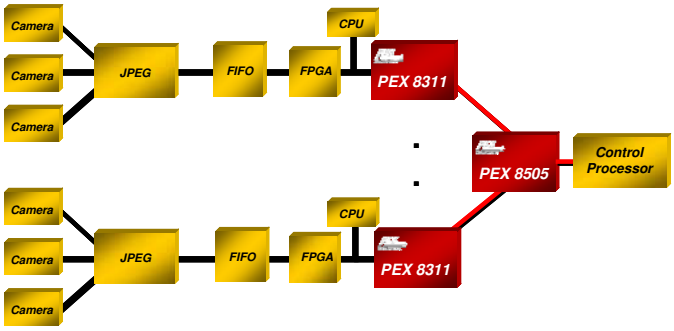



**Figure 4. Video Surveillance**

## Printer Application

In a printer application, low power and low latency devices are commonly used. Figure 5 shows an example of a printer application. In this example, the low power processor used provides a limited number of PCI Express ports. The PEX 8505 can be used to provide four additional PCI Express ports for the connectivity of other system peripherals such as Ethernet as well any proprietary PCI Express based ASICs. The Peer-to-Peer feature in the PEX 8505, allows a peripheral connected on a downstream port the ability to transfer data directly to another peripheral device. As shown in Figure 5, the ASIC connected to the scanner side can transfer data directly to the PCIe Slot and/or the ASIC connected on the Marking Engine side resulting in a low latency data transfer. In this case, the processor is not directly involved in the transfer.

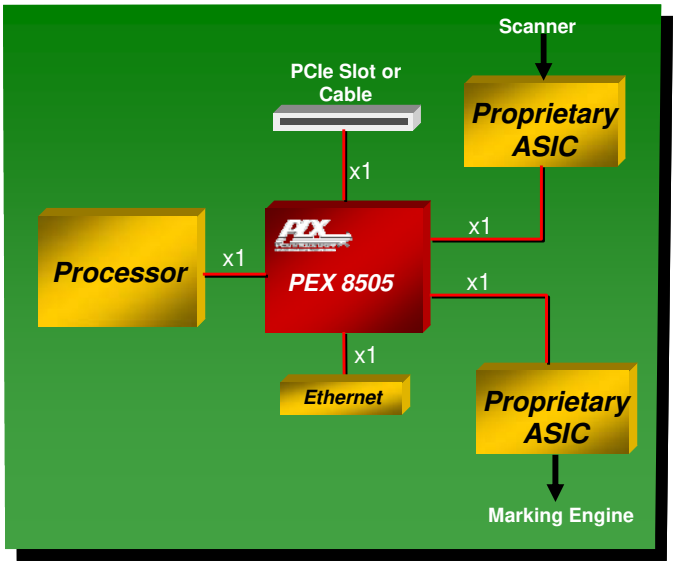



**Figure 5. Printer Engine**

## Software Usage Model

From a system model viewpoint, each PCI Express port is a virtual PCI to PCI bridge device with its own set of PCI Express configuration registers. It is through the upstream port that the BIOS or host can configure the other ports using standard PCI enumeration. The virtual PCI to PCI bridges within the PEX 8505 are compliant to the PCI and PCI Express system models. The Configuration Space Registers (CSRs) in a virtual primary/secondary PCI to PCI Bridge are accessible by type 0 configuration cycles through the virtual primary bus interface (matching bus number, device number, and function number).

## Interrupt Sources/Events

The ExpressLane PEX 8505 switch supports the INTx interrupt message type (compatible with the PCI 2.3 Interrupt signals) or Message Signaled Interrupts (MSI) when enabled. Interrupts/messages are generated by the PEX 8505 for hot plug events, baseline error reporting, and advanced error reporting.

## Development Tools

PLX offers the PEX 8505RDK which includes hardware and software tools to enable rapid customer design activity. These tools consist of a hardware module, hardware documentation and a Software Development Kit (SDK).

## ExpressLane PEX 8505RDK

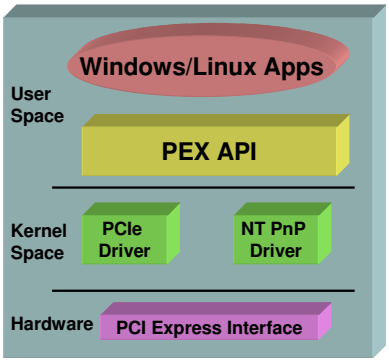
The RDK hardware includes three modules: the PEX 8505 base board, the Port Expander which provides four x1 ports, and a PCI Express adapter board which provides connection to the Host slot.

The PEX 8505RDK hardware module is configured as a bench-top board to provide five ports. The adapter board routes the PCI Express signals from the Host slot to a standard (PCI SIG defined) PCI Express x1 cable connector. The connection between the PEX 8505 and the host is made via the x1 cable. The PEX 8505RDK can be used to test and validate customer software. Additionally, it can be used as an evaluation vehicle for the PEX 8505 features and benefits.

## SDK

The SDK tool set includes:

- Linux and Windows drivers
- C/C++ Source code, Objects, libraries
- User's Guides, Application examples, Tutorials



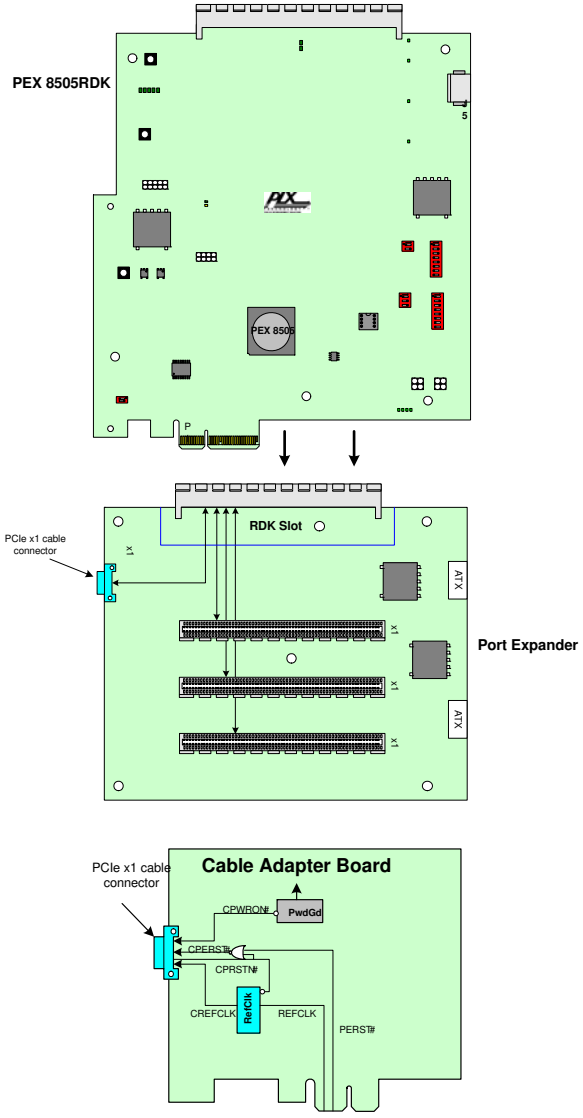




**Figure 6. PEX 8505RDK**

## Product Ordering Information

| Part Number | Description |
|---|---|
| PEX 8505-AA25BI | 5-Lane, 5-port PCI Express Switch |
| PEX 8505-AA25BI G | 5-Lane, 5-port PCI Express Switch Pb-Free |
| PEX 8505-AA RDK Kit | PEX 8505 Rapid Development Kit Base Board; x1 PCIe Cable; x1 PCIe Cable Adapter and RDK Port Expander |

Please visit the PLX Web site at http://www.plxtech.com/8505 or contact PLX sales at 408-774-9060 for sampling.

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