FAIRCHILD SEMICONDUCTOR™

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74F193
Up/Down Binary Counter with Separate Up/Down Clocks

General Description

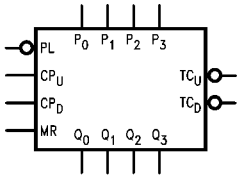
The F193 is an up/down modulo-16 binary counter. Separate Count Up and Count Down Clocks are used, and in either counting mode the circuits operate synchronously. The outputs change state synchronously with the LOW-to-HIGH transitions on the clock inputs. Separate Terminal Count Up and Terminal Count Down outputs are provided that are used as the clocks for subsequent stages without extra logic, thus simplifying multi-stage counter designs. Individual preset inputs allow the circuit to be used as a programmable counter. Both the Parallel Load ($\overline{PL}$) and the Master Reset (MR) inputs asynchronously override the clocks.

Ordering Code:

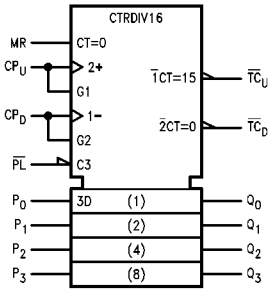
Order Number	Package Number	Package Description
74F193SC	M16A	16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow Body
74F193SJ	M16D	16-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74F193PC	N16E	16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

Devices also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering code.

Logic Symbols

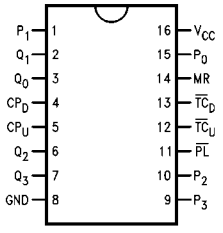


IEEE/IEC



Connection Diagram

Pin Assignment for DIP, SOIC and SOP



Unit Loading/Fan Out

Pin Names	Description	U.L. HIGH/LOW	Input I_{IH}/I_{IL} Output I_{OH}/I_{OL}
CP_U	Count Up Clock Input (Active Rising Edge)	1.0/3.0	20 µA/–1.8 mA
CP_D	Count Down Clock Input (Active Rising Edge)	1.0/3.0	20 µA/–1.8 mA
MR	Asynchronous Master Reset Input (Active HIGH)	1.0/1.0	20 µA/–0.6 mA
$\overline{PL}$	Asynchronous Parallel Load Input (Active LOW)	1.0/1.0	20 µA/–0.6 mA
P_0–P_3	Parallel Data Inputs	1.0/1.0	20 µA/–0.6 mA
Q_0–Q_3	Flip-Flop Outputs	50/33.3	–1 mA/20 mA
$\overline{TC}_D$	Terminal Count Down (Borrow) Output (Active LOW)	50/33.3	–1 mA/20 mA
$\overline{TC}_U$	Terminal Count Up (Carry) Output (Active LOW)	50/33.3	–1 mA/20 mA

Functional Description

The F193 is a 4-bit binary synchronous up/down (reversible) counter. It contains four edge-triggered flip-flops, with internal gating and steering logic to provide master reset, individual preset, count up and count down operations.

A LOW-to-HIGH transition on the CP input to each flip-flop causes the output to change state. Synchronous switching, as opposed to ripple counting, is achieved by driving the steering gates of all stages from a common Count Up line and a common Count Down line, thereby causing all state changes to be initiated simultaneously. A LOW-to-HIGH transition on the Count Up input will advance the count by one; a similar transition on the Count Down input will decrease the count by one. While counting with one clock input, the other should be held HIGH, as indicated in the Function Table.

The Terminal Count Up ($\overline{TC}_U$) and Terminal Count Down ($\overline{TC}_D$) outputs are normally HIGH. When the circuit has reached the maximum count state 15, the next HIGH-to-LOW transition of the Count Up Clock will cause $\overline{TC}_U$ to go LOW. $\overline{TC}_U$ will stay LOW until CP_U goes HIGH again, thus effectively repeating the Count Up Clock, but delayed by two gate delays. Similarly, the $\overline{TC}_D$ output will go LOW when the circuit is in the zero state and the Count Down Clock goes LOW. Since the $\overline{TC}$ outputs repeat the clock waveforms, they can be used as the clock input signals to the next higher order circuit in a multistage counter.

$$\overline{TC}_U = Q_0 \cdot Q_1 \cdot Q_2 \cdot Q_3 \cdot \overline{CP}_U$$

$$\overline{TC}_D = \overline{Q}_0 \cdot \overline{Q}_1 \cdot \overline{Q}_2 \cdot \overline{Q}_3 \cdot \overline{CP}_D$$

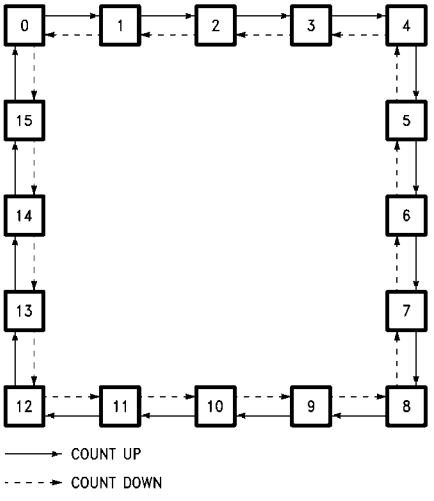
The F193 has an asynchronous parallel load capability permitting the counter to be preset. When the Parallel Load ($\overline{PL}$) and the Master Reset (MR) inputs are LOW, information present on the Parallel Data input (P_0–P_3) is loaded into the counter and appears on the outputs regardless of the conditions of the clock inputs. A HIGH signal on the Master Reset input will disable the preset gates, override both clock inputs, and latch each Q output in the LOW state. If one of the clock inputs is LOW during and after a reset or load operation, the next LOW-to-HIGH transition of that clock will be interpreted as a legitimate signal and will be counted.

Function Table

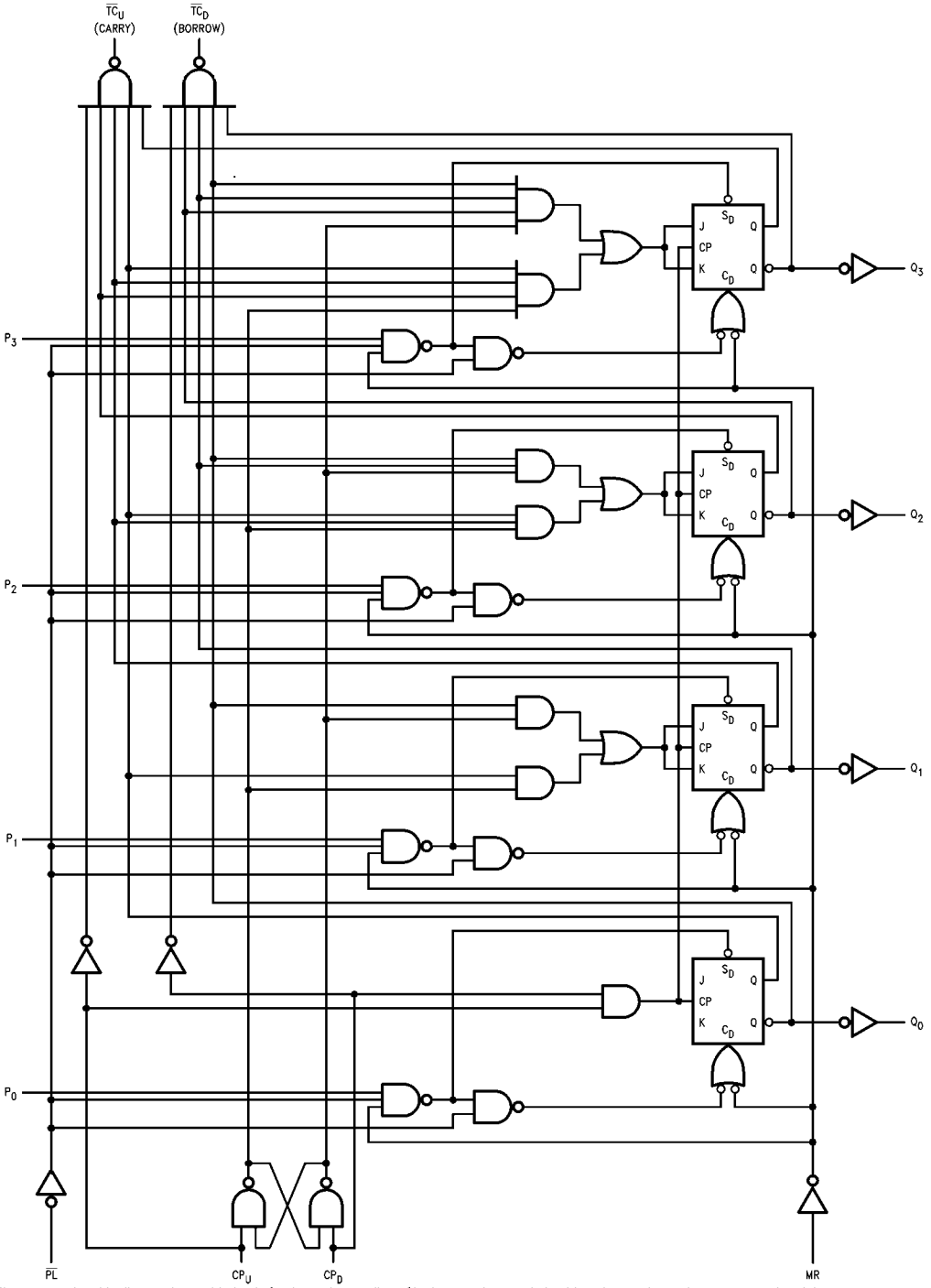
MR	$\overline{PL}$	CP_U	CP_D	Mode
H	X	X	X	Reset (Asyn.)
L	L	X	X	Preset (Asyn.)
L	H	H	H	No Change
L	H	↗	H	Count Up
L	H	H	↗	Count Down

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
↗ = LOW-to-HIGH Clock Transition

State Diagram



Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings(Note 1)

Storage Temperature	−65°C to +150°C
Ambient Temperature under Bias	−55°C to +125°C
Junction Temperature under Bias	−55°C to +150°C
V_{CC} Pin Potential to Ground Pin	−0.5V to +7.0V
Input Voltage (Note 2)	−0.5V to +7.0V
Input Current (Note 2)	−30 mA to +5.0 mA
Voltage Applied to Output in HIGH State (with V_{CC} = 0V)	
Standard Output	−0.5V to V_{CC}
3-STATE Output	−0.5V to +5.5V
Current Applied to Output in LOW State (Max)	twice the rated I_{OL} (mA)

Recommended Operating Conditions

Free Air Ambient Temperature	0°C to +70°C
Supply Voltage	+4.5V to +5.5V

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

DC Electrical Characteristics

Symbol	Parameter		Min	Typ	Max	Units	V_{CC}	Conditions
V_{IH}	Input HIGH Voltage		2.0			V		Recognized as a HIGH Signal
V_{IL}	Input LOW Voltage				0.8	V		Recognized as a LOW Signal
V_{CD}	Input Clamp Diode Voltage				−1.2	V	Min	I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	10% V_{CC}	2.5			V	Min	I_{OH} = −1 mA
		5% V_{CC}	2.7					I_{OH} = −1 mA
V_{OL}	Output LOW Voltage	10% V_{CC}			0.5	V	Min	I_{OL} = 20 mA
I_{IH}	Input HIGH Current				5.0		Max	V_{IN} = 2.7V
I_{BVI}	Input HIGH Current Breakdown Test				100 7.0	µA	Max	V_{IN} = 7.0V
I_{CEX}	Output HIGH Leakage Current				50	µA	Max	V_{OUT} = V_{CC}
V_{ID}	Input Leakage Test		4.75			V	0.0	I_{ID} = 1.9 µA All Other Pins Grounded
I_{OD}	Output Leakage Circuit Current				3.75	µA	0.0	V_{IOD} = 150 mV All Other Pins Grounded
I_{IL}	Input LOW Current				−0.6 −1.8	mA	Max	V_{IN} = 0.5V ($\overline{MR}$, $\overline{PL}$, P_n) V_{IN} = 0.5V (CP_u, CP_D)
I_{OS}	Output Short-Circuit Current		−60		−150	mA	Max	V_{OUT} = 0V
I_{CC}	Power Supply Current			38	55	mA	Max	

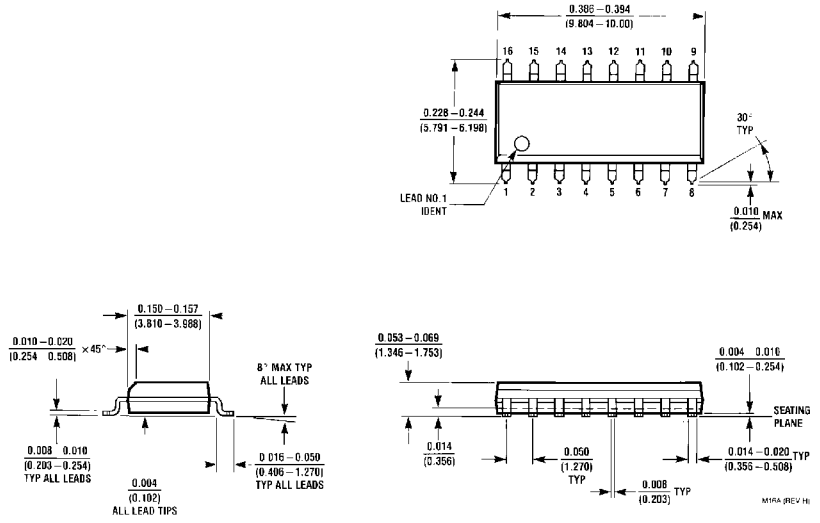
AC Electrical Characteristics

Symbol	Parameter	$T_A = +25°C$, $V_{CC} = +5.0V$, $C_L = 50$ pF			T_A, V_{CC} = Com, $C_L = 50$ pF		Units
		Min	Typ	Max	Min	Max	
f_{max}	Maximum Count Frequency	100	125		90		MHz
t_{PLH}	Propagation Delay	4.0	7.0	9.0	4.0	10.0	
t_{PHL}	CP_U or CP_D to	3.5	6.0	8.0	3.5	9.0	ns
	$\overline{TC}_U$ or $\overline{TC}_D$						
t_{PLH}	Propagation Delay	4.0	6.5	8.5	4.0	9.5	ns
t_{PHL}	CP_U or CP_D to Q_n	5.5	9.5	12.5	5.5	13.5	
t_{PLH}	Propagation Delay	3.0	4.5	7.0	3.0	8.0	ns
t_{PHL}	P_n to Q_n	6.0	11.0	14.5	6.0	15.5	
t_{PLH}	Propagation Delay	5.0	8.5	11.0	5.0	12.0	ns
t_{PHL}	$\overline{PL}$ to Q_n	5.5	10.0	13.0	5.5	14.0	
t_{PHL}	Propagation Delay	5.5	11.0	14.5	5.5	15.5	
	MR to Q_n						
t_{PLH}	Propagation Delay	6.0	10.5	13.5	6.0	14.5	ns
	MR to $\overline{TC}_U$						
t_{PHL}	Propagation Delay	6.0	11.5	14.5	6.0	15.5	
	MR to $\overline{TC}_D$						
t_{PLH}	Propagation Delay	7.0	12.0	15.5	7.0	16.5	ns
t_{PHL}	$\overline{PL}$ to $\overline{TC}_U$ or $\overline{TC}_D$	7.0	11.5	14.5	7.0	15.5	
t_{PLH}	Propagation Delay	7.0	11.5	14.5	7.0	15.5	ns
t_{PHL}	P_n to $\overline{TC}_U$ or $\overline{TC}_D$	6.5	11.0	14.0	6.5	15.0	

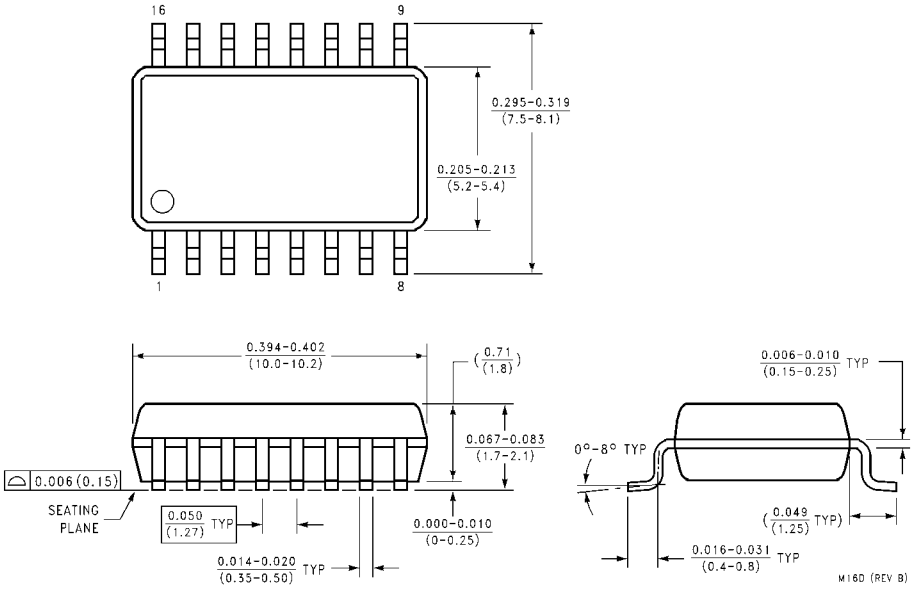
AC Operating Requirements

Symbol	Parameter	$T_A = +25°C$, $V_{CC} = +5.0V$		T_A, V_{CC} = Com		Units
		Min	Max	Min	Max	
$t_s(H)$	Setup Time, HIGH or LOW	4.5		5.0		
$t_s(L)$	P_n to $\overline{PL}$	4.5		5.0		
$t_h(H)$	Hold Time, HIGH or LOW	2.0		2.0		ns
$t_h(L)$	P_n to $\overline{PL}$	2.0		2.0		
$t_w(L)$	$\overline{PL}$ Pulse Width, LOW	6.0		6.0		ns
$t_w(L)$	CP_U or CP_D	5.0		5.0		ns
	Pulse Width, LOW					
$t_w(L)$	CP_U or CP_D					
	Pulse Width, LOW	10.0		10.0		ns
	(Change of Direction)					
$t_w(H)$	MR Pulse Width, HIGH	6.0		6.0		ns
t_{rec}	Recovery Time	6.0		6.0		ns
	$\overline{PL}$ to CP_U or CP_D					
t_{rec}	Recovery Time	4.0		4.0		ns
	MR to CP_U or CP_D					

Physical Dimensions inches (millimeters) unless otherwise noted

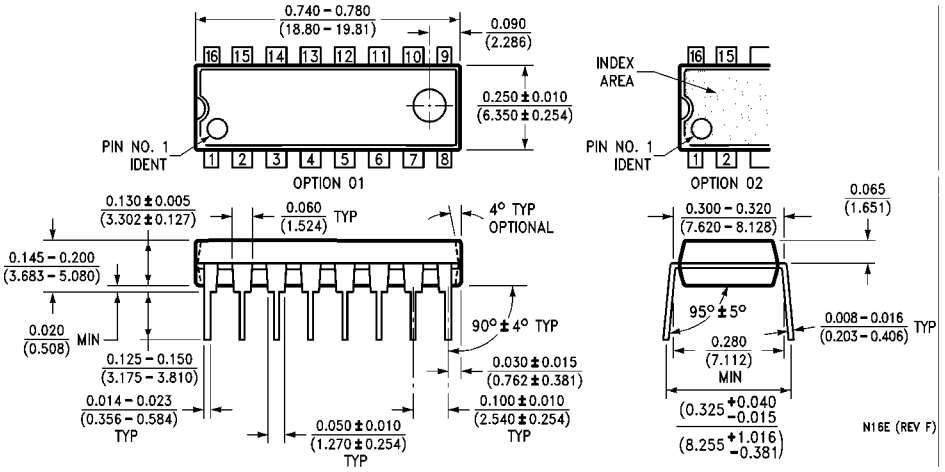


16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow Body
Package Number M16A



16-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
Package Number M16D

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide
Package Number N16E

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2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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