HARRIS SEMICONDUCTOR

HM-8832

32K x 8 Asynchronous CMOS Static RAM Module

January 1992

Features

- Full CMOS Six Transistor Memory Cell
- Low Standby Supply Current 250µA
- Low Operating Supply Current..... 15mA
- Fast Address Access Time 180ns
- Low Data Retention Supply Voltage..... 2.0V
- CMOS/TTL Compatible Inputs/Outputs
- JEDEC Approved Pinout
- Equal Cycle and Access Times
- No Clocks or Strobes Required
- Single 5V Power Supply
- Easy Microprocessor Interfacing
- Operating Temperature Range ..... -55°C to +125°C
- Standard DIP Size - 0.6" x 1.4"

Ordering Information

PKG	TEMP. RANGE	180ns/200µA*	180ns/750µA*
MODULE	-55°C to +125°C	HM5-8832B-8	HM5-8832-8

* Access Time/Data Retention Supply Current

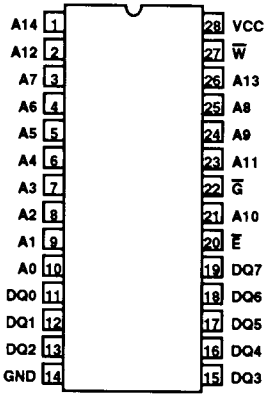
Description

The HM-8832 is a 32K x 8 Bit Asynchronous CMOS Static RAM Module based on a multilayered, co-fired, dual-in-line ceramic substrate, four HM-65642 CMOS Asynchronous Static RAMs, and an HCT-138 high-speed CMOS decoder, all mounted in ceramic leadless chip carriers. In addition to this, each module is equipped with a ceramic capacitor to minimize power supply noise and reduce the need for external decoupling. Furthermore, this capacitor is sealed in a ceramic leadless carrier for maximum reliability, even in extreme environments. All inputs on the HM-8832 are gated by the $\overline{E}$ input to simplify system design requirements to obtain the minimum standby and data retention supply current. The pinout of the HM-8832 conforms with the JEDEC standard for eight-bit wide, 28 pin RAMs, which allows the module to be pin compatible with future generations of high density RAMs and EPROMs.

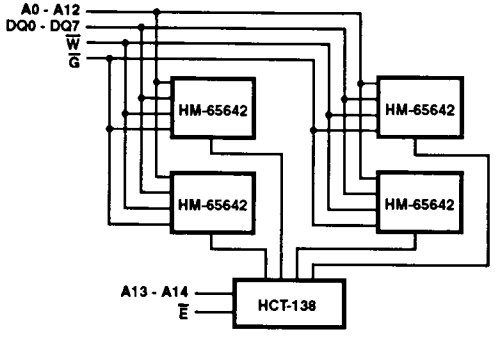
The HM-65642 RAMs used on the HM-8832 module are full CMOS devices, utilizing arrays of six-transistor (6T) memory cells for the most stable and lowest possible standby and data retention supply current over the full military operating temperature range. In addition to this, the high stability of the 6T cell provides excellent protection against soft errors due to power supply noise and alpha particles. This stability also improves the radiation tolerance of the module over that of RAMs utilizing four transistor (4T) Mix-MOS memory cells.

Pinout

28 LEAD MODULE
TOP VIEW



Functional Diagram



TRUTH TABLE

MODE	$\overline{E}$	$\overline{W}$	$\overline{G}$
Standby (CMOS)	VCC	X	X
Standby (TTL)	VIH	X	X
Enabled (High Z)	VIL	VIH	VIH
Read	VIL	VIH	VIL
Write	VIL	VIL	X

PIN DESCRIPTION

PIN	FUNCTION
A0 - A14	Address Inputs
DQ0 - DQ7	Data Input/Output
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
$\overline{W}$	Write Enable
VCC	Power (+5V)
GND	Ground

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number 3008

Absolute Maximum Ratings

Supply Voltage ..... +7.0V
Input, Output or I/O Voltage ..... GND-0.3V to VCC+0.3V
Storage Temperature Range ..... -65°C to +150°C
Junction Temperature ..... +175°C
Lead Temperature (Soldering 10s) ..... +300°C
Gate Count ..... 405,230 Gates

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Operating Conditions

Operating Voltage Range ..... +4.5V to +5.5V
Operating Temperature Range ..... -55°C to +125°C

DC Electrical Specifications

VCC = 5V ± 10%; T_A = -55°C to +125°C (HM-8832B-8, HM-8832-8)

SYMBOL	PARAMETER	LIMITS MIN	LIMITS MAX	UNITS	(NOTE 1) TEST CONDITIONS
ICCSBI	Standby Supply Current (CMOS)	-	250	µA	HM-8832B, IO = 0, $\overline{E}$ = VCC - 0.3V
		-	900	µA	HM-8832, IO = 0, $\overline{E}$ = VCC - 0.3V
ICCSB	Standby Supply Current (TTL)	-	2	mA	HM-8832B, IO = 0, $\overline{E}$ = VIH
		-	10	mA	HM-8832, IO = 0, $\overline{E}$ = VIH
ICCEN	Enabled Supply Current	-	10	mA	IO = 0, $\overline{E}$ = VIL
ICCOP	Operating Supply Current (Note 3)	-	15	mA	IO = 0, f = 1MHz, $\overline{E}$ = VIL, VIN = VCC or GND
ICCDR	Data Retention Supply Current	-	200	µA	HM-8832B, VCC = 2.0V, $\overline{E}$ = VCC - 0.3V
		-	750	µA	HM-8832, VCC = 2.0V, $\overline{E}$ = VCC - 0.3V
II	Input Leakage Current	-1.0	+1.0	µA	VIN = VCC or GND
IIOZ	I/O Leakage Current	-1.0	+1.0	µA	VIO = VCC or GND
VCCDR	Data Retention Supply Voltage	2.0	-	V	$\overline{E}$ = VCC
VOL	Output Voltage Low	-	0.4	V	IOL = 4.0mA
VOH1	Output Voltage High	2.4	-	V	IOH = -1.0mA
VOH2	Output Voltage High (Note 2)	VCC - 0.4	-	V	IOH = 100µA
VIL	Input Voltage Low	0	0.8	V	
VIH	Input Voltage High	2.4	VCC	V	

Capacitance

T_A = +25°C (Note 2)

SYMBOL	PARAMETER	MAX	UNITS	TEST CONDITIONS
CA	Address Input Capacitance	40	pF	VA = VCC or GND, f = 1MHz
CDQ, CG	Data, Output Enable Capacitance	45	pF	VDQ, VG = VCC or GND, f = 1MHz
CEN	Chip Enable Capacitance	15	pF	VEN = VCC or GND, f = 1MHz
CW	Write Enable Capacitance	60	pF	VW = VCC or GND, f = 1MHz

NOTES:

1. All devices tested at worst case temperature and supply voltage limits.
2. Guaranteed but not tested.
3. Typical derating 5mA/MHz increase in ICCOP.

AC Electrical Specifications VCC = 5V ± 10%, T_A = -55°C to +125°C (HM-8832B-8, HM-8832-8)

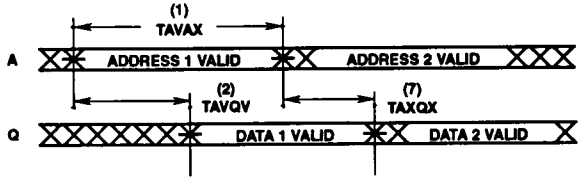
SYMBOL	PARAMETER		LIMITS HM-8832B-8 MIN	LIMITS HM-8832B-8 MAX	LIMITS HM-8832-8 MIN	LIMITS HM-8832-8 MAX	UNITS	(NOTES 1, 3) TEST CONDITIONS
READ CYCLE								
(1) TAVAX	Read Cycle Time		180	-	180	-	ns	
(2) TAVQV	Address Access Time		-	180	-	180	ns	
(3) TELQV	Chip Enable Access Time		-	180	-	180	ns	
(4) TGLQV	Output Enable Access Time		-	75	-	75	ns	
(5) TELQX	Chip Enable Output Enable Time		10	-	10	-	ns	(Note 2)
(6) TGLQX	Output Enable Time		5	-	5	-		(Note 2)
(7) TAXQX	Address Output Hold Time		10	-	10	-	ns	(Note 2)
(8) TEHQZ	Chip Disable Output Disable Time		0	80	0	80	ns	(Note 2)
(9) TGHQZ	Output Disable Time		0	55	0	55	ns	(Note 2)
WRITE CYCLE								
(10) TAVAX	Write Cycle Time		180	-	180	-	ns	
(11) TWLWH	Write Pulse Width		95	-	95	-	ns	
(12) TELWH	Chip Enable to End of Write	$\overline{W}$ Controlled	95	-	95	-	ns	
(13) TELEH	Chip Enable to End of Write	$\overline{E}$ Controlled	90	-	90	-	ns	(Note 2)
(14) TAVWL	Address Setup Time	$\overline{W}$ Controlled	30	-	30	-	ns	
(15) TAVEL	Address Setup Time	$\overline{E}$ Controlled	30	-	30	-	ns	(Note 2)
(16) TWHAX	Write Recovery Time	$\overline{W}$ Controlled	10	-	10	-	ns	
(17) TEHAX	Write Recovery Time	$\overline{E}$ Controlled	40	-	40	-	ns	(Note 2)
(18) TDVWH	Data Setup Time	$\overline{W}$ Controlled	65	-	65	-	ns	
(19) TDVEH	Data Setup Time	$\overline{E}$ Controlled	65	-	65	-	ns	(Note 2)
(20) TWHDX	Data Hold Time	$\overline{W}$ Controlled	10	-	10	-	ns	
(21) TEHDX	Data Hold Time	$\overline{E}$ Controlled	40	-	40	-	ns	(Note 2)
(22) TWLQZ	Write Enable Output Disable Time		-	15	-	55	ns	(Note 2)
(23) TWHQX	Write Disable Output Enable Time		5	-	5	-	ns	(Note 2)

NOTES:

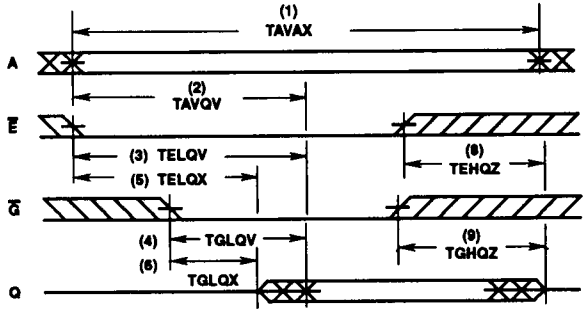
1. Input pulse levels: 0 to 3.0V; Input rise and fall times: 5ns (max); Input and output timing reference level: 1.5V; Output load: 1 TTL gate equivalent CL = 100pF (min) including scope and jig - for CL greater than 100pF, access time is derated by 0.15ns per pF.
2. Guaranteed but not tested.
3. All devices tested at worst case temperature and supply voltage limits.

Timing Diagram

READ CYCLE 1: ADDRESS CONTROLLED (Notes 1, 2)

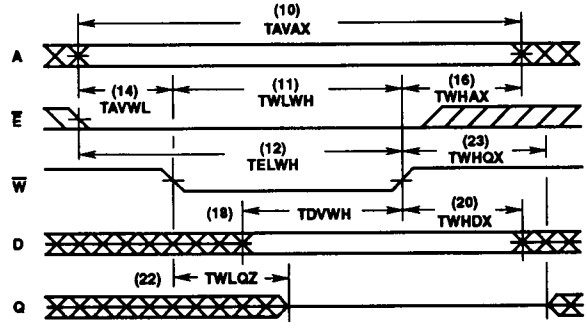


READ CYCLE 2: $\overline{E}$ OR $\overline{G}$ CONTROLLED (Note 1)

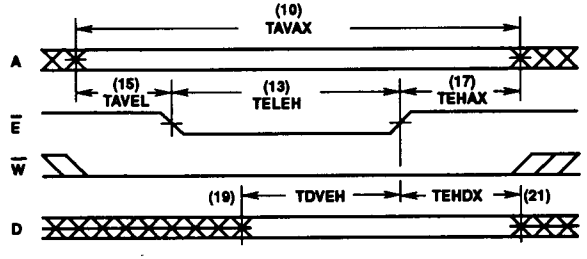


READ CYCLE NOTES: 1. In a read cycle, $\overline{W}$ is held high.
2. In read cycle 1, the module is kept continuously enabled: $\overline{E}$ and $\overline{G}$ are held low.

WRITE CYCLE 1: $\overline{W}$ CONTROLLED (Note 1)



WRITE CYCLE 1: $\overline{E}$ CONTROLLED (Note 2)



WRITE CYCLE NOTES: 1. In Write Cycle 1, the module is first enabled, and then data is strobed into the RAM with a pulse on $\overline{W}$. If $\overline{G}$ is held high for the entire cycle, the outputs will remain in the high impedance state. If $\overline{G}$ is held low, it may be necessary to lengthen the cycle to prevent bus contention. This would occur if TWLQZ and TDVWH overlapped.
2. In Write Cycle 2, Address (A) and Write Enable ($\overline{W}$) are first setup and then data is strobed into the RAM with a pulse on $\overline{E}$.