

74LVXZ161284 • 74LVXZ161284B

Low Voltage IEEE 161284 Translating Transceiver with Power-Up Protection

General Description

These transceivers contain eight bidirectional data buffers and eleven control/status buffers to implement a full IEEE 1284 compliant interface. The devices support the IEEE 1284 standard and are intended to be used in an Extended Capabilities Port mode (ECP). The pinout allows for easy connection from the Peripheral (A-side) to the Host (cable side).

Outputs on the cable side can be configured to be either open drain or high drive (± 14 mA) and are connected to a separate power supply pin ($V_{CC-Cable}$) that allows these outputs to be driven by a higher supply voltage than the A-side. The pull-up and pull-down series termination resistance of these outputs on the cable side is optimized to drive an external cable. In addition, the C inputs and the B and Y outputs on the cable side contain internal pull-up resistors connected to the $V_{CC-Cable}$ supply to provide proper input termination and pull-ups for open drain output mode.

Outputs on the Peripheral side are standard low-drive CMOS outputs designed to interface with 3V logic. The DIR input controls data flow on the A_1-A_8/B_1-B_8 transceiver pins.

The devices also have an added power-up protection feature which forces the Y outputs ($Y_9 - Y_{13}$) to a high state after power-on until one of the associated inputs ($A_9 - A_{13}$) goes HIGH. When an associated input ($A_9 - A_{13}$) goes HIGH, all Y outputs ($Y_9 - Y_{13}$) are activated.

The 74LVXZ161284B device provides increased noise tolerance for stable power-on circuit logic states.

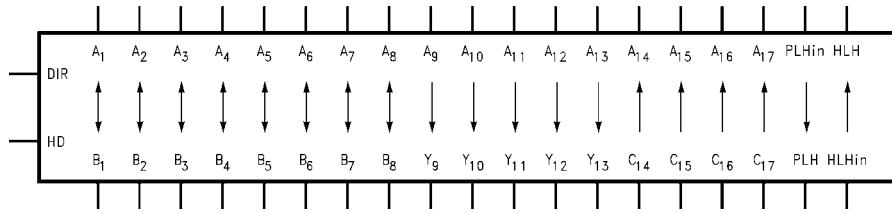
Features

- Supports IEEE 1284 Level 1 and Level 2 signaling standards for bidirectional parallel communications between personal computers and printing peripherals
- Translation capability allows outputs on the cable side to interface with 5V signals
- All inputs have hysteresis to provide noise margin
- B and Y output resistance optimized to drive external cable
- B and Y outputs in high impedance mode during power down
- C inputs and B, Y outputs on cable side have internal 1.4 k Ω pull-up resistors
- Flow-through pin configuration allows easy interface between the "Peripheral and Host"
- Replaces the function of two (2) 74ACT1284 devices
- Power-up protection prevents errors when the printer is powered on but no valid signal is at the input pins ($A_9 - A_{13}$).

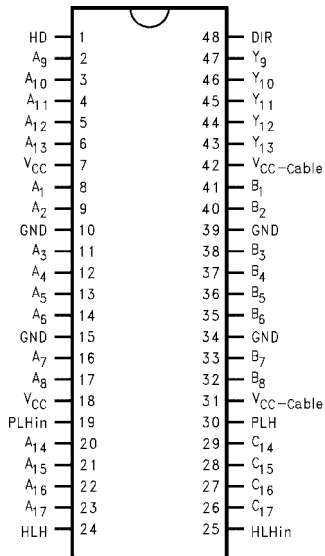
Ordering Code

Order Number	Package Number	Package Description
74LVXZ161284MEA	MS48A	48-Lead Small Shrink Outline Package (SSOP), JEDEC MO-118, 0.300" Wide [RAIL]
74LVXZ161284MEX	MS48A	48-Lead Small Shrink Outline Package (SSOP), JEDEC MO-118, 0.300" Wide [TAPE and REEL]
74LVXZ161284MTD	MTD48	48-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide [RAIL]
74LVXZ161284MTX	MTD48	48-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide [TAPE and REEL]
74LVXZ161284BMT	MTD48	48-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide [RAIL]
74LVXZ161284BTX	MTD48	48-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide [TAPE and REEL]

Logic Symbol



Connection Diagram



Pin Descriptions

Pin Names	Description
HD	High Drive Enable Input (Active HIGH)
DIR	Direction Control Input
A ₁ -A ₈	Inputs or Outputs
B ₁ -B ₈	Inputs or Outputs
A ₉ -A ₁₃	Inputs
Y ₉ -Y ₁₃	Outputs
A ₁₄ -A ₁₇	Outputs
C ₁₄ -C ₁₇	Inputs
PLH _{IN}	Peripheral Logic HIGH Input
PLH	Peripheral Logic HIGH Output
HLH _{IN}	Host Logic HIGH Input
HLH	Host Logic HIGH Output

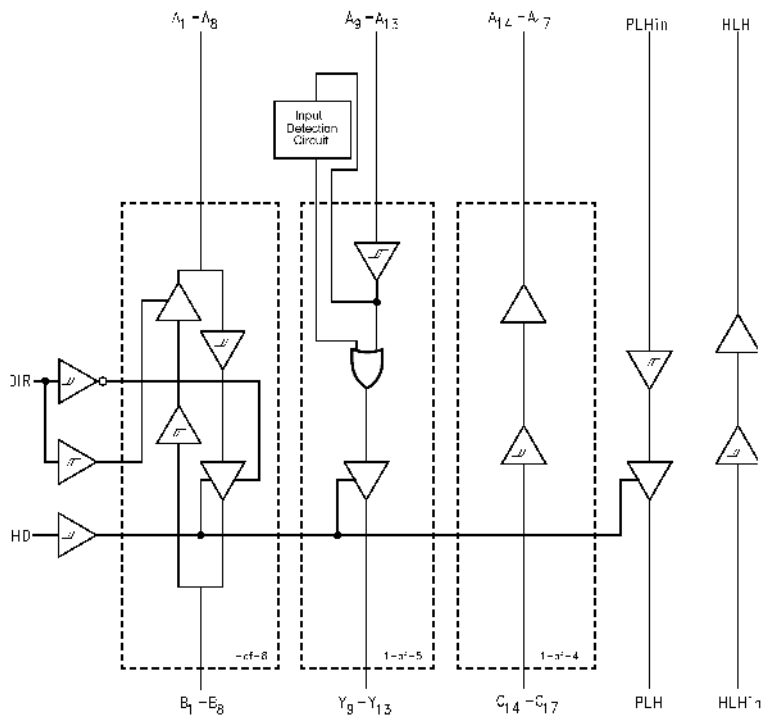
Truth Table

Inputs		Outputs
DIR	HD	
L	L	B ₁ -B ₈ Data to A ₁ -A ₈ , and A ₉ -A ₁₃ Data to Y ₉ -Y ₁₃ (Note 1) C ₁₄ -C ₁₇ Data to A ₁₄ -A ₁₇ PLH Open Drain Mode
L	H	B ₁ -B ₈ Data to A ₁ -A ₈ , and A ₉ -A ₁₃ Data to Y ₉ -Y ₁₃ C ₁₄ -C ₁₇ Data to A ₁₄ -A ₁₇
H	L	A ₁ -A ₈ Data to B ₁ -B ₈ (Note 2) A ₉ -A ₁₃ Data to Y ₉ -Y ₁₃ (Note 1) C ₁₄ -C ₁₇ Data to A ₁₄ -A ₁₇ PLH Open Drain Mode
H	H	A ₁ -A ₈ Data to B ₁ -B ₈ A ₉ -A ₁₃ Data to Y ₉ -Y ₁₃ C ₁₄ -C ₁₇ Data to A ₁₄ -A ₁₇

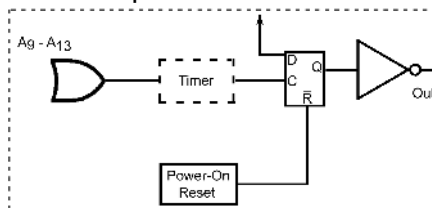
Note 1: Y₉-Y₁₃ Open Drain Outputs with 1.4 kΩ pull-ups

Note 2: B₁-B₈ Open Drain Outputs with 1.4 kΩ pull-ups

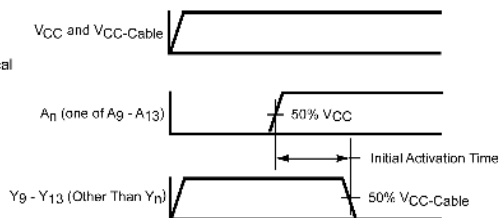
Logic Diagrams



Input Detection Circuit

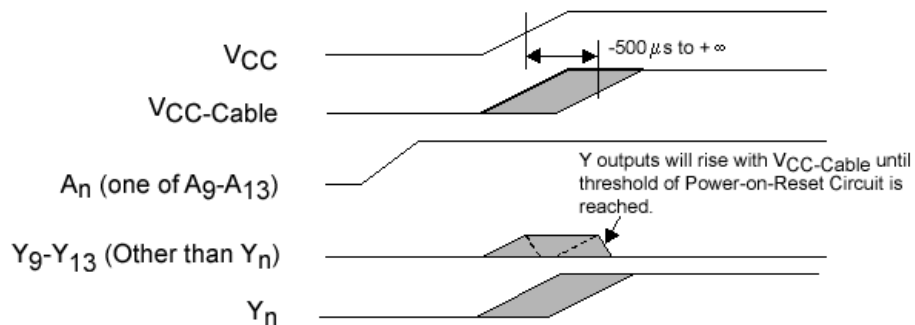


VCC = 3.3V
 VCC-Cable = 5V
 TA = 25° C
 Initial Activation Time = 140ns typical



An (One of A9 - A13) is Switched as Shown Above and Other Four Inputs are Forced at Low State

FIGURE 1. Input Detection Circuit Timing



With 74LVXZ161284B any of the A₉ - A₁₃ inputs may transition HIGH prior to V_{CC} and V_{CC-Cable} becoming stable. In this case it is critical that V_{CC-Cable} does not ramp earlier than V_{CC}. V_{CC} and V_{CC-Cable} ramping concurrently will result in valid operation of this device. Concurrent ramping is defined as V_{CC} and V_{CC-Cable} having less than a 500 μs delta between them.

FIGURE 2. 74LVXZ161284B Adds Tolerance to Power-On Noise

Absolute Maximum Ratings (Note 3)			Recommended Operating Conditions					
Supply Voltage								
V_{CC}		-0.5V to +4.6V	Supply Voltage	3.0V to 3.6V				
$V_{CC-Cable}$		-0.5V to +7.0V	V_{CC}	3.0V to 5.5V				
$V_{CC-Cable}$ Must Be $\geq V_{CC}$			$V_{CC-Cable}$	0V to V_{CC}				
Input Voltage (V_I)—(Note 4)			DC Input Voltage (V_I)	0V to 5.5V				
A_1-A_{13} , PLH _{IN} , DIR, HD		-0.5V to $V_{CC} + 0.5V$	Open Drain Voltage (V_O)	0V to 5.5V				
B_1-B_8 , $C_{14}-C_{17}$, HLH _{IN}		-0.5V to +5.5V (DC)	Operating Temperature (T_A)	-40°C to +85°C				
B_1-B_8 , $C_{14}-C_{17}$, HLH _{IN}		-2.0V to +7.0V*						
		*40 ns Transient						
Output Voltage (V_O)								
A_1-A_8 , $A_{14}-A_{17}$, HLH		-0.5V to $V_{CC} + 0.5V$						
B_1-B_8 , Y_9-Y_{13} , PLH		-0.5V to +5.5V (DC)						
B_1-B_8 , Y_9-Y_{13} , PLH		-2.0V to +7.0V*						
		*40 ns Transient						
DC Output Current (I_O)								
A_1-A_8 , HLH		± 25 mA						
B_1-B_8 , Y_9-Y_{13}		± 50 mA						
PLH (Output LOW)		84 mA						
PLH (Output HIGH)		-50 mA						
Input Diode Current (I_{IK})—(Note 4)								
DIR, HD, A_9-A_{13} , PLH, HLH, $C_{14}-C_{17}$		-20 mA						
Output Diode Current (I_{OK})								
A_1-A_8 , $A_{14}-A_{17}$, HLH		± 50 mA						
B_1-B_8 , Y_9-Y_{13} , PLH		-50 mA						
DC Continuous V_{CC} or Ground Current			± 200 mA					
Storage Temperature			-65°C to +150°C					
ESD								
Human Body Model		4000V	Note 3: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Fairchild does not recommend operation outside the databook specifications.					
Machine Model		200V	Note 4: Either voltage limit or current limit is sufficient to protect inputs.					
Charged Device Model		2000V						
DC Electrical Characteristics								
Symbol	Parameter	V_{CC} (V)	$V_{CC-Cable}$ (V)	$T_A = 0^\circ\text{C}$	$T_A = -40^\circ\text{C}$	Units	Conditions	
				to +70°C	to +85°C			
Guaranteed Limits								
V_{IK}	Input Clamp Diode Voltage	3.0	3.0	-1.2	-1.2	V	$I_i = -18$ mA	
V_{IH}	Minimum HIGH Level	$A_n, B_n, PLH_{IN}, DIR, HD$	3.0 to 3.6	3.0 to 5.5	2.0	2.0	V	
	Input Voltage	C_n	3.0 to 3.6	3.0 to 5.5	2.3	2.3		
		HLH _{IN}	3.0 to 3.6	3.0 to 5.5	2.6	2.6		
V_{IL}	Maximum LOW Level	$A_n, B_n, PLH_{IN}, DIR, HD$	3.0 to 3.6	3.0 to 5.5	0.8	0.8	V	
	Input Voltage	C_n	3.0 to 3.6	3.0 to 5.5	0.8	0.8		
		HLH _{IN}	3.0 to 3.6	3.0 to 5.5	1.6	1.6		
ΔV_T	Minimum Input Hysteresis	$A_n, B_n, PLH_{IN}, DIR, HD$	3.3	5.0	0.4	0.4	V	$V_T^+ - V_T^-$
		C_n	3.3	5.0	0.8	0.8		$V_T^+ - V_T^-$
		HLH _{IN}	3.3	5.0	0.2	0.2		$V_T^+ - V_T^-$
V_{OH}	Minimum HIGH Level Output Voltage	A_n, HLH	3.0	3.0	2.8	2.8	V	$I_{OH} = -50$ μ A
			3.0	3.0	2.4	2.4		$I_{OH} = -4$ mA
		B_n, Y_n	3.0	3.0	2.0	2.0		$I_{OH} = -14$ mA
		B_n, Y_n	3.0	4.5	2.23	2.23		$I_{OH} = -14$ mA
		PLH	3.15	3.15	3.1	3.1		$I_{OH} = -500$ μ A

DC Electrical Characteristics (Continued)									
Symbol	Parameter		V _{CC} (V)	V _{CC—Cable} (V)	T _A = 0°C	T _A = -40°C	Units	Conditions	
					to +70°C	to +85°C			
Guaranteed Limits									
V _{OL}	Maximum LOW Level Output Voltage	A _n , HLH	3.0	3.0	0.2	0.2	V	I _{OL} = 50 μA	
			3.0	3.0	0.4	0.4		I _{OL} = 4 mA	
		B _n , Y _n	3.0	3.0	0.8	0.8		I _{OL} = 14 mA	
		B _n , Y _n	3.0	4.5	0.77	0.77		I _{OL} = 14 mA	
		PLH	3.0	3.0	0.85	0.95		I _{OL} = 84 mA	
		PLH	3.0	4.5	0.8	0.9		I _{OL} = 84 mA	
R _D	Maximum Output Impedance	B ₁ - B ₈ , Y ₉ - Y ₁₃	3.3	3.3	60	60	Ω	(Note 5)(Note 7)	
			3.3	5.0	55	55			
	Minimum Output Impedance	B ₁ - B ₈ , Y ₉ - Y ₁₃	3.3	3.3	30	30		(Note 5)(Note 7)	
			3.3	5.0	35	35			
R _P	Maximum Pull-Up Resistance	B ₁ - B ₈ , Y ₉ - Y ₁₃ , C ₁₄ - C ₁₇	3.3	3.3	1650	1650	Ω		
			3.3	5.0	1650	1650			
	Minimum Pull-Up Resistance	B ₁ - B ₈ , Y ₉ - Y ₁₃ , C ₁₄ - C ₁₇	3.3	3.3	1150	1150	Ω		
			3.3	5.0	1150	1150			
I _{IH}	Maximum Input Current in HIGH State	A ₉ - A ₁₃ , PLH _{IN} , HD, DIR, HLH _{IN}	3.6	3.6	1.0	1.0	μA	V _I = 3.6V	
		C ₁₄ - C ₁₇	3.6	3.6	50.0	50.0		V _I = 3.6V	
		C ₁₄ - C ₁₇	3.6	5.5	100	100		V _I = 5.5V	
I _{IL}	Maximum Input Current in LOW State	A ₉ - A ₁₃ , PLH _{IN} , HD, DIR, HLH _{IN}	3.6	3.6	-1.0	-1.0	μA	V _I = 0.0V	
		C ₁₄ - C ₁₇	3.6	3.6	-3.5	-3.5		mA	V _I = 0.0V
		C ₁₄ - C ₁₇	3.6	5.5	-5.0	-5.0			
I _{OZH}	Maximum Output Disable Current (HIGH)	A ₁ - A ₈	3.6	3.6	20	20	μA	V _O = 3.6V	
		B ₁ - B ₈	3.6	3.6	50	50		V _O = 3.6V	
		B ₁ - B ₈	3.6	5.5	100	100		V _O = 5.5V	
I _{OZL}	Maximum Output Disable Current (LOW)	A ₁ - A ₈	3.6	3.6	-20	-20	μA	V _O = 0.0V	
		B ₁ - B ₈	3.6	3.6	-3.5	-3.5			
		B ₁ - B ₈	3.6	5.5	-5.0	-5.0			
I _{OZPU}	Maximum Power-Up Disable Current	Y ₉ - Y ₁₃	0 to 1.5	0 to 1.5	350	350	μA	V _O = 5.5V	
		B ₁ - B ₈	(Note 8)	(Note 8)	-5	-5		mA	V _O = 0.0V
I _{OZPD}	Maximum Power-Down Disable Current	Y ₉ - Y ₁₃	0 to 1.5	0 to 1.5	350	350	μA	V _O = 5.5V	
		B ₁ - B ₈	(Note 8)	(Note 8)	-5	-5		mA	V _O = 0.0V
I _{OFF}	Power Down Output Leakage	B ₁ - B ₈ , Y ₉ - Y ₁₃ , PLH	0.0	0.0	100	100	μA	V _O = 5.5V	
I _{OFF}	Power Down Input Leakage	C ₁₄ -C ₁₇ , HLH _{IN}	0.0	0.0	100	100	μA	V _I = 5.5V	
I _{OFF—ICC}	Power Down Leakage to V _{CC}		0.0	0.0	250	250	μA	(Note 6)	
I _{OFF—ICC2}	Power Down Leakage to V _{CC—Cable}		0.0	0.0	250	250	μA	(Note 6)	
I _{CC}	Maximum Supply Current		3.6	3.6	45	45	mA	V _I = V _{CC} or GND	
			3.6	5.5	70	70		V _I = V _{CC} or GND	

Note 5: Output impedance is measured with the output active LOW and active HIGH (HD = HIGH).

Note 6: Power-down leakage to V_{CC} or V_{CC—Cable} is tested by simultaneously forcing all pins on the cable-side (B₁-B₈, Y₉-Y₁₃, PLH, C₁₄-C₁₇ and HLH_{IN}) to 5.5V and measuring the resulting I_{CC} or I_{CC—Cable}.

Note 7: This parameter is guaranteed but not tested, characterized only.

Note 8: Connect all V_{CC} pins and V_{CC—Cable} pins when forcing voltage applied, DIR = HD = 0V.

AC Electrical Characteristics							
Symbol	Parameter	$T_A = 0^\circ\text{C to } +70^\circ\text{C}$		$T_A = -40^\circ\text{C to } +85^\circ\text{C}$		Units	Figure Number
		$V_{CC} = 3.0\text{V} - 3.6\text{V}$		$V_{CC} = 3.0\text{V} - 3.6\text{V}$			
		$V_{CC-Cable} = 3.0\text{V} - 5.5\text{V}$		$V_{CC-Cable} = 3.0\text{V} - 5.5\text{V}$			
		Min	Max	Min	Max		
t_{PHL}	A_1-A_8 to B_1-B_8	2.0	40.0	2.0	44.0	ns	Figure 3
t_{PLH}	A_1-A_8 to B_1-B_8	2.0	40.0	2.0	44.0	ns	Figure 4
t_{PHL}	B_1-B_8 to A_1-A_8	2.0	40.0	2.0	44.0	ns	Figure 5
t_{PLH}	B_1-B_8 to A_1-A_8	2.0	40.0	2.0	44.0	ns	Figure 5
t_{PHL}	A_9-A_{13} to Y_9-Y_{13}	2.0	40.0	2.0	44.0	ns	Figure 3
t_{PLH}	A_9-A_{13} to Y_9-Y_{13}	2.0	40.0	2.0	44.0	ns	Figure 4
t_{PHL}	$C_{14}-C_{17}$ to $A_{14}-A_{17}$	2.0	40.0	2.0	44.0	ns	Figure 5
t_{PLH}	$C_{14}-C_{17}$ to $A_{14}-A_{17}$	2.0	40.0	2.0	44.0	ns	Figure 5
t_{SKEW}	LH-LH or HL-HL		10.0		12.0	ns	(Note 10)
t_{PHL}	PLH_{IN} to PLH	2.0	40.0	2.0	44.0	ns	Figure 3
t_{PLH}	PLH_{IN} to PLH	2.0	40.0	2.0	44.0	ns	Figure 4
t_{PHL}	HLH_{IN} to HLH	2.0	40.0	2.0	44.0	ns	Figure 5
t_{PLH}	HLH_{IN} to HLH	2.0	40.0	2.0	44.0	ns	Figure 5
t_{PHZ}	Output Disable Time	2.0	15.0	2.0	18.0	ns	Figure 9
t_{PLZ}	DIR to A_1-A_8	2.0	15.0	2.0	18.0	ns	Figure 9
t_{PZH}	Output Enable Time	2.0	50.0	2.0	50.0	ns	Figure 10
t_{PZL}	DIR to A_1-A_8	2.0	50.0	2.0	50.0	ns	Figure 10
t_{PHZ}	Output Disable Time	2.0	50.0	2.0	50.0	ns	Figure 11
t_{PLZ}	DIR to B_1-B_8	2.0	50.0	2.0	50.0	ns	Figure 11
t_{PEN}	Output Enable Time	2.0	25.0	2.0	28.0	ns	Figure 4
	HD to B_1-B_8 , Y_9-Y_{13}	2.0	25.0	2.0	28.0	ns	Figure 4
t_{pDIS}	Output Disable Time	2.0	25.0	2.0	28.0	ns	Figure 4
	HD to B_1-B_8 , Y_9-Y_{13}	2.0	25.0	2.0	28.0	ns	Figure 4
$t_{PEN} - t_{pDIS}$	Output Enable- Output Disable		10.0		12.0	ns	
t_{SLEW}	Output Slew Rate					V/ns	
t_{PLH}	B_1-B_8 , Y_9-Y_{13}	0.05	0.40	0.05	0.40	V/ns	Figure 7
t_{PHL}		0.05	0.40	0.05	0.40	V/ns	Figure 6
t_r, t_f	t_{RISE} and t_{FALL} B_1-B_8 (Note 9), Y_9-Y_{13} (Note 9)		120		120	ns	Figure 8 (Note 11)
			120		120	ns	

Note 9: Open Drain

Note 10: t_{SKEW} is measured for common edge output transitions and compares the measured propagation delay for a given path type:

- (i) A_1-A_8 to B_1-B_8 , A_9-A_{13} to Y_9-Y_{13}
- (ii) B_1-B_8 to A_1-A_8
- (iii) $C_{14}-C_{17}$ to $A_{14}-A_{17}$

Note 11: This parameter is guaranteed but not tested, characterized only.

Capacitance

Symbol	Parameter	Typ	Units	Conditions
C_{IN}	Input Capacitance	3	pF	$V_{CC} = 0.0\text{V}$ (HD, DIR, A_9-A_{13} , $C_{14}-C_{17}$, PLH_{IN} and HLH_{IN})
C_{IO} (Note 12)	I/O Pin Capacitance	5	pF	$V_{CC} = 3.3\text{V}$

Note 12: C_{IO} is measured at frequency = 1 MHz, per MIL-STD-883B, Method 3012

AC Loading and Waveforms

Pulse Generator for all pulses: Rate ≤ 1.0 MHz; $Z_O \leq 50\Omega$; $t_f \leq 2.5$ ns, $t_r \leq 2.5$ ns.

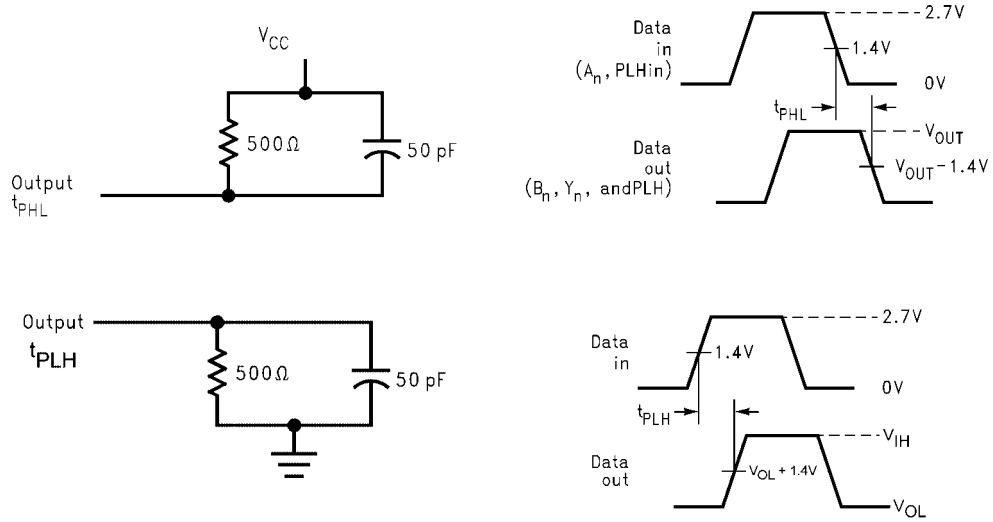


FIGURE 3. Port A to B and A to Y Propagation Delay Waveforms

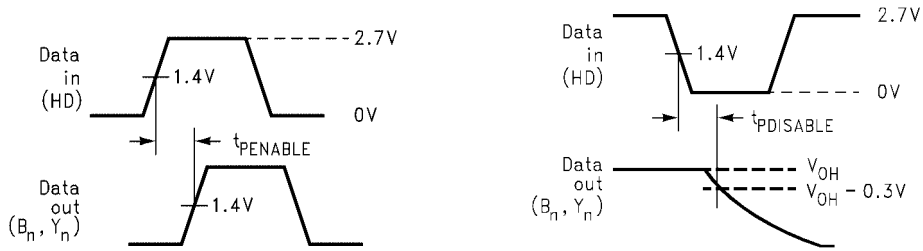


FIGURE 4. Port A to B and A to Y Output Waveforms

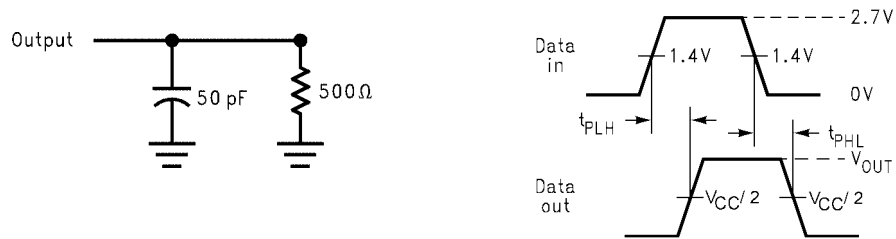


FIGURE 5. Port B to A, C to A and HLH_{in} to HLH Propagation Delay Waveforms

AC Loading and Waveforms (Continued)

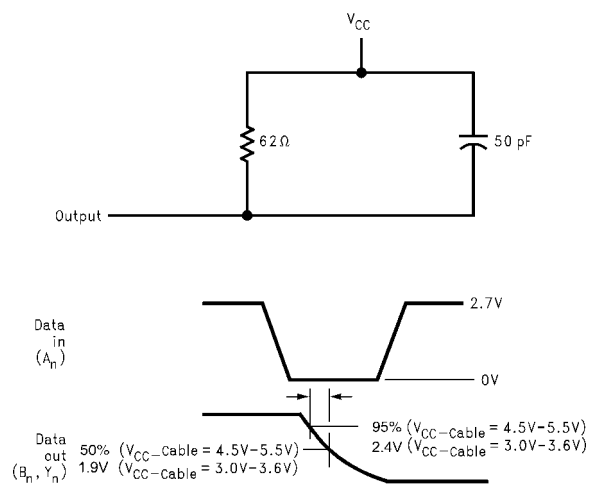


FIGURE 6. Port A to B and A to Y HL Slew Test Load and Waveforms

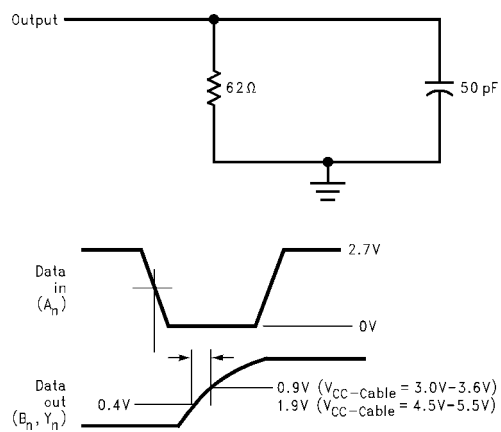
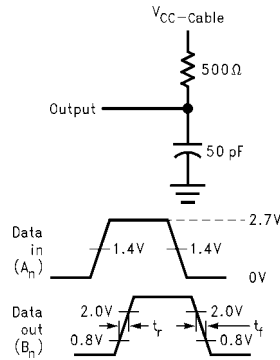


FIGURE 7. Port A to B and A to Y LH Slew Test Load and Waveforms

AC Loading and Waveforms (Continued)



t_r = Output Rise Time, Open Drain
 t_f = Output Fall Time, Open Drain

FIGURE 8. Ports A to B and A to Y Rise and Fall Test Load and Waveforms for Open Drain Outputs

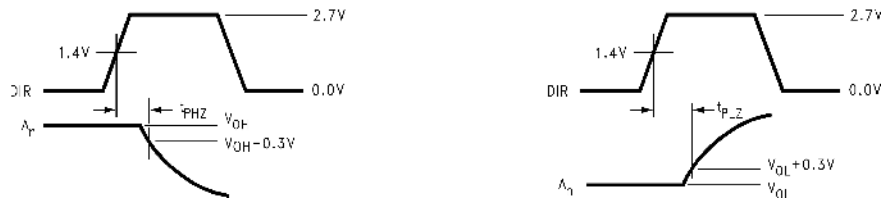
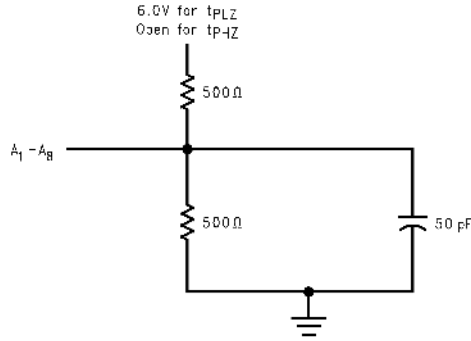


FIGURE 9. t_{PHZ} and t_{PLZ} Test Load and Waveforms, DIR to A_1-A_8

AC Loading and Waveforms (Continued)

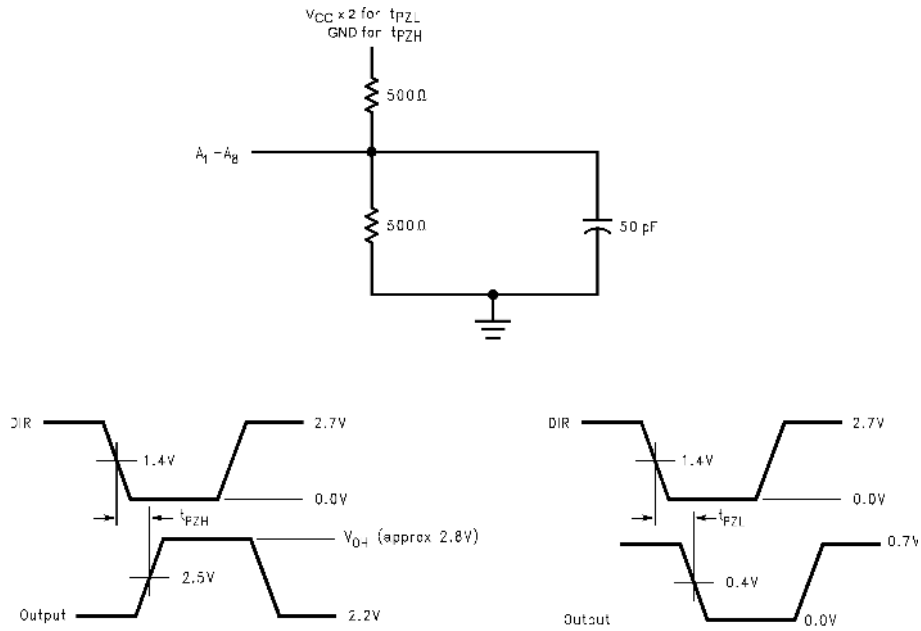


FIGURE 10. t_{PZH} and t_{PZL} Test Load and Waveforms, DIR to A₁-A₈

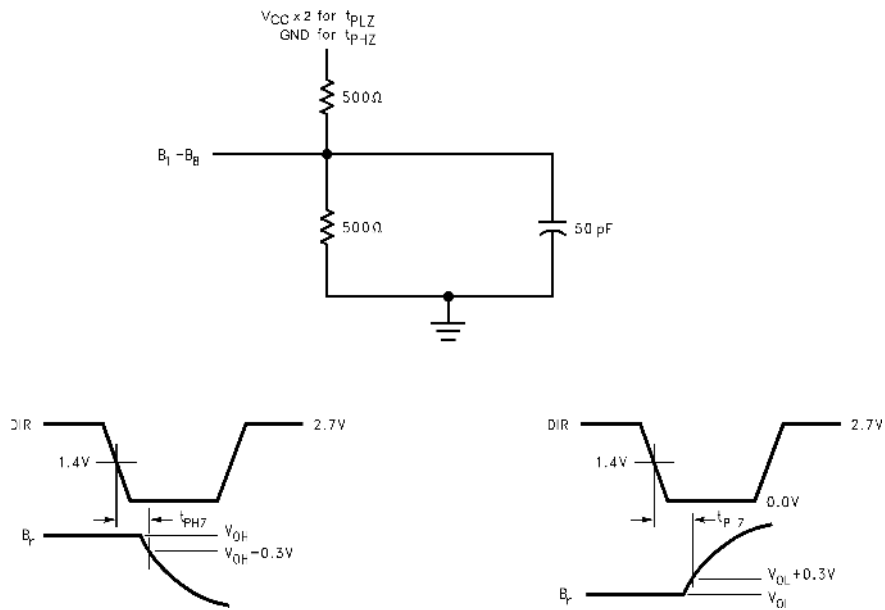
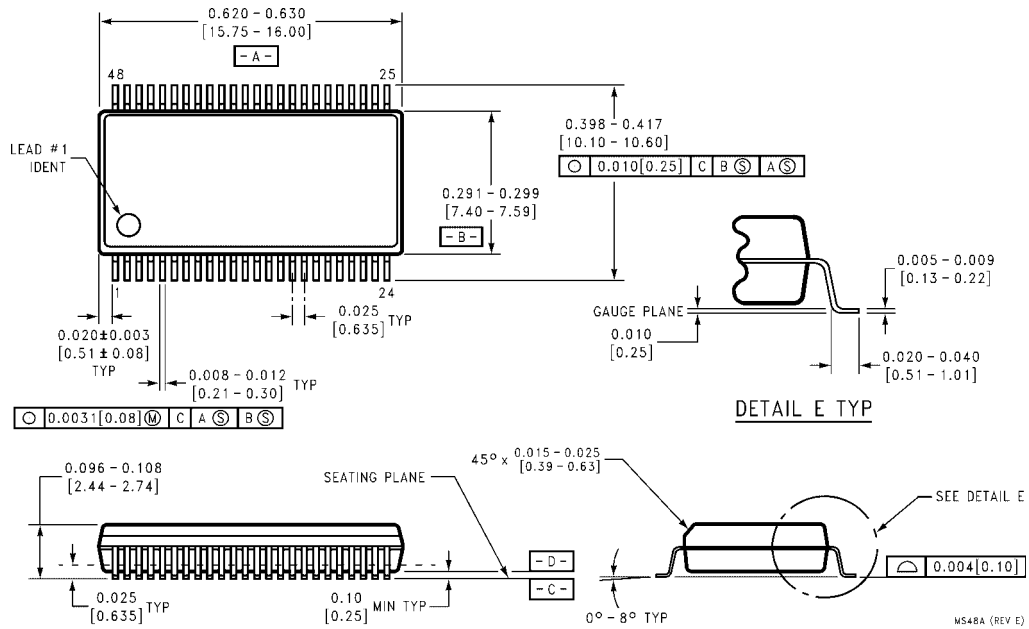


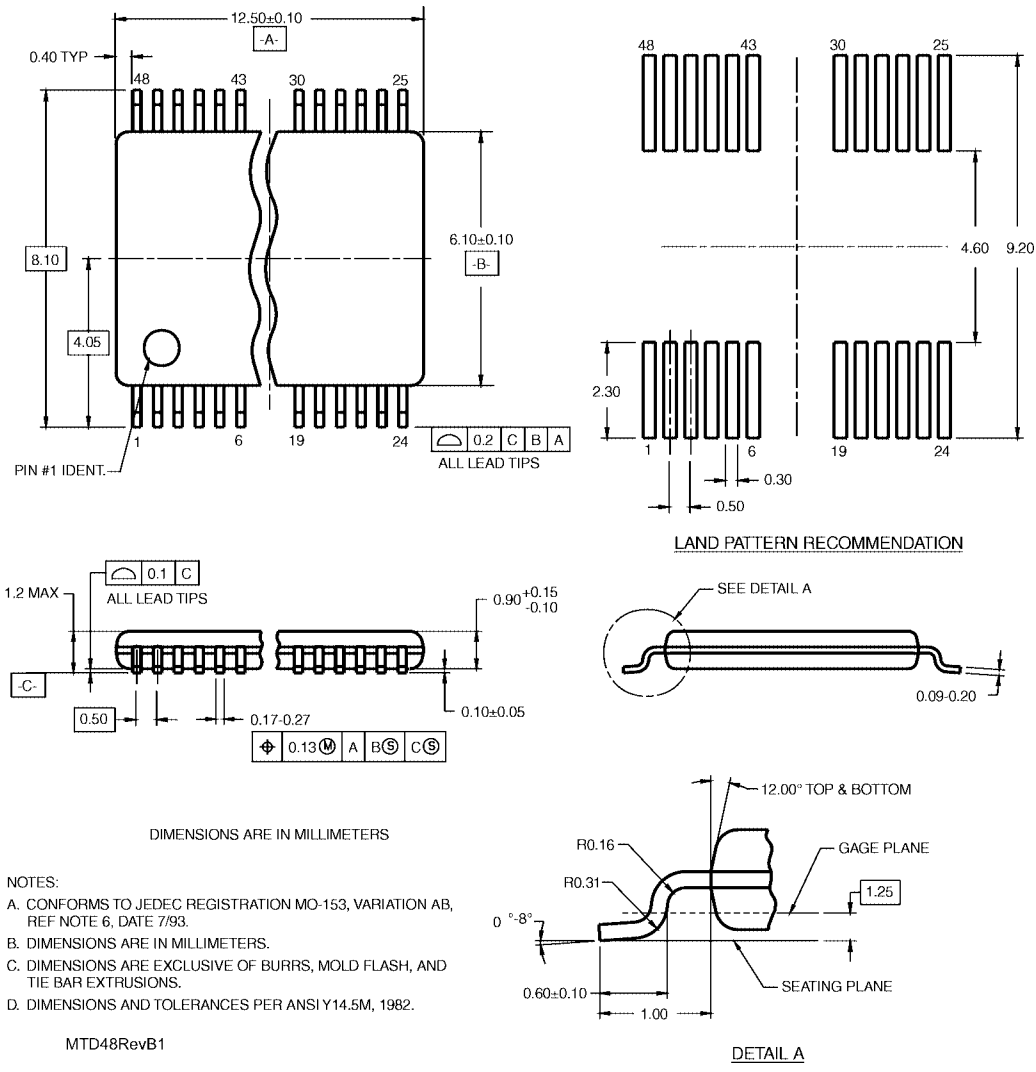
FIGURE 11. t_{PHZ} and t_{PLZ} Test Load and Waveforms DIR to B₁-B₈

Physical Dimensions inches (millimeters) unless otherwise noted



**48-Lead Small Shrink Outline Package (SSOP), JEDEC MO-118, 0.300" Wide
Package Number MS48A**

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



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