National Semiconductor

July 6, 2011

LMH6733

Single Supply, 1.0 GHz, Triple Operational Amplifier

General Description

The LMH6733 is a triple, wideband, operational amplifier designed specifically for use where high speed and low power are required. Input voltage range and output voltage swing are optimized for operation on supplies as low as 3V and up to ±6V. Benefiting from National's current feedback architecture, the LMH6733 offers a gain range of ±1 to ±10 while providing stable operation without external compensation, even at unity gain. These amplifiers provide 650 MHz small signal bandwidth at a gain of 2 V/V , a low 2.1 $\mathrm{nV}/\sqrt{\mathrm{Hz}}$ input referred noise and only consume 5.5 mA (per amplifier) from a single 5V supply.

The LMH6733 is offered in a 16-Pin SSOP package with flow through pinout for ease of layout and is also pin compatible with the LMH6738. Each amplifier has an individual shutdown pin.

Features

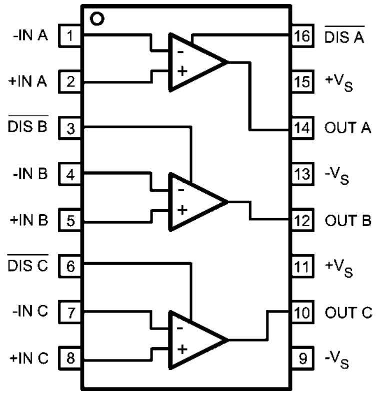
- Supply range 3 to 12V single supply
- Supply range ±1.5V to ±6V split supply
- 1.0 GHz −3 dB small signal bandwidth ($A_V = +1$, $V_S = \pm5V$)
- 650 MHz −3 dB small signal bandwidth ($A_V = +2$, $V_S = 5V$)
- Low supply current (5.5 mA per op amp, $V_S = 5V$)
- 2.1 $\mathrm{nV}/\sqrt{\mathrm{Hz}}$ input noise voltage
- 3750 V/μs slew rate
- 70 mA linear output current
- CMIR and output swing to 1V from each supply rail

Applications

- HDTV component video driver
- High resolution projectors
- Flash A/D driver
- D/A transimpedance buffer
- Wide dynamic range IF amp
- Radar/communication receivers
- DDS post-amps
- Wideband inverting summer
- Line driver

Connection Diagram

16-Pin SSOP



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Top View

Ordering Information

Package	Part Number	Package Marking	Transport Media	NSC Drawing
16-pin SSOP	LMH6733MQ	LH6733MQ	95 Units/Rail	MQA16
	LMH6733MQX		2.5k Units Tape and Reel	

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Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

ESD Tolerance (Note 2)	
Human Body Model	2000V
Machine Model	200V
Supply Voltage ($V^+ - V^-$)	13.2V
I_{OUT}	(Note 3)
Common Mode Input Voltage	$\pm V_{CC}$
Maximum Junction Temperature	+150°C
Storage Temperature Range	−65°C to +150°C
Soldering Information	
Infrared or Convection (20 sec.)	235°C
Wave Soldering (10 sec.)	260°C
Storage Temperature Range	−65°C to +150°C

Operating Ratings (Note 1)

Thermal Resistance			
Package	**(θ_{JC})**		**(θ_{JA})**
16-Pin SSOP	36°C/W		120°C/W
Temperature Range (Note 4)	−40°C		+85°C
Supply Voltage ($V^+ - V^-$)	3V	to	12V

5V Electrical Characteristics (Note 5)

$A_V = +2$, $V_{CC} = 5V$, $R_L = 100\Omega$, $R_F = 340\Omega$; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Frequency Domain Performance						
UGBW	−3 dB Bandwidth	Unity Gain, $V_{OUT} = 200\ mV_{PP}$		870		MHz
SSBW	−3 dB Bandwidth	$V_{OUT} = 200\ mV_{PP}$, $R_L = 100\Omega$		650		MHz
SSBW		$V_{OUT} = 200\ mV_{PP}$, $R_L = 150\Omega$		685		
LSBW		$V_{OUT} = 2\ V_{PP}$		480		
0.1 dB BW	0.1 dB Gain Flatness	$V_{OUT} = 200\ mV_{PP}$		320		MHz
Time Domain Response						
TRS	Rise and Fall Time (10% to 90%)	2V Step		0.8		ns
SR	Slew Rate	2V Step		1900		V/μs
t_s	Settling Time to 0.1%	2V Step		10		ns
t_e	Enable Time	From $\overline{\text{Disable}}$ = Rising Edge		10		ns
t_d	Disable Time	From $\overline{\text{Disable}}$ = Falling Edge		15		ns
Distortion						
HD2L	2nd Harmonic Distortion	$2\ V_{PP}$, 10 MHz		−63		dBc
HD3L	3rd Harmonic Distortion	$2\ V_{PP}$, 10 MHz		−73		dBc
Equivalent Input Noise						
V_N	Non-Inverting Voltage	>10 MHz		2.1		$nV/\sqrt{Hz}$
I_{CN}	Inverting Current	>10 MHz		18.6		$pA/\sqrt{Hz}$
N_{CN}	Non-Inverting Current	>10 MHz		26.9		$pA/\sqrt{Hz}$
Video Performance						
DG	Differential Gain	4.43 MHz, $R_L = 150\Omega$		0.03		%
DP	Differential Phase	4.43 MHz, $R_L = 150\Omega$		0.025		deg
Static, DC Performance						
VIO	Input Offset Voltage (Note 7)			0.4	2.0 **2.5**	mV
IBN	Input Bias Current (Note 7)	Non-Inverting	2	16.7	28 **32**	μA
IBI	Input Bias Current (Note 7)	Inverting		1.0	17 **19**	μA
PSRR	Power Supply Rejection Ratio (Note 7)	+PSRR	59 **59**	61		dB
		−PSRR	58 **57**	61		

Symbol	Parameter	Conditions	Min	Typ	Max	Units
CMRR	Common Mode Rejection Ratio (Note 7)		52 **51.5**	54.5		dB
XTLK	Crosstalk	Input Referred, f = 10 MHz, Drive Channels A,C Measure Channel B		–80		dB
I_{CC}	Supply Current (Note 7)	All Three Amps Enabled, No Load		16.7	18	mA
	Supply Current Disabled V^+	$R_L = \infty$		1.54	1.8	mA
	Supply Current Disabled V^-	$R_L = \infty$		0.75	1.8	mA
Miscellaneous Performance						
$R_{IN}+$	Non-Inverting Input Resistance			200		kΩ
$C_{IN}+$	Non-Inverting Input Capacitance			1		pF
$R_{IN}-$	Inverting Input Impedance	Output Impedance of Input Buffer.		27		Ω
R_O	Output Impedance	DC		0.05		Ω
V_O	Output Voltage Range (Note 7)	$R_L = 100\Omega$	1.25-3.75 **1.3-3.7**	1.12-3.88		V
		$R_L = \infty$	1.11-3.89 **1.15-3.85**	1.03-3.97		
CMIR	Common Mode Input Range (Note 7)	CMRR > 40 dB	1.1-3.9 **1.2-3.8**	1.0–4.0		V
I_O	Linear Output Current (Note 3, Note 7)	$V_{IN} = 0V$, $V_{OUT} < \pm42$ mV	±50	±60		mA
I_{SC}	Short Circuit Current (Note 6)	$V_{IN} = 2V$ Output Shorted to Ground		170		mA
I_{IH}	Disable Pin Bias Current High	$\overline{\text{Disable}}$ Pin = V^+		–72		μA
I_{IL}	Disable Pin Bias Current Low	$\overline{\text{Disable}}$ Pin = 0V		–360		μA
V_{DMAX}	Voltage for Disable	$\overline{\text{Disable}}$ Pin $\leq V_{DMAX}$		3.2		V
V_{DMIM}	Voltage for Enable	$\overline{\text{Disable}}$ Pin $\geq V_{DMIN}$		3.6		V

±5V Electrical Characteristics (Note 5)

$A_V = +2$, $V_{CC} = \pm5V$, $R_L = 100\Omega$, $R_F = 383\Omega$; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Frequency Domain Performance						
UGBW	–3 dB Bandwidth	Unity Gain, $V_{OUT} = 200\ mV_{PP}$		1000		MHz
SSBW	–3 dB Bandwidth	$V_{OUT} = 200\ mV_{PP}$, $R_L = 100\Omega$		830		MHz
SSBW		$V_{OUT} = 200\ mV_{PP}$, $R_L = 150\Omega$		950		
LSBW		$V_{OUT} = 2\ V_{PP}$		600		
0.1 dB BW	0.1 dB Gain Flatness	$V_{OUT} = 200\ mV_{PP}$		350		MHz
Time Domain Response						
TRS	Rise and Fall Time (10% to 90%)	2V Step		0.7		ns
TRL		5V Step		0.8		
SR	Slew Rate	4V Step		3750		V/μs
t_s	Settling Time to 0.1%	2V Step		10		ns
t_e	Enable Time	From $\overline{\text{Disable}}$ = Rising Edge		10		ns
t_d	Disable Time	From $\overline{\text{Disable}}$ = Falling Edge		15		ns
Distortion						
HD2L	2nd Harmonic Distortion	$2\ V_{PP}$, 10 MHz		–72		dBc
HD3L	3rd Harmonic Distortion	$2\ V_{PP}$, 10 MHz		–63		dBc
Equivalent Input Noise						
V_N	Non-Inverting Voltage	>10 MHz		2.1		$nV/\sqrt{Hz}$
I_{CN}	Inverting Current	>10 MHz		18.6		$pA/\sqrt{Hz}$

Symbol	Parameter	Conditions	Min	Typ	Max	Units
N_{CN}	Non-Inverting Current	>10 MHz		26.9		$pA/\sqrt{Hz}$
Video Performance						
DG	Differential Gain	4.43 MHz, R_L = 150Ω		0.03		%
DP	Differential Phase	4.43 MHz, R_L = 150Ω		0.03		Deg
Static, DC Performance						
VIO	Input Offset Voltage (Note 7)			0.6	2.2 **2.5**	mV
IBN	Input Bias Current (Note 7)	Non-Inverting	−14 **−19**	3.5	19 **24**	μA
IBI	Input Bias Current (Note 7)	Inverting		5	23 **26**	μA
PSRR	Power Supply Rejection Ratio (Note 7)	+PSRR	59	61.5		dB
		−PSRR	58	61		
CMRR	Common Mode Rejection Ratio (Note 7)		53 **52.5**	55		dB
XTLK	Crosstalk	Input Referred, f = 10 MHz, Drive Channels A,C Measure Channel B		−80		dB
I_{CC}	Supply Current (Note 7)	All Three Amps Enabled, No Load		19.5	20.8 **22.0**	mA
	Supply Current Disabled V^+	$R_L = \infty$		1.54	1.8	mA
	Supply Current Disabled V^-	$R_L = \infty$		0.75	1.8	mA
Miscellaneous Performance						
$R_{IN}+$	Non-Inverting Input Resistance			200		kΩ
$C_{IN}+$	Non-Inverting Input Capacitance			1		pF
$R_{IN}-$	Inverting Input Impedance	Output Impedance of Input Buffer		30		Ω
R_O	Output Impedance	DC		0.05		Ω
V_O	Output Voltage Range (Note 7)	R_L = 100Ω	±3.55 **±3.5**	±3.7		V
		$R_L = \infty$	±3.85	±4.0		
CMIR	Common Mode Input Range (Note 7)	CMRR > 43 dB	±3.9 **±3.8**	±4.0		V
I_O	Linear Output Current (Note 3, Note 7)	V_{IN} = 0V, V_{OUT} < ±42 mV	70	±80		mA
I_{SC}	Short Circuit Current (Note 6)	V_{IN} = 2V Output Shorted to Ground		237		mA
I_{IH}	Disable Pin Bias Current High	$\overline{\text{Disable}}$ Pin = V^+		−72		μA
I_{IL}	Disable Pin Bias Current Low	$\overline{\text{Disable}}$ Pin = 0V		−360		μA
V_{DMAX}	Voltage for Disable	$\overline{\text{Disable}}$ Pin ≤ V_{DMAX}		3.2		V
V_{DMIM}	Voltage for Enable	$\overline{\text{Disable}}$ Pin ≥ V_{DMIN}		3.6		V

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not guaranteed. For guaranteed specifications, see the Electrical Characteristics tables.

Note 2: Human Body Model, applicable std. MIL-STD-883, Method 3015.7. Machine Model, applicable std. JESD22-A115-A (ESD MM std. of JEDEC) Field-Induced Charge-Device Model, applicable std. JESD22-C101-C (ESD FICDM std. of JEDEC).

Note 3: The maximum output current (I_{OUT}) is determined by device power dissipation limitations. See the Power Dissipation section of the Applications Information for more details.

Note 4: The maximum power dissipation is a function of $T_{J(MAX)}$, θ_{JA}. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} - T_A)/\ \theta_{JA}$. All numbers apply for packages soldered directly onto a PC Board.

Note 5: Electrical Table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that $T_J = T_A$. No guarantee of parametric performance is indicated in the electrical tables under conditions of internal self-heating where $T_J > T_A$.

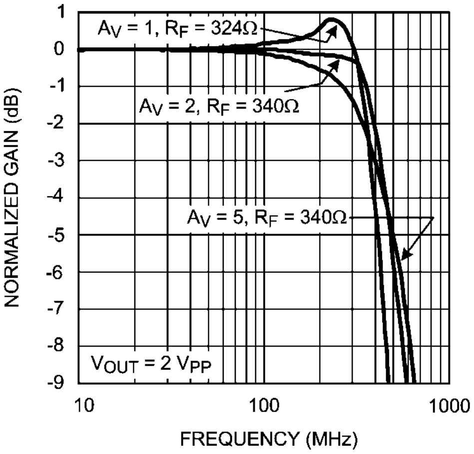
Note 6: Short circuit current should be limited in duration to no more than 10 seconds. See the Power Dissipation section of the Application Section for more details.

Note 7: Parameter 100% production tested at 25° C.

Typical Performance Characteristics

$A_V = +2$, $V_{CC} = 5V$, $R_L = 100\Omega$, $R_F = 340\Omega$; unless otherwise specified).

Large Signal Frequency Response



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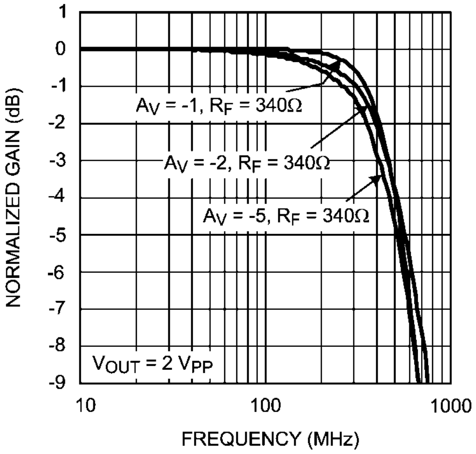
Large Signal Frequency Response



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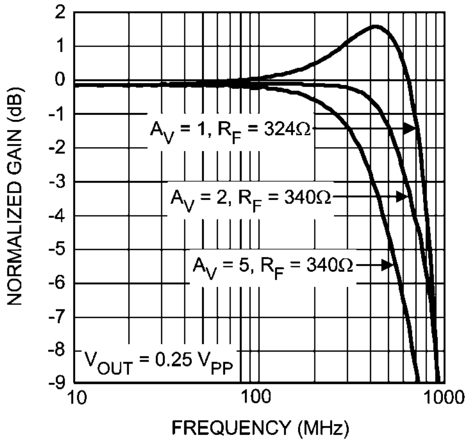
Small Signal Frequency Response



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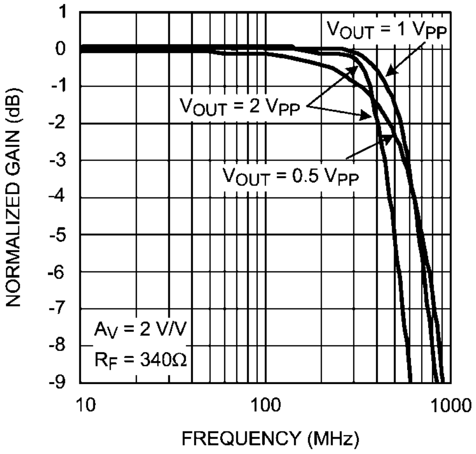
Frequency Response vs. V_{OUT}



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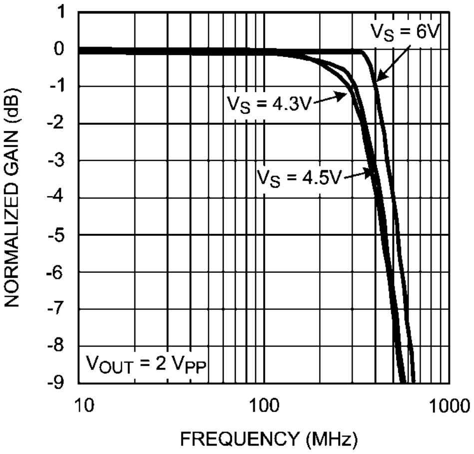
Frequency Response vs. Supply Voltage



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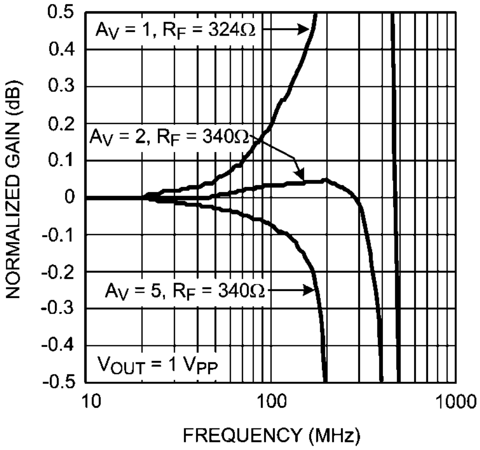
Gain Flatness



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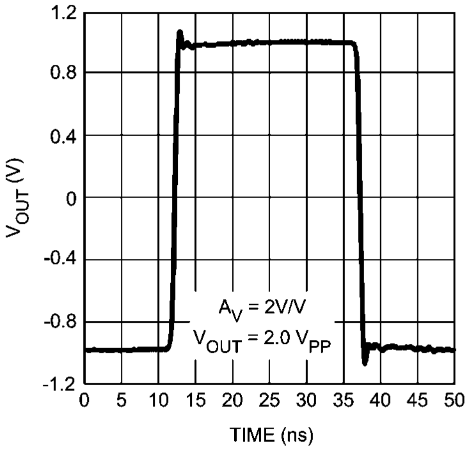
Pulse Response



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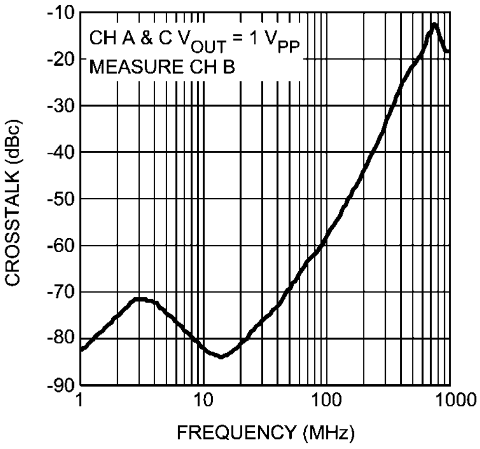
Crosstalk vs. Frequency



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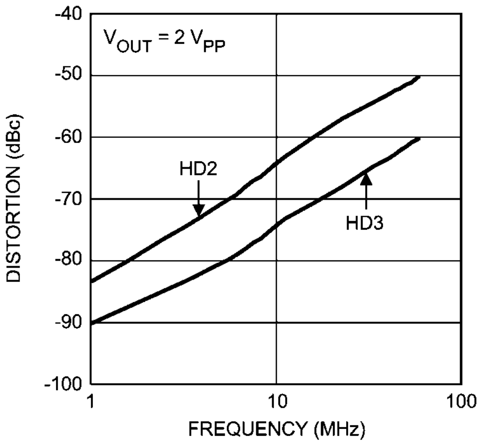
Distortion vs. Frequency



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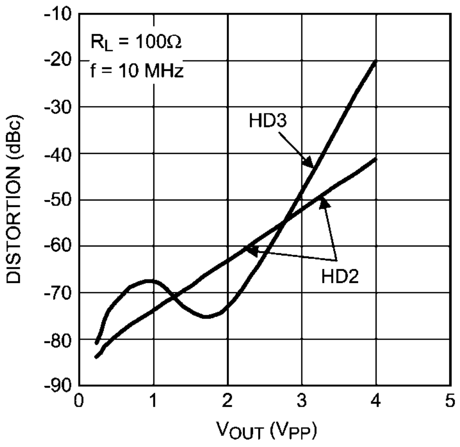
Distortion vs. Output Voltage



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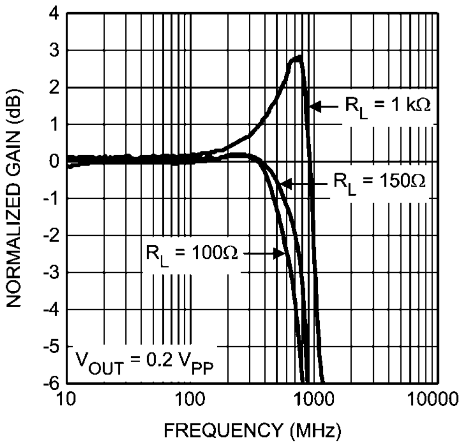
Small Signal Frequency Response vs. R_L



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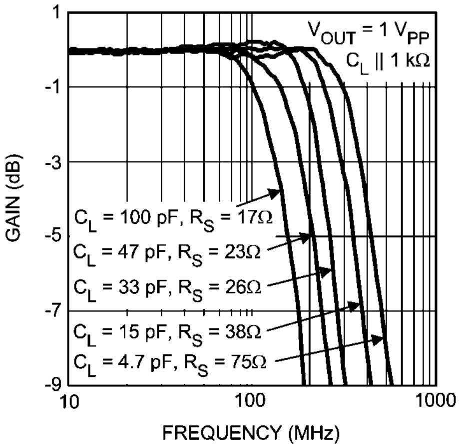
Frequency Response vs. Capacitive Load



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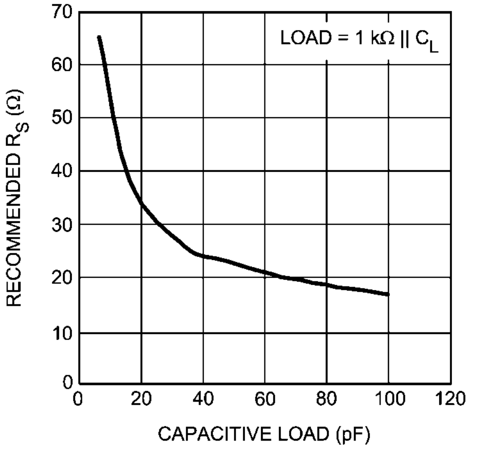
Series Output Resistance vs. Capacitive Load



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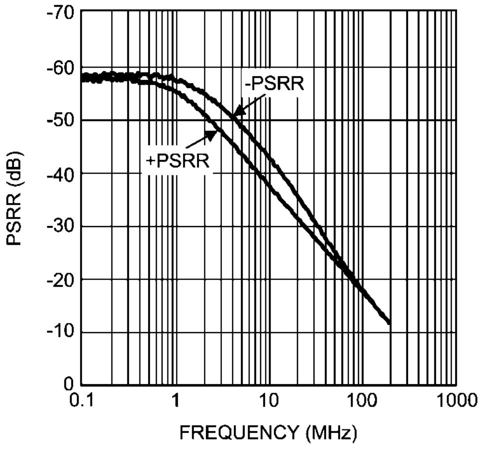
PSRR vs. Frequency



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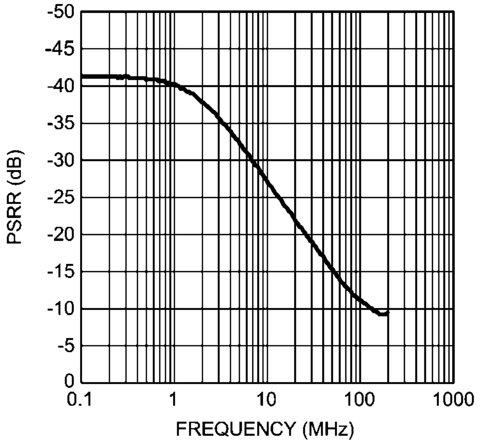
CMRR vs. Frequency



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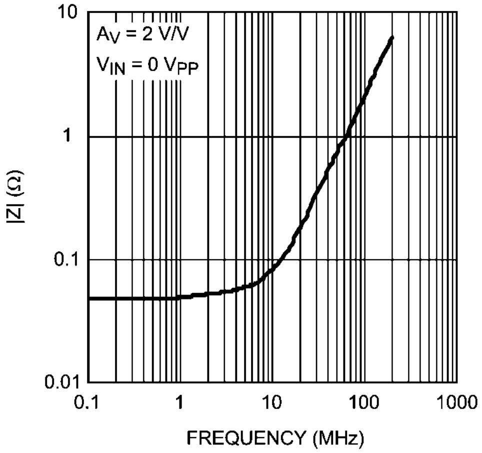
Closed Loop Output Impedance |Z|



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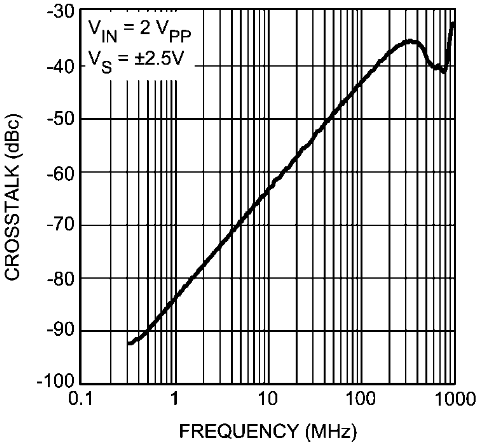
Disabled Channel Isolation vs. Frequency



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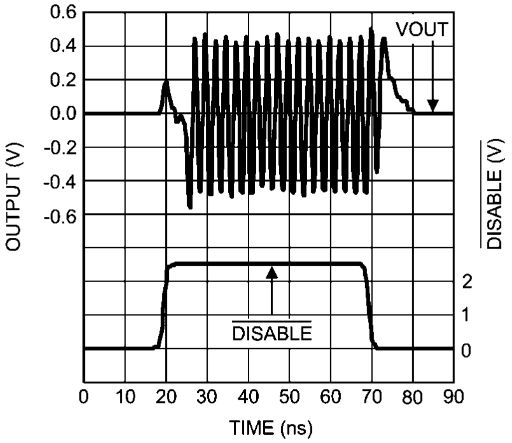
Disable Timing



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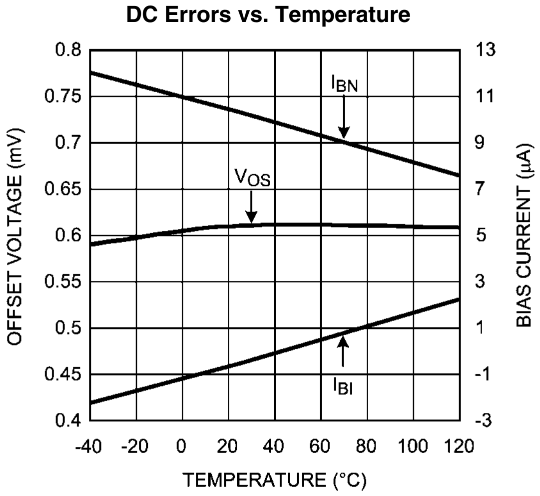

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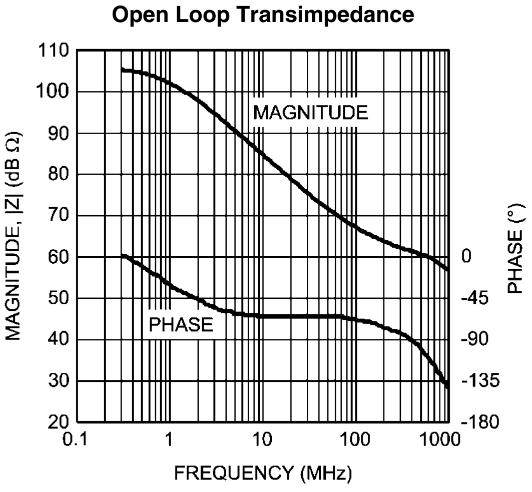

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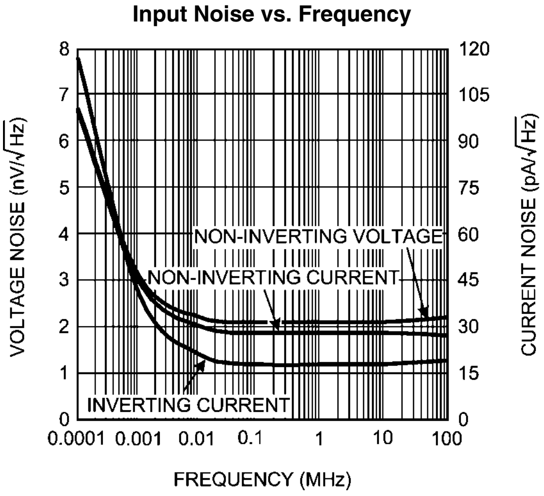

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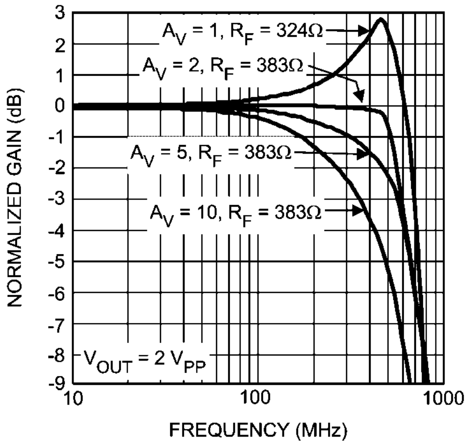
Typical Performance Characteristics

$A_V = +2$, $V_{CC} = \pm5V$, $R_L = 100\Omega$, $R_F = 383\Omega$; unless otherwise specified).

Large Signal Frequency Response



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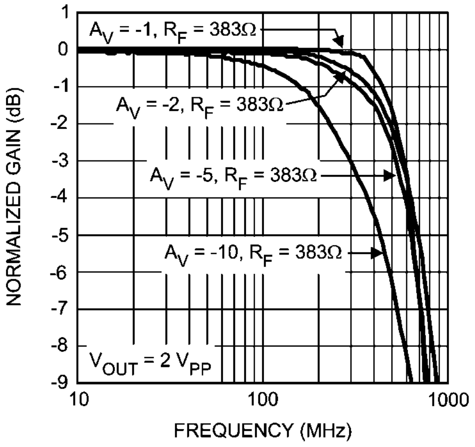
Large Signal Frequency Response



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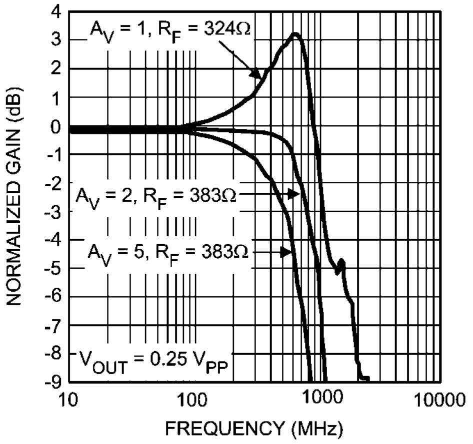
Small Signal Frequency Response



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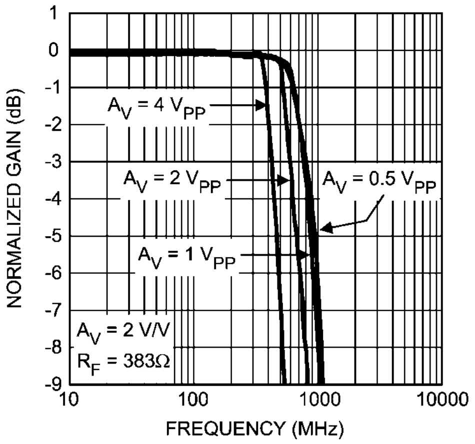
Frequency Response vs. V_{OUT}



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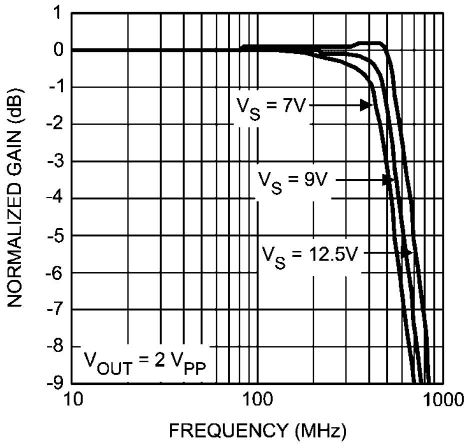
Frequency Response vs. Supply Voltage



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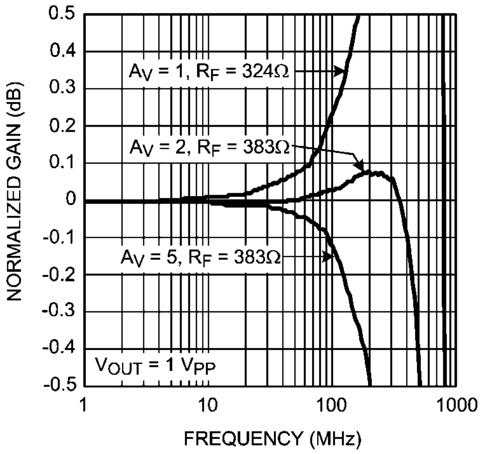
Gain Flatness



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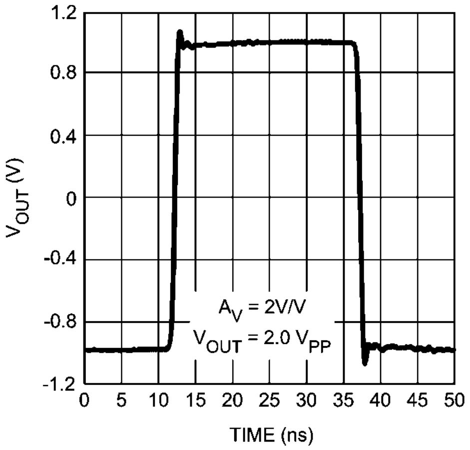
Pulse Response



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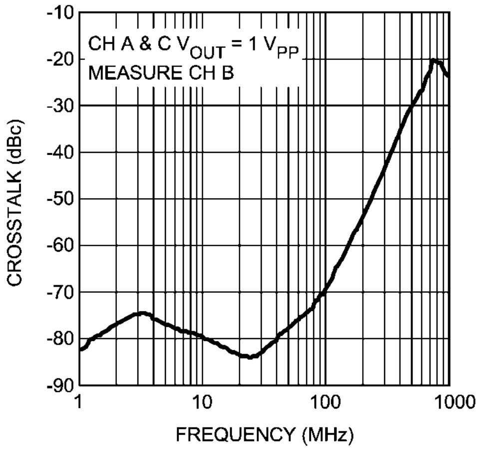
Crosstalk vs. Frequency



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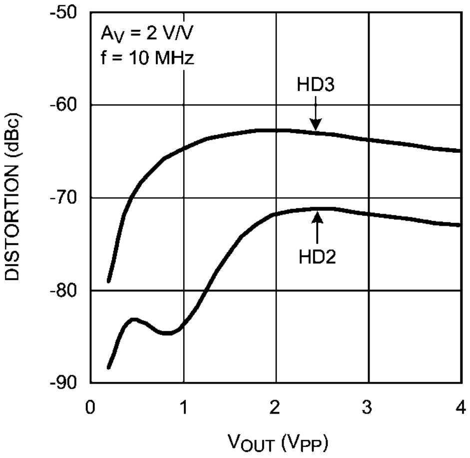
Distortion vs. Output Voltage



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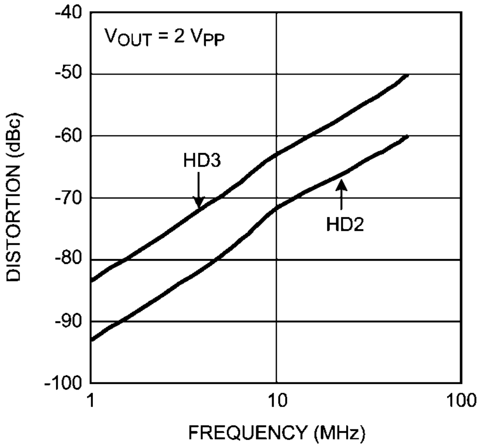
Distortion vs. Frequency



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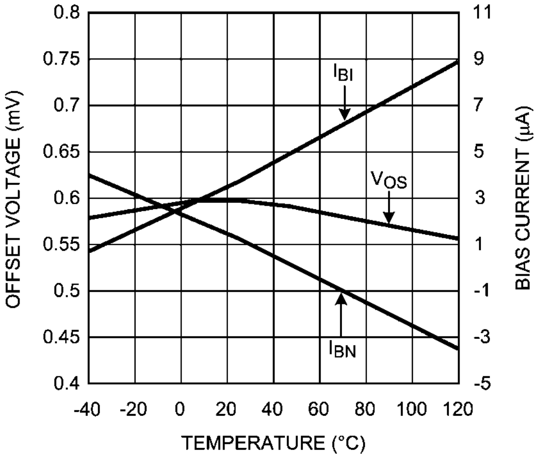
DC Errors vs. Temperature



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Application Information

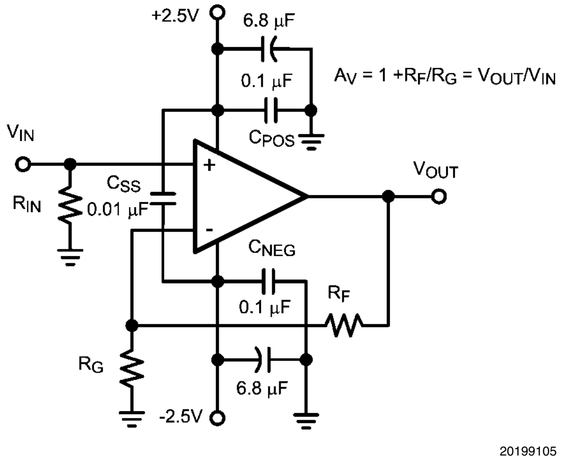

FIGURE 1. Recommended Non-Inverting Gain Circuit

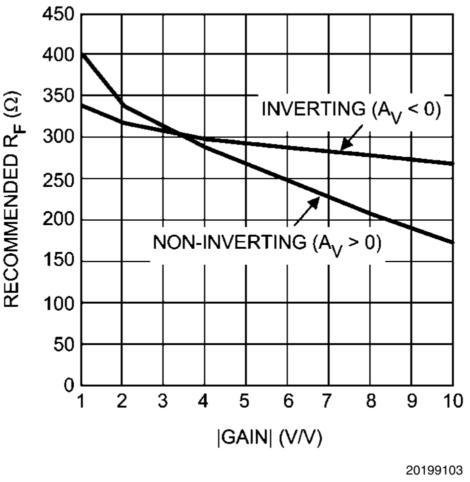

FIGURE 3. Recommended R_F vs. Gain

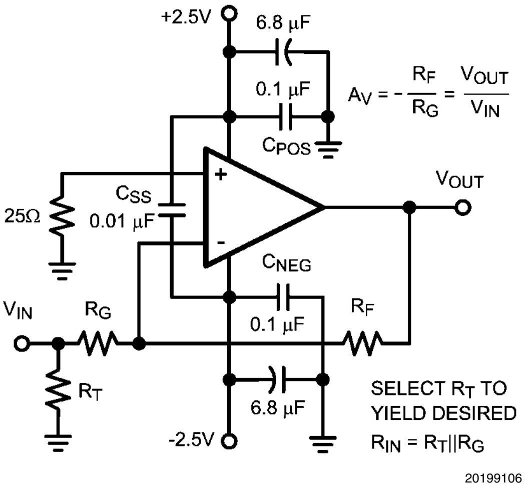

FIGURE 2. Recommended Inverting Gain Circuit

GENERAL INFORMATION

The LMH6733 is a high speed current feedback amplifier, optimized for very high speed and low distortion. The LMH6733 has no internal ground reference so single or split supply configurations are both equally useful.

FEEDBACK RESISTOR SELECTION

One of the key benefits of a current feedback operational amplifier is the ability to maintain optimum frequency response independent of gain by using the appropriate values for the feedback resistor (R_F). The Electrical Characteristics and Typical Performance plots specify an R_F of 340Ω, a gain of +2 V/V and ±2.5V power supplies (unless otherwise specified). Generally, lowering R_F from its recommended value will peak the frequency response and extend the bandwidth while increasing the value of R_F will cause the frequency response to roll off faster. Reducing the value of R_F too far below its recommended value will cause overshoot, ringing and, eventually, oscillation.

See Figure 3 for selecting a feedback resistor value for gains of ±1 to ±10. Since each application is slightly different it is worth some experimentation to find the optimal R_F for a given circuit. In general a value of R_F that produces about 0.1 dB of peaking is the best compromise between stability and maximal bandwidth. Note that it is not possible to use a current feedback amplifier with the output shorted directly to the inverting input. The buffer configuration of the LMH6733 requires a 324Ω feedback resistor for stable operation.

The LMH6733 has been optimized for high speed operation. As shown in Figure 3 the suggested value for R_F decreases for higher gains. Due to the impedance of the input buffer there is a practical limit for how small R_F can go, based on the lowest practical value of R_G. This limitation applies to both inverting and non-inverting configurations. For the LMH6733 the input resistance of the inverting input is approximately 30Ω and 20Ω is a practical (but not hard and fast) lower limit for R_G. The LMH6733 begins to operate in a gain bandwidth limited fashion in the region where R_G is nearly equal to the input buffer impedance. Note that the amplifier will operate with R_G values well below 20Ω, however results may be substantially different than predicted from ideal models. In particular the voltage potential between the inverting and non-inverting inputs cannot be expected to remain small.

Inverting gain applications that require impedance matched inputs may limit gain flexibility somewhat (especially if maximum bandwidth is required). The impedance seen by the source is R_G || R_T (R_T is optional). The value of R_G is R_F /gain. Thus for an inverting gain of −5 V/V and an optimal value for R_F the input impedance is equal to 55Ω. Using a termination resistor this can be brought down to match a 25Ω source; however, a 150Ω source cannot be matched. To match a 150Ω source would require using a 1050Ω feedback resistor and would result in reduced bandwidth.

For more information see Application Note OA-13 which describes the relationship between R_F and closed-loop frequency response for current feedback operational amplifiers. The value for the inverting input impedance for the LMH6733 is approximately 30Ω. The LMH6733 is designed for optimum performance at gains of +1 to +10 V/V and −1 to −9 V/V. Higher gain configurations are still useful; however, the bandwidth will fall as gain is increased, much like a typical voltage feedback amplifier.

ACTIVE FILTER

The choice of reactive components requires much attention when using any current feedback operational amplifier as an active filter. Reducing the feedback impedance, especially at higher frequencies, will almost certainly cause stability problems. Likewise capacitance on the inverting input should be avoided. See Application Notes OA-7 and OA-26 for more information on Active Filter applications for Current Feedback Op Amps.

When using the LMH6733 as a low pass filter the value of R_F can be substantially reduced from the value recommended in the R_F vs. Gain charts. The benefit of reducing R_F is increased gain at higher frequencies, which improves attenuation in the stop band. Stability problems are avoided because in the stop band additional device bandwidth is used to cancel the input signal rather than amplify it. The benefit of this change depends on the particulars of the circuit design. With a high pass filter configuration reducing R_F will likely result in device instability and is not recommended.

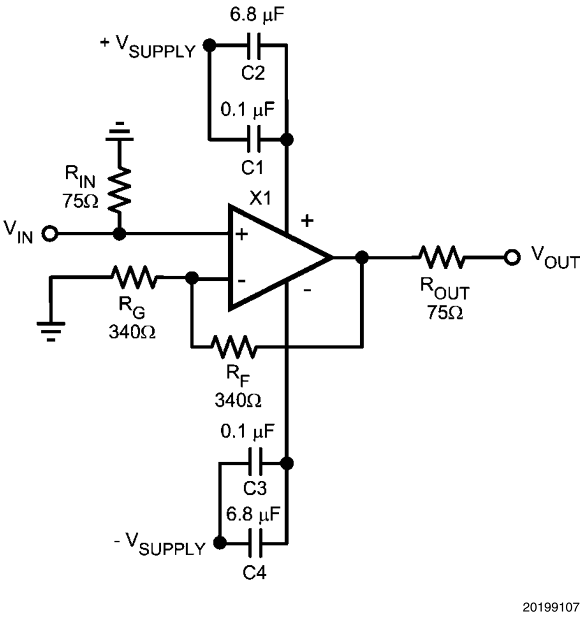

FIGURE 4. Typical Video Application

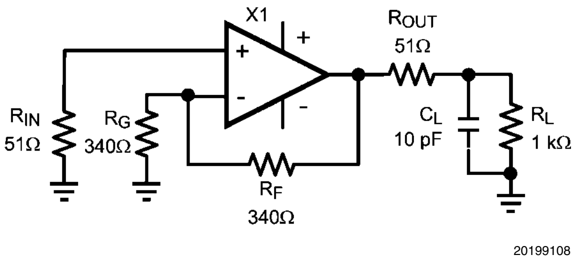

FIGURE 5. Decoupling Capacitive Loads

DRIVING CAPACITIVE LOADS

Capacitive output loading applications will benefit from the use of a series output resistor R_{OUT}. shows the use of a series output resistor, R_{OUT}, to stabilize the amplifier output under capacitive loading. Capacitive loads of 5 to 120 pF are the most critical, causing ringing, frequency response peaking and possible oscillation. The chart “Frequency Response vs. Capacitive Load” give a recommended value for selecting a series output resistor for mitigating capacitive loads. The values suggested in the charts are selected for .5 dB or less of peaking in the frequency response. This gives a good compromise between settling time and bandwidth. For applications where maximum frequency response is needed and some peaking is tolerable, the value of R_{OUT} can be reduced slightly from the recommended values.

CAT5 HIGH DEFINITION VIDEO TRANSMISSION

The LMH6733 can be used to send component 1080i High Definition (HD) video over CAT5 twisted-pairs. As shown Figure 6 , the LMH6733 can be utilized to perform all three video transmitter, video receiver, and equalization circuitry. The equalization circuitry enhances the video signal to accomodate for the CAT5 attenuation over various cable lengths. Refer to application note AN-1822 for more details regarding this application.

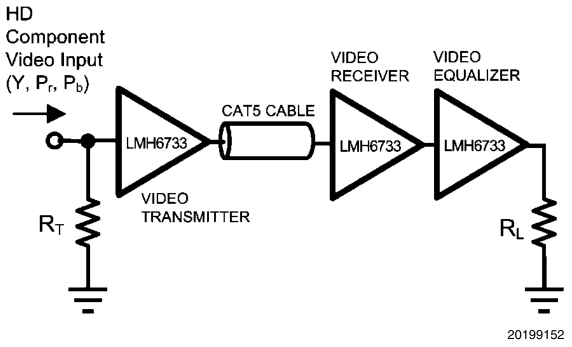

FIGURE 6. CAT5 High Definition Video Transmission

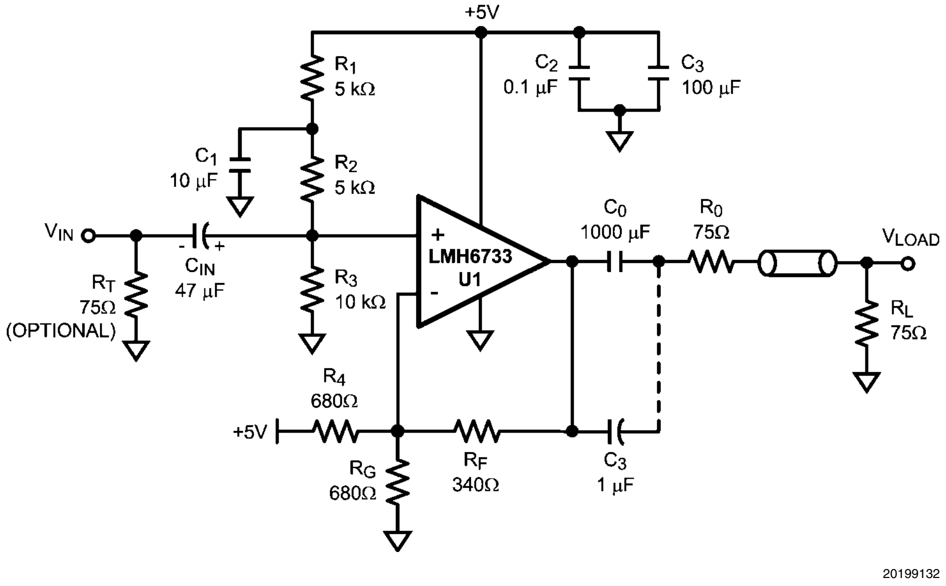

FIGURE 7. AC Coupled Single Supply Video Amplifier

AC-COUPLED VIDEO

The LMH6733 can be used as an AC-coupled single supply video amplifier for driving 75Ω coax with a gain of 2. The input signal is nominally 0.7V or 1.0V for component YP_RP_B and RGB, depending on the presence of a sync. R_1, R_2, and R_3 simply set the input to the center of the input linear range while C_{IN} AC couples the video onto the op amp's input.

As can be seen in , Figure 7 amplifier U1 is used in a positive gain configuration set for a closed loop gain of 2. The feedback resistor R_F is 340Ω. The gain resistor is created from the parallel combination of R_G and R_4, giving a Thevenin equivalent of 340Ω connected to 2.5V.

The 75Ω back termination resistor R_O divides the signal such that V_{OUT} equals a buffered version of V_{IN}. The back termination will eliminate any reflection of the signal that comes from the load. The input termination resistor, R_T, is optional – it is used only if matching of the incoming line is necessary. In some applications, it is recommended that a small valued ceramic capacitor be used in parallel with C_O which is itself electrolytic because of its rather large value. The ceramic cap will tend to shunt the inductive behavior of this electrolytic cap, C_O, at higher frequencies for an improved overall, low-impedance output.

INVERTING INPUT PARASITIC CAPACITANCE

Parasitic capacitance is any capacitance in a circuit that was not intentionally added. It comes about from electrical interaction between conductors. Parasitic capacitance can be reduced but never entirely eliminated. Most parasitic capacitances that cause problems are related to board layout or lack of termination on transmission lines. Please see the section on Layout Considerations for hints on reducing problems due to parasitic capacitances on board traces. Transmission lines should be terminated in their characteristic impedance at both ends.

High speed amplifiers are sensitive to capacitance between the inverting input and ground or power supplies. This shows up as gain peaking at high frequency. The capacitor raises device gain at high frequencies by making R_G appear smaller. Capacitive output loading will exaggerate this effect. In general, avoid introducing unnecessary parasitic capacitance at both the inverting input and the output.

One possible remedy for this effect is to slightly increase the value of the feedback (and gain set) resistor. This will tend to offset the high frequency gain peaking while leaving other parameters relatively unchanged. If the device has a capacitive load as well as inverting input capacitance using a series output resistor as described in the section on "Driving Capacitive Loads" will help.

LAYOUT CONSIDERATIONS

Whenever questions about layout arise, use the evaluation board as a guide. The LMH730275 is the evaluation board supplied with samples of the LMH6733.

To reduce parasitic capacitances ground and power planes should be removed near the input and output pins. Components in the feedback loop should be placed as close to the device as possible. For long signal paths controlled impedance lines should be used, along with impedance matching elements at both ends.

Bypass capacitors should be placed as close to the device as possible. Bypass capacitors from each rail to ground are applied in pairs. The larger electrolytic bypass capacitors can be located farther from the device, the smaller ceramic capacitors should be placed as close to the device as possible. The LMH6733 has multiple power and ground pins for enhanced supply bypassing. Every pin should ideally have a separate bypass capacitor. Sharing bypass capacitors may slightly degrade second order harmonic performance, especially if the supply traces are thin and /or long. In Figure 1 and Figure 2 C_{SS} is optional, but is recommended for best second harmonic distortion. Another option to using C_{SS} is to use pairs of .01 µF and .1 µF ceramic capacitors for each supply bypass.

VIDEO PERFORMANCE

The LMH6733 has been designed to provide excellent performance with production quality video signals in a wide variety of formats such as HDTV and High Resolution VGA. NTSC and PAL performance is nearly flawless. Best performance will be obtained with back terminated loads. The back termination reduces reflections from the transmission line and effectively masks transmission line and other parasitic capacitances from the amplifier output stage. Figure 4 shows a typical configuration for driving a 75Ω cable. The amplifier is configured for a gain of two to make up for the 6 dB of loss in R_{OUT}.

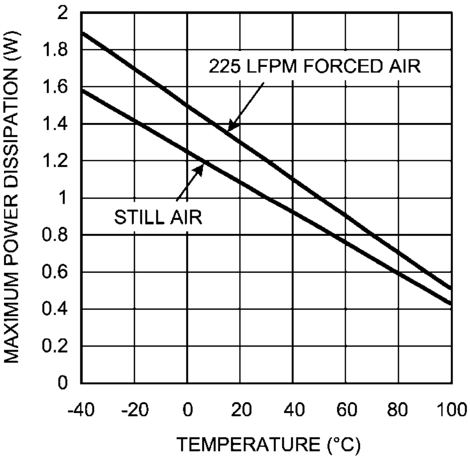

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FIGURE 8. Maximum Power Dissipation

POWER DISSIPATION

The LMH6733 is optimized for maximum speed and performance in the small form factor of the standard SSOP-16 package. To achieve its high level of performance, the LMH6733 consumes an appreciable amount of quiescent current which cannot be neglected when considering the total package power dissipation limit. The quiescent current contributes to about 40° C rise in junction temperature when no additional heat sink is used (V_S = ±5V, all 3 channels on). Therefore, it is easy to see that proper precautions need to be taken in order to make sure the junction temperature's absolute maximum rating of 150°C is not violated.

To ensure maximum output drive and highest performance, thermal shutdown is not provided. Therefore, it is of utmost importance to make sure that the T_{JMAX} is never exceeded due to the overall power dissipation (all 3 channels).

With the LMH6733 used in a back-terminated 75Ω RGB analog video system (with 2 V_{PP} output voltage), the total power dissipation is around 305 mW of which 220 mW is due to the quiescent device dissipation (output black level at 0V). With no additional heat sink used, that puts the junction temperature to about 120° C when operated at 85°C ambient.

To reduce the junction temperature many options are available. Forced air cooling is the easiest option. An external add-on heat-sink can be added to the SSOP-16 package, or alternatively, additional board metal (copper) area can be utilized as heat-sink.

An effective way to reduce the junction temperature for the SSOP-16 package (and other plastic packages) is to use the copper board area to conduct heat. With no enhancement the major heat flow path in this package is from the die through the metal lead frame (inside the package) and onto the surrounding copper through the interconnecting leads. Since high frequency performance requires limited metal near the device pins the best way to use board copper to remove heat is through the bottom of the package. A gap filler with high thermal conductivity can be used to conduct heat from the bottom of the package to copper on the circuit board. Vias to a ground or power plane on the back side of the circuit board will provide additional heat dissipation. A combination of front side copper and vias to the back side can be combined as well.

Follow these steps to determine the maximum power dissipation for the LMH6733:

1. Calculate the quiescent (no-load) power: $P_{AMP} = I_{CC}$ X (V_S), where $V_S = V^+ - V^-$
2. Calculate the RMS power dissipated in the output stage: P_D (rms) = rms ((V_S - V_{OUT}) X I_{OUT}) where V_{OUT} and I_{OUT} are the voltage and the current across the external load and V_S is the total supply voltage
3. Calculate the total RMS power: $P_T = P_{AMP}+P_D$

The maximum power that the LMH6733, package can dissipate at a given temperature can be derived with the following equation (See Figure 8):

P_{MAX} = (150°C/W– T_{AMB})/ θ_{JA}, where T_{AMB} = ambient temperature (°C) and θ_{JA} = thermal resistance, from junction to ambient, for a given package (°C/W). For the SSOP package θ_{JA} is 120°C/W.

ESD PROTECTION

The LMH6733 is protected against electrostatic discharge (ESD) on all pins. The LMH6733 will survive 2000V Human Body Model and 200V Machine Model events.

Under closed loop operation the ESD diodes have no affect on circuit performance. There are occasions, however, when the ESD diodes will be evident. If the LMH6733 is driven by a large signal while the device is powered down the ESD diodes will conduct.

The current that flows through the ESD diodes will either exit the chip through the supply pins or will flow through the device, hence it is possible to power up a chip with a large signal applied to the input pins. Shorting the power pins to each other will prevent the chip from being powered up through the input.

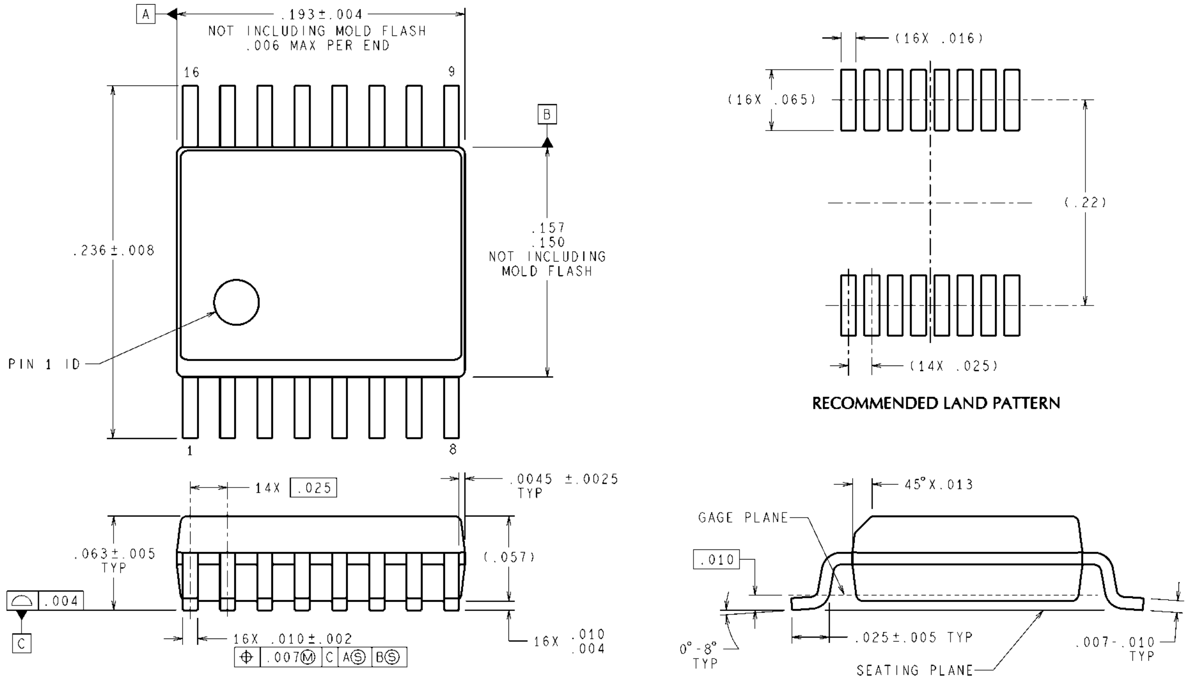
EVALUATION BOARDS

National Semiconductor provides the following evaluation boards as a guide for high frequency layout and as an aid in device testing and characterization. Many of the datasheet plots were measured with these boards.

Device	Package	Evaluation Board Part Number
LMH6733MQ	SSOP	LMH730275

A bare evaluation board can be ordered when a sample request is placed with National Semiconductor.

Physical Dimensions inches (millimeters) unless otherwise noted



DIMENSIONS ARE IN INCHES
DIMENSIONS IN ( ) FOR REFERENCE ONLY

MQA16 (Rev B)

16-Pin SSOP
NS Package Number MQA16

Notes

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