GaNPower International Inc.

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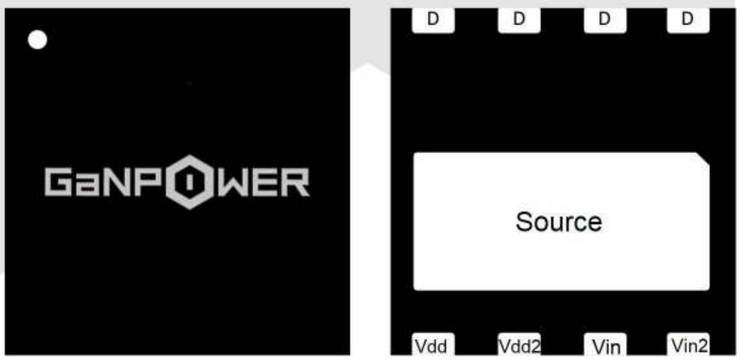
GPIRGIC15DFV

GaN Power IC in DFN8x8 Package

Datasheet version: 2.1

Features

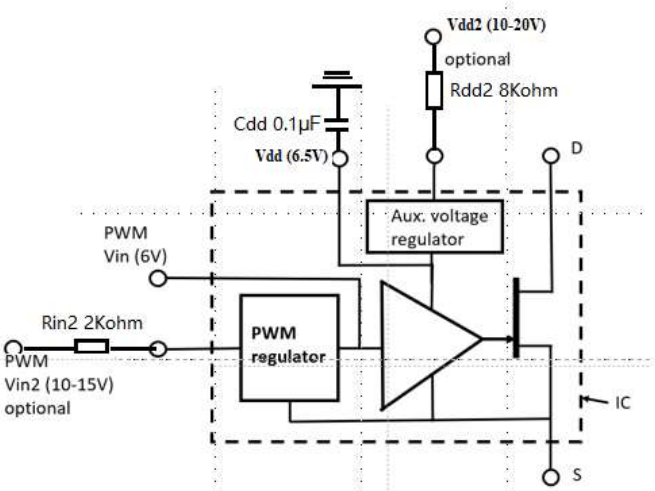
BVdss	Rdson	DC bus
900 V	85 mΩ	400-600 V



- Ultra-low R_{DS}(on)
- High dv/dt capability
- Fast switching
- Low Profile
- Suitable for DC bus voltage of 400-600 V

Applications

- Switching Power Applications
- Power adapters and power delivery chargers
- Start up procedure: Please set Vdd to be a normal operation voltage (e.g., 6.5 V) before turning on the high voltage power supply or apply high voltage to the drain. Vdd is the power supply for the internal gate driver in our GaN Power IC. Only when a normal operation voltage is applied to Vdd (e.g., 6.5 V), will the internal driver and GaN HEMT work properly. Alternately, Vdd2 (e.g., 8-20 V) with appropriate Rdd2 can be used to replace Vdd.
- Application configurations: PWM options: 1) Vin2-open, Vin(PWM)=6.5 V or 2) Vin-open, Vin2(PWM)=8-15V with Rin2=2kOhm. Auxiliary power options: 1) Vdd2-open; Vdd=6.5V or 2) Vdd connected to 0.1uF, Vdd2=8-30V (set at 15V), Rdd2=8kOhm connected to secondary of transformer.



Description

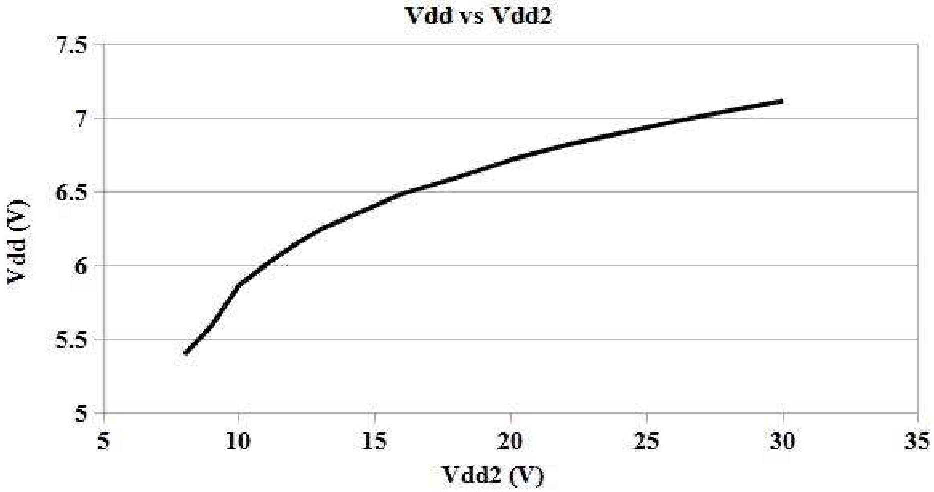
These devices are power IC based on Power GaN HEMTs using proprietary E-mode GaN on silicon technology. The voltage regulator and gate driver are integrated with the main power transistor resulting in large-voltage tuning range, fast switching, high system power density and low cost.

Device Characteristics

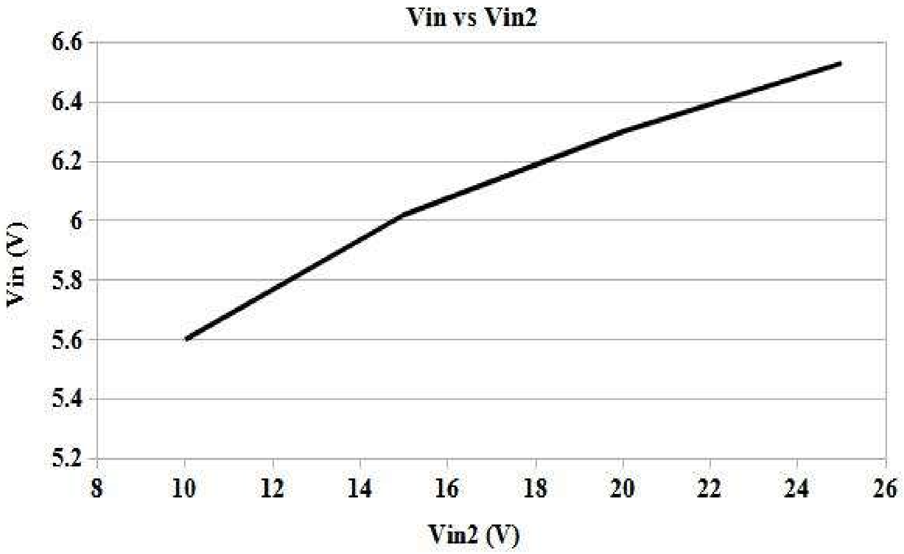
Basic Parameters				**Test data**			
	Parameters		**Conditions**	**Min**	**Typical**	**Max**	**Unit**
1	BV_{dss}	Drain-Source breakdown voltage	V_{gs}=0V I_d=10uA	900			V
2	R_{dson}	Static drain-source on resistance, T_C = 25°C	V_{in}=6V, V_{dd}=6.5V, I_d=2.5A,		85	105	mΩ
3	R_{dson}	Static drain-source on resistance, T_C = 125°C	V_{in}=6V, V_{dd}=6.5V, I_d=2.5A,		170		mΩ
4	V_{dd}	Drive supply voltage		5	6.5	8	V
5	V_{in}	PWM input voltage		3	5	8	V
6	V_{dd2}	Aux voltage regulator voltage		8	15	30	
7	V_{in2}	PWM regulator voltage		8	15	20	
8	I_{ddq}	Drive supply (V_{dd}) quiescent leakage current	V_{dd}=6.5V		1.9		µA
8	I_{ddq}	Drive supply (V_{dd}) quiescent leakage current	V_{dd2}=15V		290		µA
Switching Performance				**Test data**			
	Parameters		**Conditions**	**Min**	**Typical**	**Max**	**Unit**
1	$t_{d(on)}$	Turn-on delay time	V_{bus}=600V, I_d=2A, V_{in}=6V, V_{dd}=6V		10		ns
2	t_r	Rise time			70		ns
3	$t_{d(off)}$	Turn-off delay time			20		ns
4	t_f	Fall time			20		ns

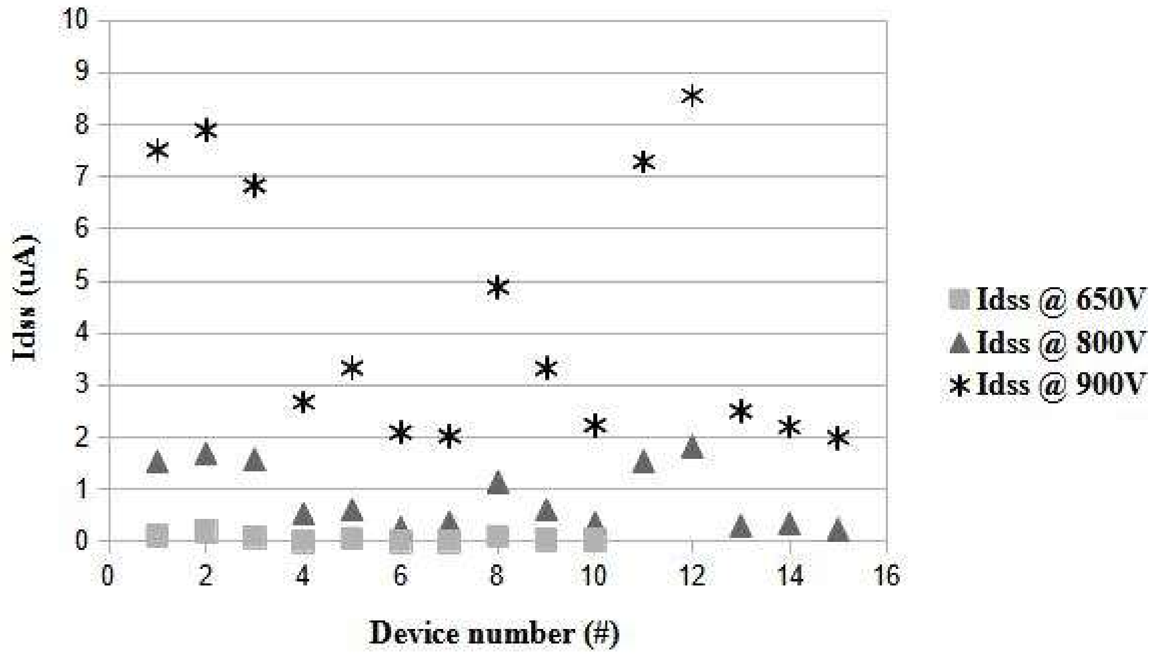
Electrical Performance

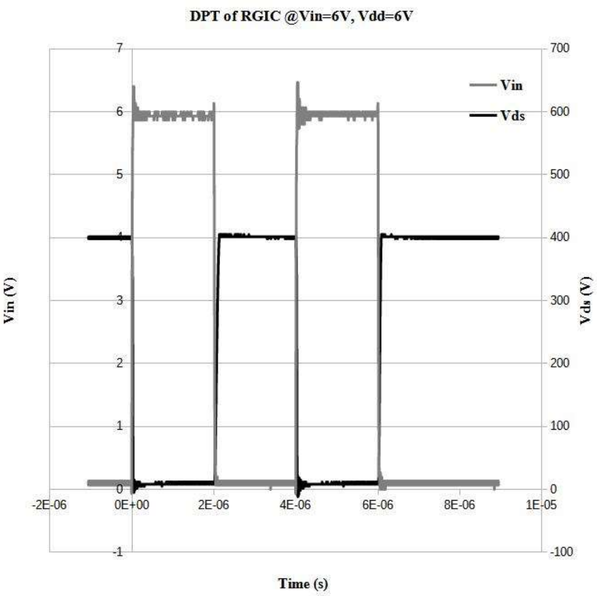
Vdd vs Vdd2 @DC
(Vin=0 V, Rdd2=8kΩ)



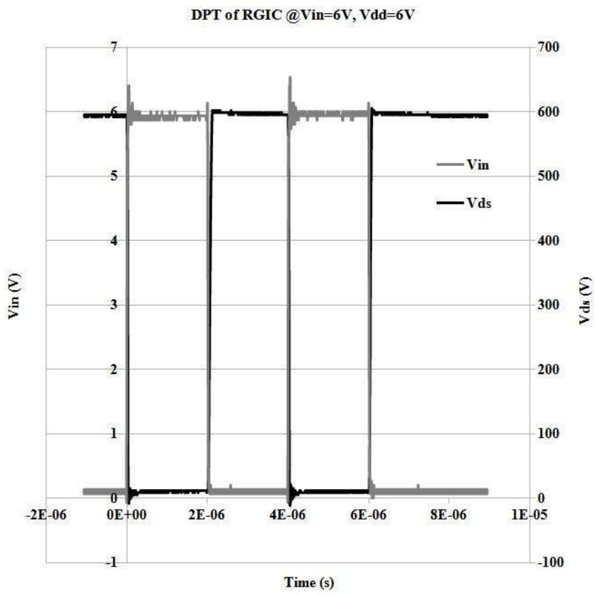
Vin vs Vin2 @DC
(Vdd=6.5V, Rin2=2kΩ)



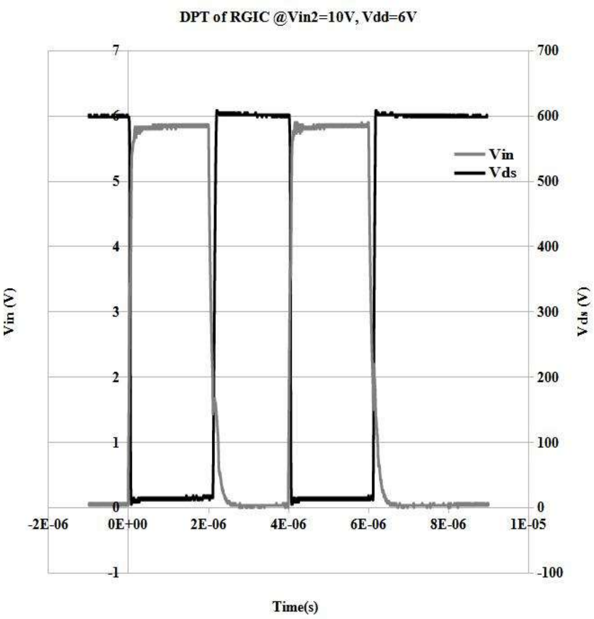

10
9
8
7
6
5
4
3
2
1
0
Idss (uA)
0
2
4
6
8
10
12
14
16
Device number (#)
Idss @ 650V
Idss @ 800V
Idss @ 900V



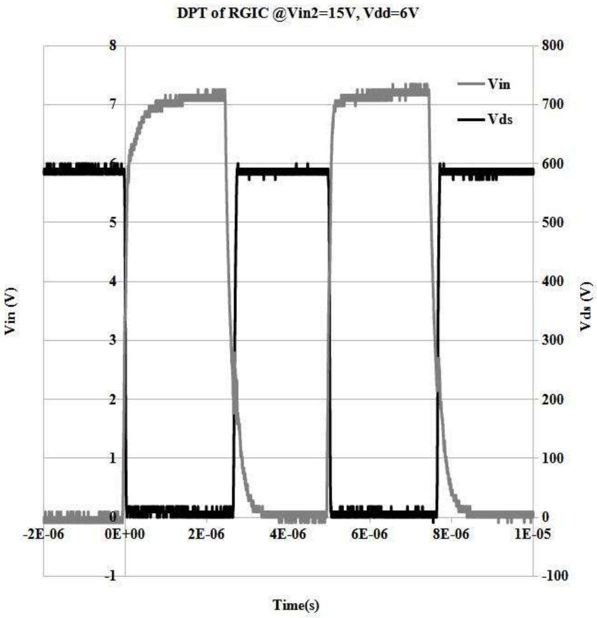
DPT test @V_{in}=6V, V_{dd}=6V, V_{bus}=400V, R_{in}=0, R_{dd}=0



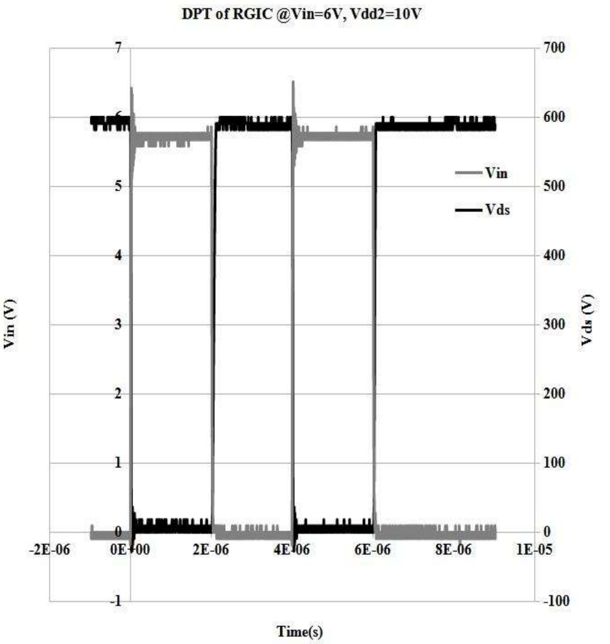
DPT test @V_{in}=6V, V_{dd}=6V, V_{bus}=600V, R_{in}=0, R_{dd}=0



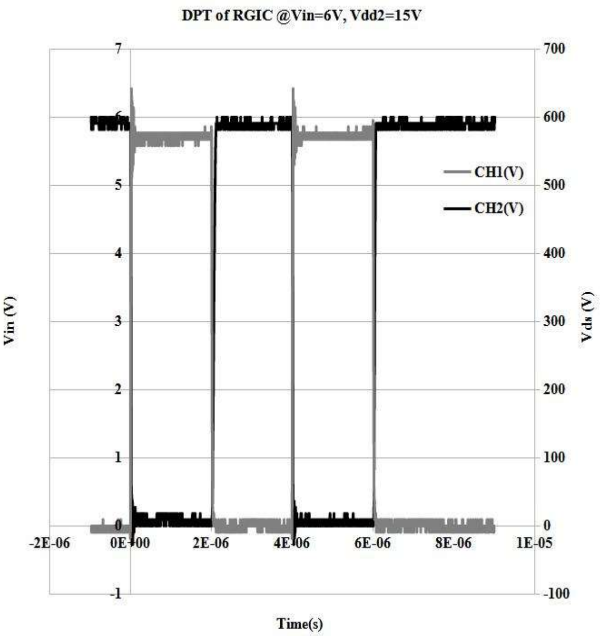
DPT test @V_{in2}=10V, V_{dd}=6V, V_{bus}=600V, R_{in2}=1kΩ, R_{dd}=0



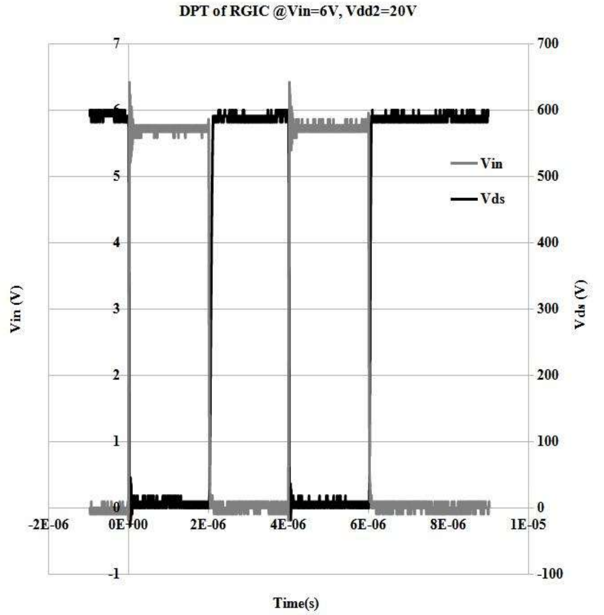
DPT test @V_{in2}=15V, V_{dd}=6V, V_{bus}=600V, R_{in2}=1kΩ, R_{dd}=0



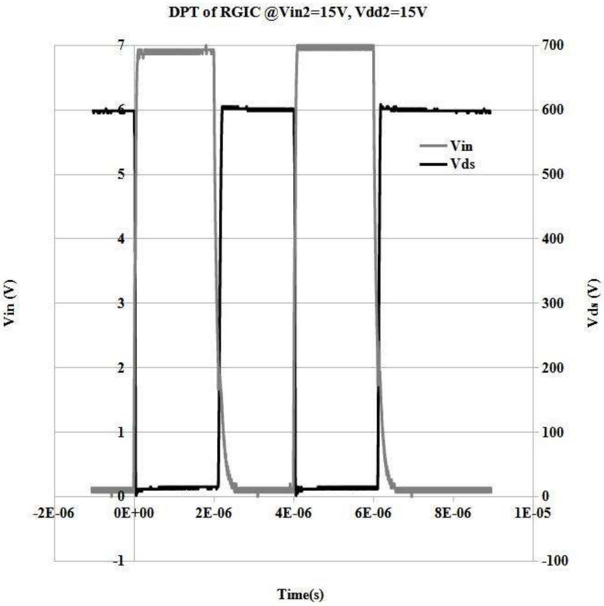
DPT test @V_{in}=6V, V_{dd2}=10V, V_{bus}=600V, R_{in}=0, R_{dd2}=8K, C_{dd}=0.1uF



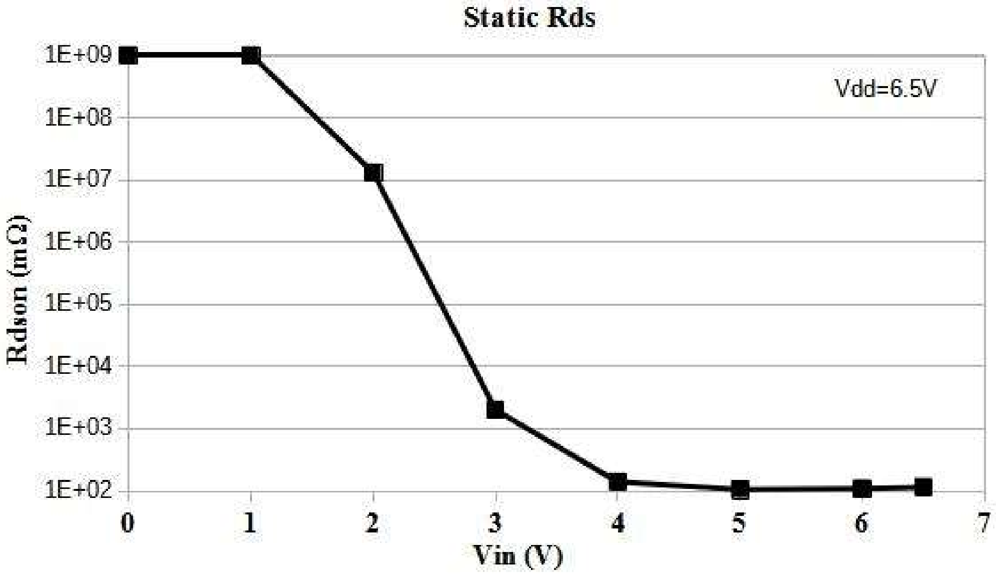
DPT test @V_{in}=6V, V_{dd2}=15V, V_{bus}=600V, R_{in}=0, R_{dd2}=8K, C_{dd}=0.1uF



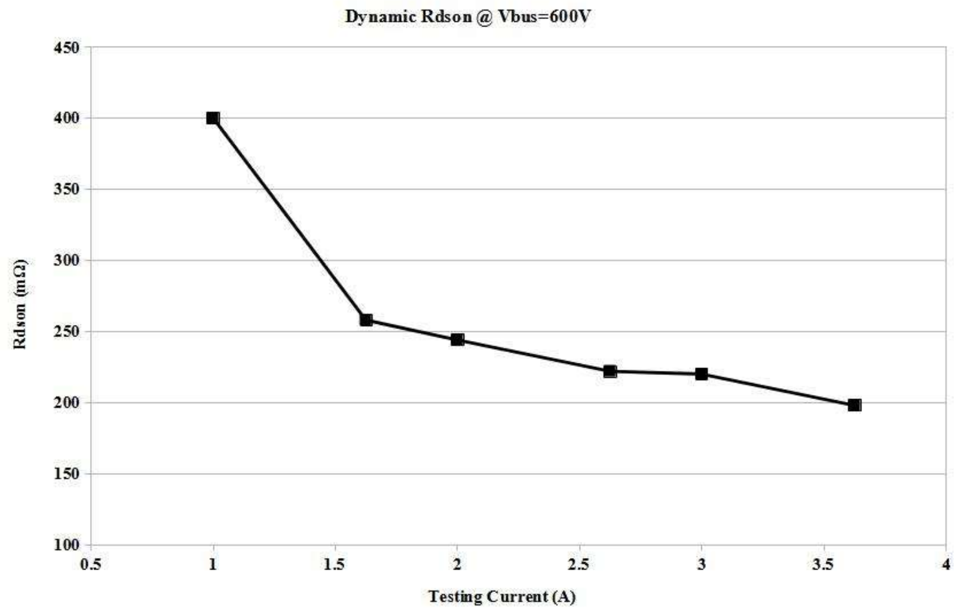
DPT test @V_{in}=6V, V_{dd2}=20V, V_{bus}=600V, R_{in}=0, R_{dd2}=8K, C_{dd}=0.1uF



DPT test @V_{in2}=15V, V_{dd2}=15V, V_{bus}=600V, R_{in2}=1K, R_{dd2}=8K, C_{dd}=0.1uF

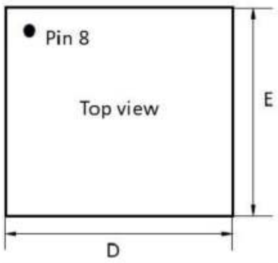


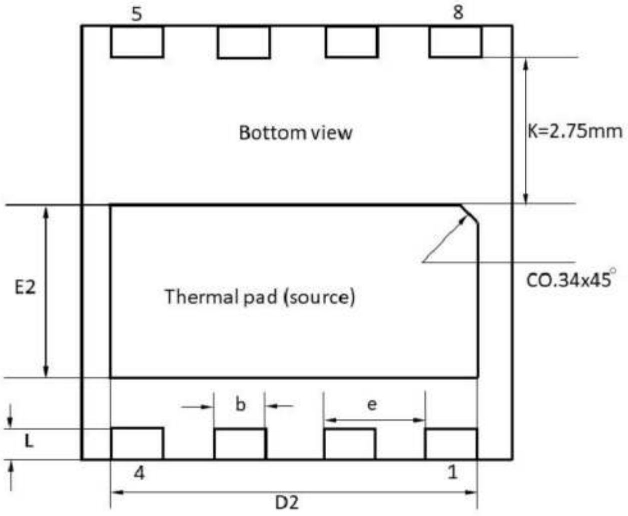
Rds versus V_{in} @V_{dd}=6.5V



Note: Dynamic R_{dson} data were captured the moment near the end of the second pulse, in order to exclude any influence of ringing and overshooting. Normally the dynamic Rdson is measured at 1 µs after IC turn-on.

Package Information

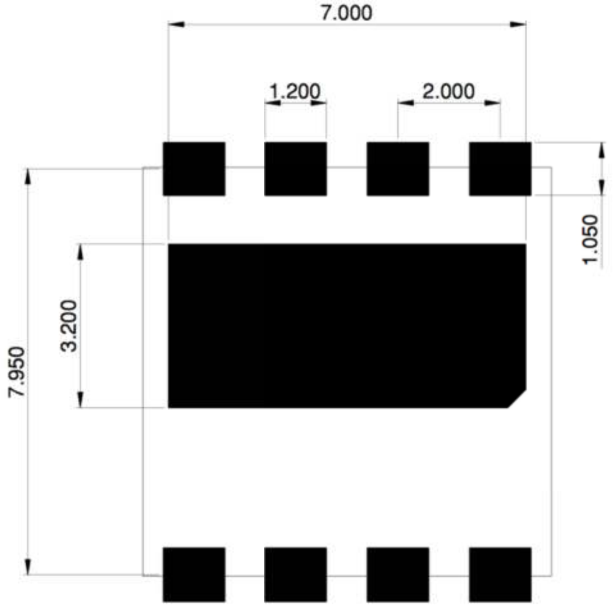




D=8; E=8; e=1.95; b=0.97;
L=0.57; D2=6.82; E2=3.19

8LEAD DFN (8x8x0.75mm, Pitch 1.95mm)

IMPORTANT: Please connect the bottom thermal pad to the source electrode on PCB



Land Pattern View

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GaN HEMT Frequently Asked Questions

1	Q: Can we do pin to pin switch for silicon MOSFET or IGBT? A: The short answer is no. GaN HEMT power devices are far superior than the best silicon devices such as super junction MOSFETs. However, due to different requirements of gate driving voltage and extremely high dv/dt slew rate, special drivers and optimized PCB layouts are recommended to minimize the impact from circuit parasitics.
2	Q: How do GaN power devices compare with SiC? A: Currently GaN power HEMT devices are most suitable for low to medium voltage (≤1200V) and power (<20KW) applications. GaN is the ideal choice for high frequency applications. SiC devices are better choice for high voltage and high-power applications (>20KW).
3	Q: Do we need to parallel an FRD for applications such as inverters? A: GaN devices are different from silicon MOSFET or IGBT in that they have no inherent PN junction diodes that cause reverse recovery issue. User do not need to parallel an FRD for the purpose of suppressing the body diode reverse recovery effect, since GaN HEMT can operate in both first and third quadrants. However, care should be taken for the dead time power loss since the Vsd voltage of GaN HEMT is usually close to 2V. This is especially true when a negative gate voltage is applied.
4	Q: Can we parallel GaN HEMT devices? A: Yes, GaN HEMT is ideal for paralleling, due to the positive temperature coefficient of $R_{ds,on}$. Hence, paralleling GaN HEMT devices are encouraged.