PTN3342

High speed differential line receiver

Rev. 02 — 10 August 2006

Product data sheet

1. General description

The PTN3342 is a differential line receiver that implements the electrical characteristics of Low-Voltage Differential Signaling (LVDS). This device meets or exceeds the requirements of the *ANSI TIA/EIA-644 Standard*. LVDS is used to achieve higher data rates on commonly used media. LVDS overcomes the limitations of achievable slew rates and EMI restrictions of previous differential signaling techniques. The PTN3342 operates at a 3.3 V supply level. Any of the four differential receivers provides a valid logical output state with a ±100 mV differential input voltage within the input common-mode voltage range. The input common-mode voltage range allows 1 V of ground potential difference between two LVDS nodes. The PTN3342 is identical to the PTN3332 but with the termination resistor integrated with the receiver.

The intended application of this device is for point-to-point baseband transmission rates over a controlled impedance media of approximately 100 Ω. The maximum rates and distance of data transfer are dependent upon the attenuation characteristics of the media selected and the noise coupling to the environment.

The PTN3342 is designed to function over the full industrial temperature range of –40 °C to +85 °C.

2. Features

- Meets or exceeds the requirements of ANSI *TIA/EIA-644 Standard*
- Designed for signaling rates of up to 400 Mbit/s
- Differential input thresholds of ±100 mV
- Power dissipation of 60 mW typical at 200 MHz
- Typical propagation delay of 2.6 ns
- Low Voltage TTL (LVTTL) logic output levels
- Pin compatible with AM26LS32 and SN65LVDS32
- Open-circuit fail safe
- Termination resistors on chip

3. Applications

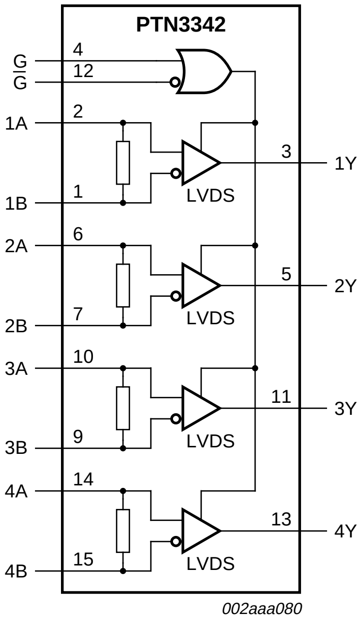
- Low voltage, low EMI, high speed differential signal receiver
- Point-to-point high speed data transmission
- High performance switches and routers

4. Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
PTN3342DH	TSSOP16	plastic thin shrink small outline package; 16 leads; body width 4.4 mm	SOT403-1
PTN3342D	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1

5. Functional diagram



resistors = 110 Ω

Fig 1. Functional diagram of PTN3342

6. Pinning information

6.1 Pinning

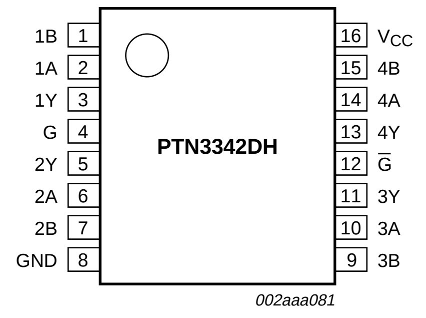


Fig 2. Pin configuration for TSSOP16

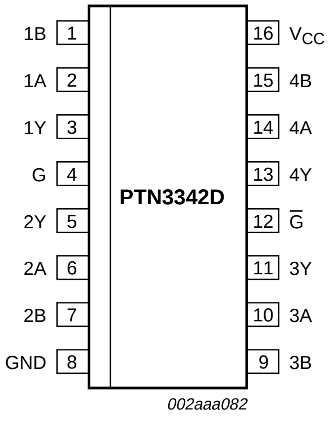


Fig 3. Pin configuration for SO16

6.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
1B	1	LVDS inverting input
1A	2	LVDS non-inverting input
1Y	3	LVTTL output
G	4	enable (active HIGH)
2Y	5	LVTTL output
2A	6	LVDS non-inverting input
2B	7	LVDS inverting input
GND	8	ground
3B	9	LVDS inverting input
3A	10	LVDS non-inverting input
3Y	11	LVTTL output
$\overline{G}$	12	enable (active LOW)
4Y	13	LVTTL output
4A	14	LVDS non-inverting input
4B	15	LVDS inverting input
V_{CC}	16	supply voltage

7. Functional description

Refer to Figure 1 “Functional diagram of PTN3342”.

7.1 Function table

Table 3. Function table
H = HIGH level; L = LOW level; X = irrelevant; high-Z = high-impedance; ? = indeterminate state

Differential input	Enables		Output
nA, nB	**G**	**$\overline{G}$**	**nY**
$V_{ID} \geq 100$ mV	H	X	H
	X	L	H
-100 mV $< V_{ID} <$ 100 mV	H	X	?
	X	L	?
$V_{ID} \leq -100$ mV	H	X	L
	X	L	L
X	L	H	high-Z
Open	H	X	L
	X	L	L

8. Limiting values

Table 4. Limiting values
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		–0.5	4.0	V
V_I	input voltage	enables and outputs	–0.5	V_{CC} + 0.5	V
T_{amb}	ambient temperature	operating	–40	+85	°C
T_j	junction temperature	operating	–40	+150	°C
T_{stg}	storage temperature		–65	+150	°C
V_{esd}	electrostatic discharge voltage		> 2	-	kV

9. Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	supply voltage		3	3.3	3.6	V
V_{IH}	HIGH-level input voltage		2	-	-	V
V_{IL}	LOW-level input voltage		-	-	0.8	V
V_{ID}	differential input voltage		0.1	-	0.6	V
V_{IC}	common-mode input voltage		$0.5V_{ID}$	-	$2.4 - 0.5V_{ID}$	V
T_{amb}	ambient temperature	operating	–40	-	+85	°C

10. Static characteristics

Table 6. Static characteristics

Over recommended operating conditions, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ[1]	Max	Unit
V_{rr+}	positive differential input voltage threshold	see Figure 4 and Table 8	-	-	100	mV
V_{rr-}	negative differential input voltage threshold	see Figure 4 and Table 8	–100	-	-	mV
V_{OH}	HIGH-level output voltage	$I_{OH} = -8$ mA	2.4	-	-	V
		$I_{OH} = -4$ mA	2.8	-	-	V
V_{OL}	LOW-level output voltage		-	-	0.4	V
I_{CC}	supply current	enabled; no load	-	10	18	mA
		disabled	-	0.25	0.5	mA
I_I	input current	A or B inputs; input current measured with other input open				
		$V_I = 0$ V	–2	–10	–20	µA
		$V_I = 2.4$ V	0	10	20	µA
$I_{I(OFF)}$	power-off input current	A or B inputs; $V_{CC} = 0$ V; $V_I = 3.6$ V	-	6	20	µA
I_{IH}	HIGH-level input current	G or $\overline{G}$ inputs; $V_{IH} = 2$ V	-	-	10	µA
I_{IL}	LOW-level input current	G or $\overline{G}$ inputs; $V_{IL} = 0.8$ V	-	-	10	µA
I_{OZ}	high-impedance output current	$V_O = 0$ V or V_{CC}	–10	-	+10	µA
R_T	termination resistance		88	-	132	Ω

[1] All typical values are at $T_{amb} = 25$ °C and $V_{CC} = 3.3$ V.

11. Dynamic characteristics

Table 7. Dynamic characteristics

Over recommended operating condition, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max[1]	Unit
t_{PLH}	LOW-to-HIGH propagation delay	output; C_L = 10 pF; see Figure 5		1.3	2.6	6	ns
t_{PHL}	HIGH-to-LOW propagation delay	output; C_L = 10 pF; see Figure 5		1.3	2.5	6	ns
t_r	rise time	output; 20 % to 80 %		-	0.6	-	ns
t_f	fall time	output; 80 % to 20 %		-	0.7	-	ns
$t_{sk(p)}$	pulse skew time	$t_{PHL} - t_{PLH}$		-	-	0.4	ns
$t_{sk(o)}$	output skew time	channel-to-channel	[2]	-	0.1	0.3	ns
$t_{sk(p-p)}$	part-to-part skew time		[3]	-	-	1	ns
t_{PZH}	propagation delay, high-impedance to HIGH-level output	see Figure 6		-	8	12	ns
t_{PZL}	propagation delay, high-impedance to LOW-level output	see Figure 6		-	3	12	ns
t_{PHZ}	propagation delay, HIGH-level to high-impedance output	see Figure 6		-	6.5	12	ns
t_{PLZ}	propagation delay, LOW-level to high-impedance output	see Figure 6		-	5.5	12	ns

[1] All typical values are at T_{amb} = 25 °C and V_{CC} = 3.3 V.

[2] $t_{sk(o)}$ is the skew between specified outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical specified loads.

[3] $t_{sk(p-p)}$ is the magnitude of the difference in propagation delay times between any specified terminals of two devices when both devices operate with the same supply voltages, same temperature, and have identical packages and test circuits.

12. Test information

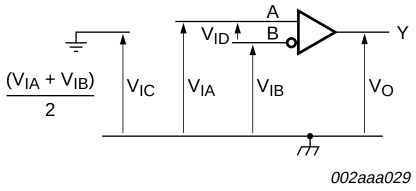


Fig 4. Voltage definitions

Table 8. Receiver minimum and maximum input threshold test voltages

Applied voltages		Resulting differential input voltage	Resulting common-mode input voltage
V_{IA}	V_{IB}	V_{ID}	V_{IC}
1.25 V	1.15 V	100 mV	1.2 V
1.15 V	1.25 V	–100 mV	1.2 V
2.4 V	2.3 V	100 mV	2.35 V
2.3 V	2.4 V	–100 mV	2.35 V
0.1 V	0 V	100 mV	0.05 V
0 V	0.1 V	–100 mV	0.05 V
1.5 V	0.9 V	600 mV	1.2 V
0.9 V	1.5 V	–600 mV	1.2 V
2.4 V	1.8 V	600 mV	2.1 V
1.8 V	2.4 V	–600 mV	2.1 V
0.6 V	0 V	600 mV	0.3 V
0 V	0.6 V	–600 mV	0.3 V

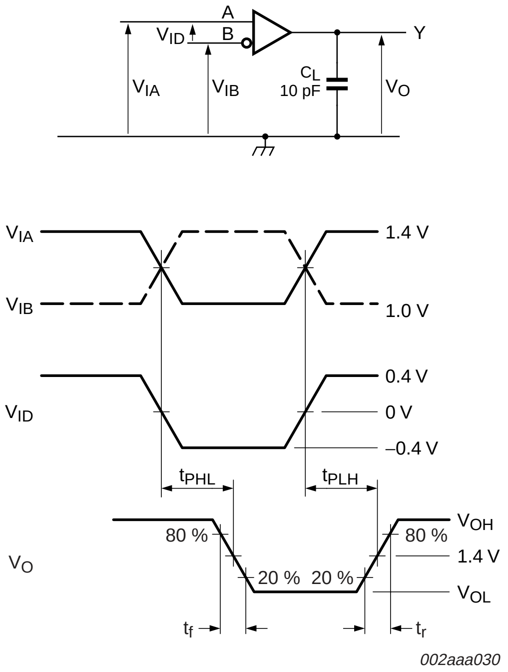


Fig 5. **Timing test circuit and waveforms**

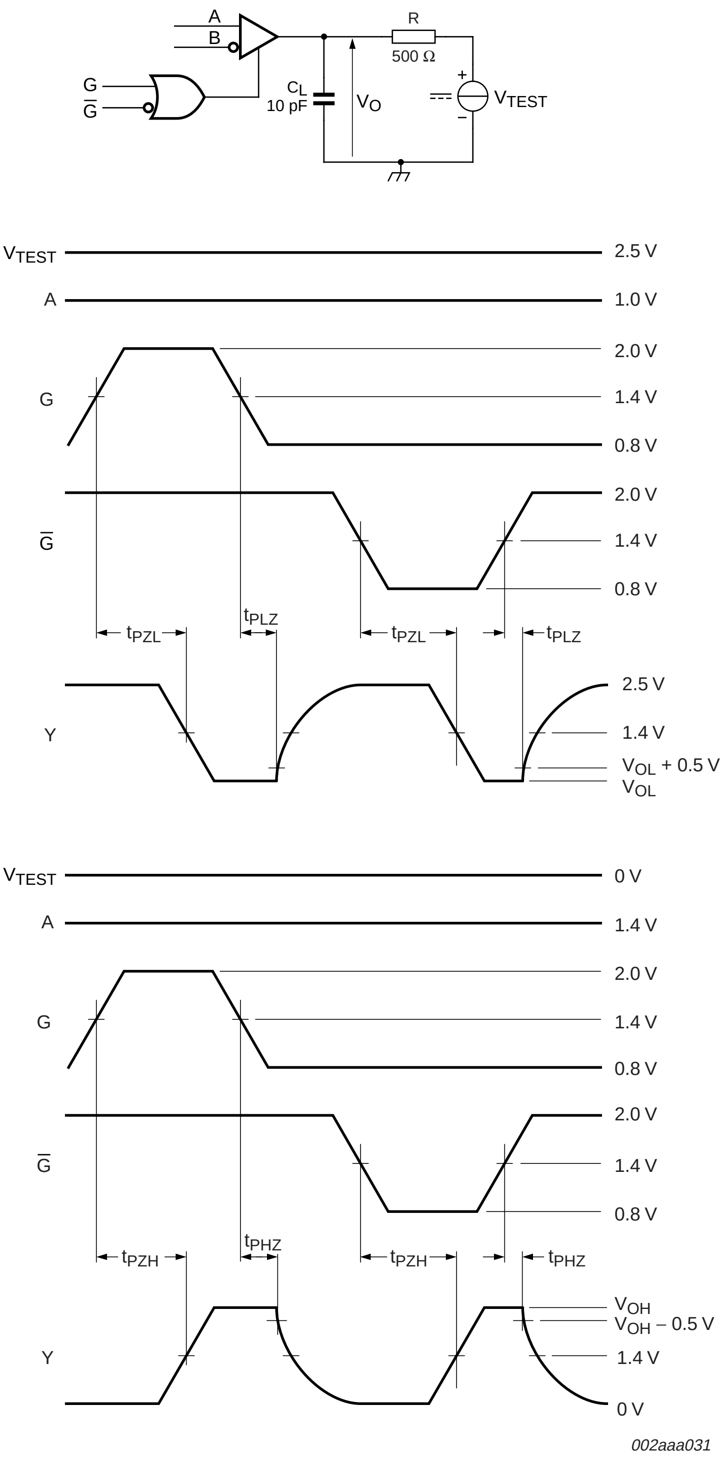
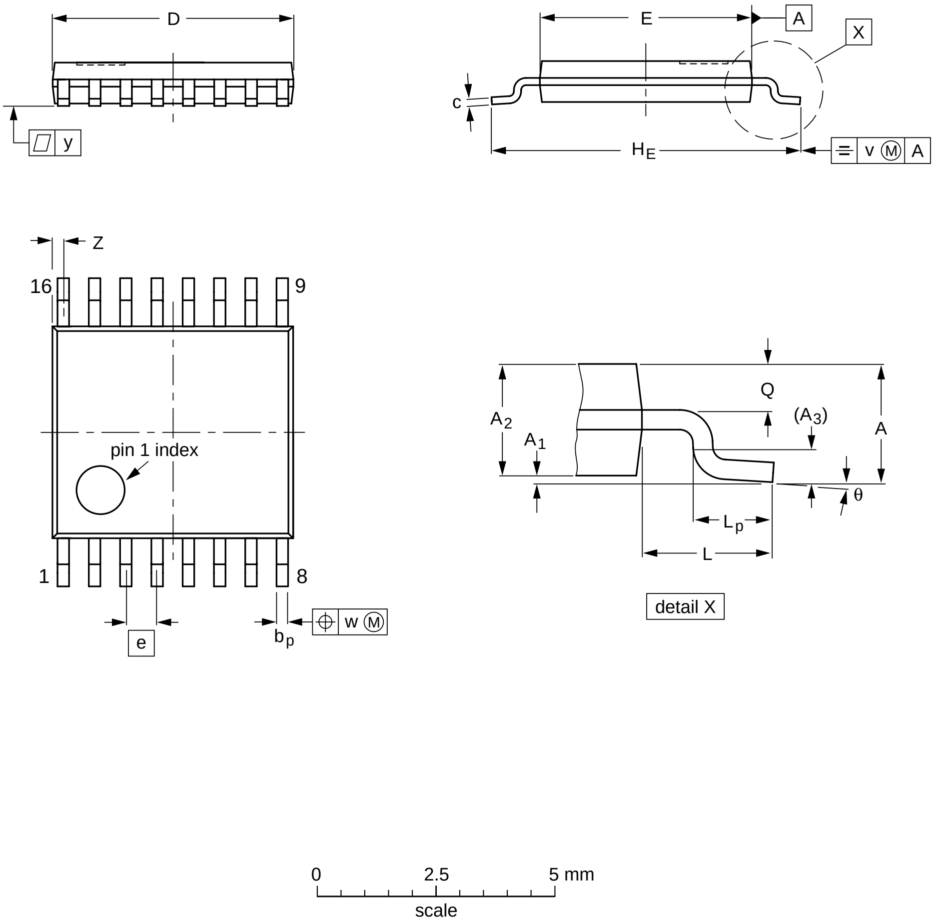


Fig 6. Enable/disable time test circuit and waveforms

13. Package outline

TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm **SOT403-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (2)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	5.1 4.9	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.40 0.06	8° 0°

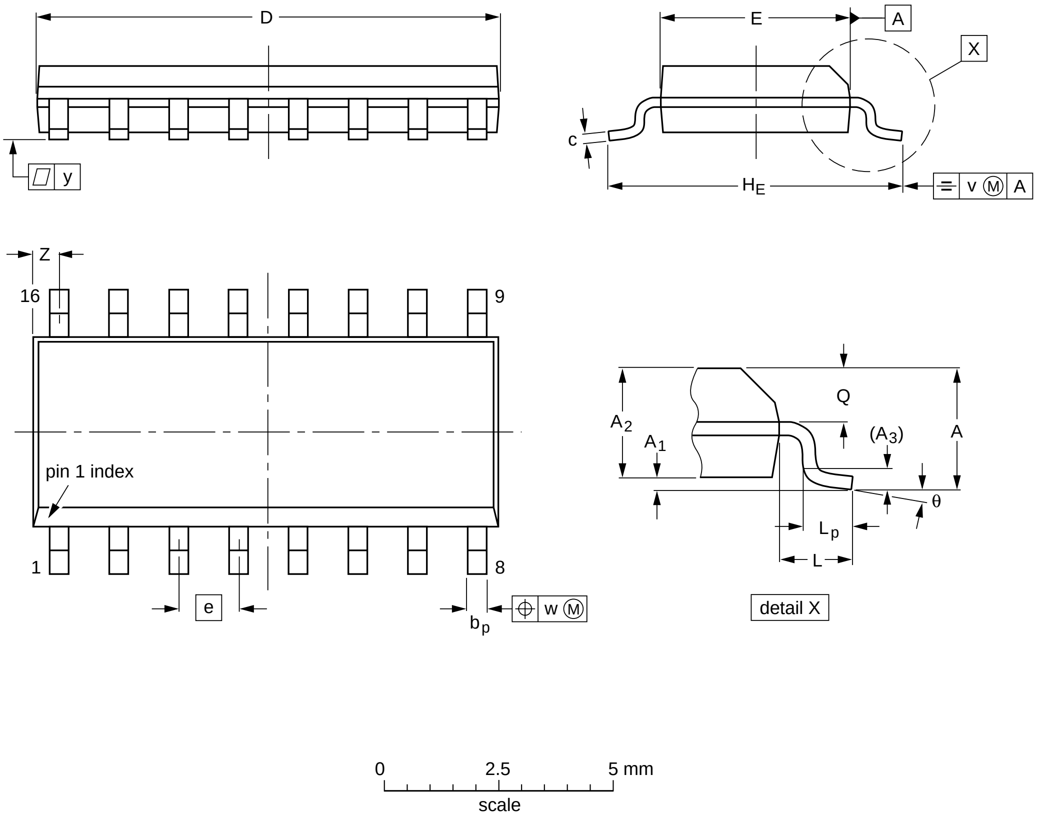
Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT403-1		MO-153				~~99-12-27~~ 03-02-18

Fig 7. Package outline SOT403-1 (TSSOP16)

SO16: plastic small outline package; 16 leads; body width 3.9 mm **SOT109-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	10.0 9.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.39 0.38	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.028 0.020	0.01	0.01	0.004	0.028 0.012	

Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT109-1	076E07	MS-012				~~99-12-27~~ 03-02-19

Fig 8. Package outline SOT109-1 (SO16)

14. Soldering

14.1 Introduction to soldering surface mount packages

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering can still be used for certain surface mount ICs, but it is not suitable for fine pitch SMDs. In these situations reflow soldering is recommended.

14.2 Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement. Driven by legislation and environmental forces the worldwide use of lead-free solder pastes is increasing.

Several methods exist for reflowing; for example, convection or convection/infrared heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 seconds and 200 seconds depending on heating method.

Typical reflow temperatures range from 215 °C to 260 °C depending on solder paste material. The peak top-surface temperature of the packages should be kept below:

Table 9. SnPb eutectic process - package peak reflow temperatures (from *J-STD-020C* July 2004)

Package thickness	Volume mm^3 < 350	Volume mm^3 ≥ 350
< 2.5 mm	240 °C + 0/–5 °C	225 °C + 0/–5 °C
≥ 2.5 mm	225 °C + 0/–5 °C	225 °C + 0/–5 °C

Table 10. Pb-free process - package peak reflow temperatures (from *J-STD-020C* July 2004)

Package thickness	Volume mm^3 < 350	Volume mm^3 350 to 2000	Volume mm^3 > 2000
< 1.6 mm	260 °C + 0 °C	260 °C + 0 °C	260 °C + 0 °C
1.6 mm to 2.5 mm	260 °C + 0 °C	250 °C + 0 °C	245 °C + 0 °C
≥ 2.5 mm	250 °C + 0 °C	245 °C + 0 °C	245 °C + 0 °C

Moisture sensitivity precautions, as indicated on packing, must be respected at all times.

14.3 Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):

  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
  - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

  The footprint must incorporate solder thieves at the downstream end.

- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time of the leads in the wave ranges from 3 seconds to 4 seconds at 250 °C or 265 °C, depending on solder material applied, SnPb or Pb-free respectively.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

14.4 Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 seconds to 5 seconds between 270 °C and 320 °C.

14.5 Package related soldering information

Table 11. Suitability of surface mount IC packages for wave and reflow soldering methods

Package[1]	**Soldering method**	
	Wave	**Reflow**[2]
BGA, HTSSON..T[3], LBGA, LFBGA, SQFP, SSOP..T[3], TFBGA, VFBGA, XSON	not suitable	suitable
DHVQFN, HBCC, HBGA, HLQFP, HSO, HSOP, HSQFP, HSSON, HTQFP, HTSSOP, HVQFN, HVSON, SMS	not suitable[4]	suitable
PLCC[5], SO, SOJ	suitable	suitable
LQFP, QFP, TQFP	not recommended[5][6]	suitable
SSOP, TSSOP, VSO, VSSOP	not recommended[7]	suitable
CWQCCN..L[8], PMFP[9], WQCCN..L[8]	not suitable	not suitable

[1] For more detailed information on the BGA packages refer to the *(LF)BGA Application Note* (AN01026); order a copy from your Philips Semiconductors sales office.

[2] All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods*.

[3] These transparent plastic packages are extremely sensitive to reflow soldering conditions and must on no account be processed through more than one soldering cycle or subjected to infrared reflow soldering with peak temperature exceeding 217 °C ± 10 °C measured in the atmosphere of the reflow oven. The package body peak temperature must be kept as low as possible.

[4] These packages are not suitable for wave soldering. On versions with the heatsink on the bottom side, the solder cannot penetrate between the printed-circuit board and the heatsink. On versions with the heatsink on the top side, the solder might be deposited on the heatsink surface.

[5] If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.

[6] Wave soldering is suitable for LQFP, QFP and TQFP packages with a pitch (e) larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.

[7] Wave soldering is suitable for SSOP, TSSOP, VSO and VSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

[8] Image sensor packages in principle should not be soldered. They are mounted in sockets or delivered pre-mounted on flex foil. However, the image sensor package can be mounted by the client on a flex foil by using a hot bar soldering process. The appropriate soldering profile can be provided on request.

[9] Hot bar soldering or manual soldering is suitable for PMFP packages.

15. Abbreviations

Table 12. Abbreviations

Acronym	Description
ANSI	American National Standards Institute
EMI	ElectroMagnetic Interference
LVDS	Low Voltage Differential Signaling
LVTTL	Low Voltage Transistor-Transistor Logic
TTL	Transistor-Transistor Logic

16. Revision history

Table 13. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PTN3342_2	20060810	Product data sheet	-	PTN3342-01
Modifications:	• The format of this data sheet has been redesigned to comply with the new presentation and information standard of Philips Semiconductors. • Section 2 “Features”, second bullet item: changed “400 Mbps” to “400 Mbit/s” • Figure 1 “Functional diagram of PTN3342”: corrected nY pin names (pin 3 = 1Y; pin 5 = 2Y; pin 11 = 3Y) • Table 4 “Limiting values”: added symbol “V_{esd}” and changed parameter from “ESD” to “electrostatic discharge voltage” • Table 6 “Static characteristics”: – updated values for I_I (condition V_I = 2.4 V) from “–1.2 µA min; –3 µA typ” to “0 µA min; 10 µA typ; 20 µA max” – changed symbol “$Z_{(t)}$” to “R_T” and added parameter description “termination resistance” • added Section 15 “Abbreviations”			
PTN3342-01 (9397 750 08484)	20040105	Product data	853-2444 A14997 (20031215)	-

17. Legal information

17.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term ‘short data sheet’ is explained in section “Definitions”.

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.semiconductors.philips.com.

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19. Contents

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Date of release: 10 August 2006

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