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IPS4260L

Datasheet

Quad low-side intelligent power switch

HTSSOP20

Features

- 8 V to 50 V operating voltage range
- Four independent protected channels
- V_{CC} undervoltage lock-out
- High speed operation (t_r, t_f < 1 µs)
- Programmable load current limitation level by external resistor
- Typical operating load current: 0.5 A (per channel) / 2 A (one channel)
- Thermally independent junction overtemperature protections
- Programmable non-dissipative short-circuit protection (cut-off) by external resistor
- Open load (off-state) and short-to-ground activated by external pull-down resistors
- Fast demagnetization of inductive loads with integrated catch diodes clamping turn-off transients
- Ground and V_{CC} wire break protection
- V_{CC} overvoltage protection
- Common open load diagnostic
- Common thermal shutdown and overload diagnostic
- Per channel thermal shutdown diagnostic
- Designed to meet IEC 61131-2
- Miniaturized HTSSOP20 package

Product status link

IPS4260L

Product label

SUSTAINABLE TECHNOLOGY

Application

- Programmable logic control
- Industrial PC peripheral input/output
- Numerical control machines
- General low-side switch applications

Description

The IPS4260L is a monolithic high speed (F_{SW} up to 250 kHz) device, which can drive four independent capacitive, resistive or inductive loads with one side connected to supply voltage. The channels can be parallelized to reduce power dissipation.

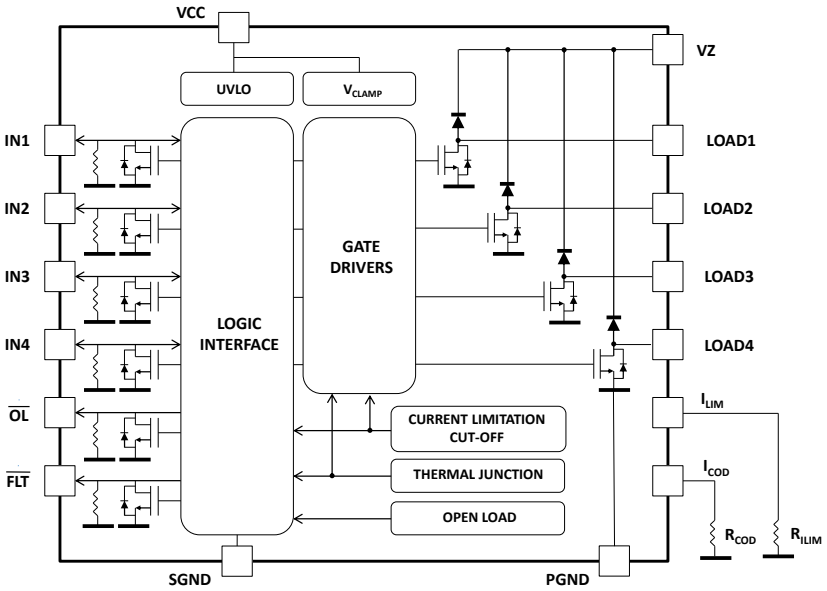
When connected to Vcc rail, four integrated catch diodes clamp the turn-off transients generated by inductive loads even with huge inductance; combined with proper external TVS connected to VCC or to GND the IC allows fast decay, too. Each channel is protected against overload or short circuit event: the intervention level can be set by an external resistor on I_{LIM} pin .

Built-in thermal shutdown protects the chip against overtemperature even in case of short-circuit. If enabled, the integrated cut-off protection features a non-dissipative protection in case of overload; it limits both the output average current value and, consequently, the device overheating. Cut-off delay/restart can be programmed by external resistors on CoD pin; it can be disabled by shorting CoD to GND.

Two common diagnostic open drains pins (OL, for open load and FLT for cut-off and thermal shutdown) together with the four open drain on each INx pin (cut-off and thermal shutdown) feature an extensive diagnostic of the chip.

1 Block diagram

Figure 1. **Block diagram**



2 Pin description

Figure 2. **Pin connection (top view)**

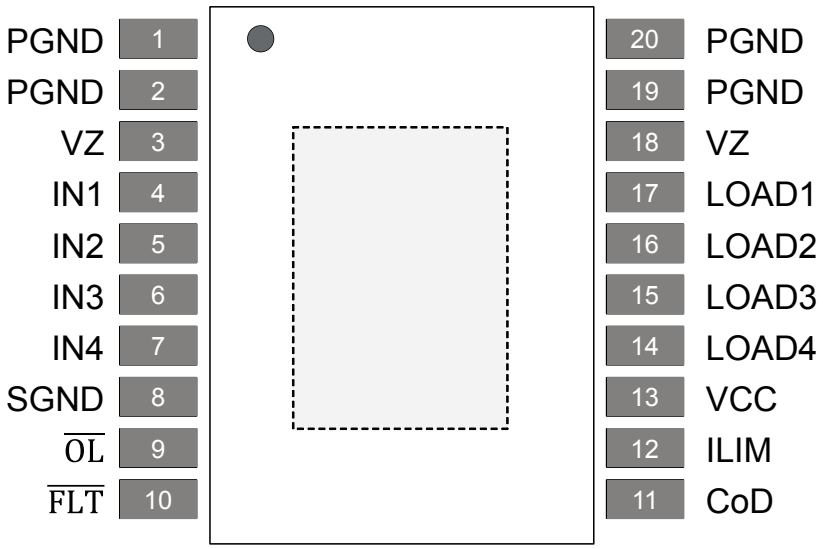


Table 1. **Pin configuration**

Number	Name	Function	Type
1, 2, 19, 20	PGND	Integrated power switch ground	Supply
3, 18	VZ	Load clamp voltage pins. Pins 3 and 18 must be shorted on the application board and then connected directly to the supply rail, or by an external Zener or TVS diode to the supply rail or to PGND (see Section 2.3 VZ)	Output
4	IN1	Channel 1 input / cut-off and thermal shutdown diagnostic	Input/output open drain
5	IN2	Channel 2 input / cut-off and thermal shutdown diagnostic	Input/output open drain
6	IN3	Channel 3 input / cut-off and thermal shutdown diagnostic	Input/output open drain
7	IN4	Channel 4 input / cut-off and thermal shutdown diagnostic	Input/output open drain
8, exposed pad	SGND	Logic interface block ground	Supply
9	$\overline{OL}$	Cumulative power stage open load or short ground common diagnostic	Output open drain
10	$\overline{FLT}$	Cut-off and thermal shutdown pin. Common diagnostic pin both for thermal shutdown and cut-off	Output open drain
11	CoD	Programmable cut-off intervention delay during overcurrent operation. It cannot be left floating: connect to PCB SGND ground plane to disable the cut-off function or connect a resistor between CoD and PCB ground plane to set the delay (see Section 6.3 Current limitation and cut-off)	Input
12	ILIM	Limitation current adjustment. It cannot be left floating: connect a resistor between ILIM and SGND to set the current limit threshold (see Section 6.3 Current limitation and cut-off)	Input
13	VCC	Supply voltage. Connect to the supply rail	Supply
14	LOAD4	Power stage, channel 4	Input

Number	Name	Function	Type
15	LOAD3	Power stage, channel 3	Input
16	LOAD2	Power stage, channel 2	Input
17	LOAD1	Power stage, channel 1	Input

2.1 VCC

IC supply voltage. This pin has to be connected to the supply rail of the application.

2.2 PGND, SGND

PGND stands for power ground and it is internally connected to the source of the integrated switches. SGND stands for signal ground and it is the reference level for the logic interface. SGND and PGND pins must be shorted on the application board. In order to reduce as much as possible the switching noises from PGND to SGND, the application board has to be designed with two different ground planes for SGND and PGND. The two ground planes have to be shorted by a dedicated net.

2.3 VZ

These two pins (corresponding to the cathodes of the clamp diodes) must be shorted together on the application and connected directly to supply rail or, alternatively, connected by a Zener or TVS diode to supply rail or PGND. Connecting VZ pins directly to the supply rail implies that the inductive loads are demagnetized without fast decay option: in fact the V_{LOADx} (voltage on LOADx pin) is forced to the forward voltage of the integrated clamp diodes. The connection by a Zener or TVS allows to drive loads requiring fast current decay (fast demagnetization). For the proper selection of the external Zener or TVS, please refer to Section 7.1 Fast current decay with TVS between VZ and supply rail and Section 7.2 Fast current decay with TVS between VZ and PGND

Note: Leaving VZ pins floating, the integrated output voltage clamp is activated and the fast current decay capability is limited by the heatsink capability of the IC. See E_{AS} in Table 2. Absolute maximum ratings.

2.4 IN1, IN2, IN3, IN4

These pins drive the power stage on pins LOAD1, LOAD2, LOAD3 and LOAD4. Besides an internal weak pull-down resistor (see Iinx in Table 7. Logic inputs), each IN1, IN2, IN3, IN4, is internally wired to an open drain transistor, used for diagnostic purposes, and must be driven through a series resistor. The open drain transistor is turned-on in case of thermal shutdown or cut-off protection of the relative channel (see Section 6.2 Overtemperature and Section 6.3 Current limitation and cut-off).

2.5 LOAD1, LOAD2, LOAD3, LOAD4

Power stage load connection pins: integrated power transistor are in low-side configuration, so the load has to be connected between LOADx pin and supply rail. The power stage channels can be paralleled.

2.6 Open load in off-state

$\overline{OL}$ pin is used for diagnostic purpose and it is internally wired to an open drain transistor. If the open load feature is enabled (see Section 6.4 Open load in off-state) the open drain transistor is activated when LOADx is in off state and the open load threshold (VOLoff) is triggered (see Table 8. Protection and diagnostic).

2.7 FLT

This pin is used for diagnostic purpose and it is internally wired to an open drain transistor. The open drain transistor is turned on in case of junction thermal shutdown or during the cut-off protection.

2.8 ILIM

This pin cannot be left floating and can be used to program the limitation current value through an external resistor (R_{ILIM}) see Table 8. Protection and diagnostic. The resistor R_{ILIM} has to be connected between ILIM and SGND pins. When the IPS4260L ICs are used in the same application, their ILIM pins cannot be wired together: each IC must be connected to its own resistor (see Section 6.3 Current limitation and cut-off)

2.9 CoD

This pin cannot be left floating and can be used to program the cut-off delay time t_{coff} (see Table 8. Protection and diagnostic) through an external resistor (R_{CoD}). The resistor RCoD has to be connected between CoD and SGND pins. The cut-off function can be completely disabled by shorting CoD pin to SGND: in this condition the power stage channel remains ON in limitation condition, supplying the current to the load until the input is forced LOW or the thermal shutdown threshold is triggered (see Section 6.3 Current limitation and cut-off)

3 Absolute maximum ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage	-0.3 to 55	V
V_Z	Internal clamp diode supply	-0.3 to 55	V
V_{LOADx}	Power stage (LOADx channel) voltage	-0.3 to V_{DEMAG}	V
V_{INx}	INx pin voltage	-0.3 to 5.5	V
I_{INx}	INx pin current	-10 to +10	mA
V_{COD}, V_{ILIM}	CoD and ILIM pin voltage	5.5	V
I_{COD}, I_{ILIM}	CoD and ILIM pin current	-1/+5	mA
V_{OD}	Open drain fault pins (FLT and OL) voltage	-0.3 to 5.5	V
I_{OD}	Open drain fault pins (FLT and OL) current	-10/10	mA
I_{CC}	Maximum DC reverse current (from GND to V_{CC})	-250	mA
I_{LOADHx}	Power stage (LOADx channel) current	Internally limited	A
$-I_{LOADHx}$	Reverse current on LOADx channel	5	A
E_{AS}	Single pulse avalanche energy per channel not simultaneously @T_{AMB}= 125 °C, I_{LOAD} = 500 mA, VZ pins floating	0.9	J
P_{TOT}	Power dissipation at T_C = 25 °C	Internally limited	W
T_{STG}	Storage temperature range	-55 to 150	°C
T_J	Junction temperature	-40 to 150	°C

Note: Absolute maximum ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied. All voltages are referenced to GND.

Table 3. Thermal data

Symbol	Termal resistance	Conditions	Value	Unit
$RTH_{(JA)}$	Junction to ambient	2s2p (4L) board Natural convection(1)	43	°C/W
$RTH_{(J-C)}$	Junction to case	Cold plate (infinite headsink like)(2)	3	°C/W

1. *JESD51-7.*
2. *JESD51-12.01*

4 Electrical characteristics

(8 V < V_{CC} < 50 V; -40 °C < T_J < 125 °C, unless otherwise specified)

Table 4. Supply

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{CC}	Operating voltage range		V_{UVON}		50	V
V_{UVON}	Undervoltage on threshold	V_{CC} increasing	7		8	V
V_{UVOFF}	Undervoltage off threshold	V_{CC} decreasing	6.5		7.5	V
V_{UVH}	Undervoltage hysteresis		0.2	0.5		V
I_S	Supply current in off-state	V_{CC} = 24 V(all INx OFF)		1		mA
		V_{CC} = 50 V(all INx OFF)		1.2	1.6	
	Supply current in on-state	V_{CC} = 24 V all INx ON, LOADx open load [x = 1..4]		2		mA
		V_{CC} = 50 V all INx ON, LOADx open load [x = 1..4]		2.4	3	

Table 5. Output stage

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$R_{DS(on)}$	On-state resistance	R_{LOAD} = 48 Ω, V_{CC} = 24 V @ T_J = 25 °C		260		mΩ
		R_{LOAD} = 48 Ω, V_{CC} = 24 V @ T_J = 125 °C			560	
$V_{OUT(OFF)}$	Off-state power stage voltage	V_{IN} = 0 V and I_{LOAD} = 0 A	V_{CC}-2			V
$I_{OUT(OFF)}$	Off-state power stage current	V_{IN} = 0 V, V_{LOAD} = V_{CC} = 24 V		0.5		µA
		V_{IN} = 0 V, V_{LOAD} = V_{CC} = 50 V			10	
V_{FCD}	Catch diodes forward voltage	$I_{forward}$ = 500uA	0.21	0.50	0.73	V
I_{RRM}	Catch diodes reverse current	V_{rrm}= 55V			1	uA

Table 6. Switching (V_{CC} = 24 V; R_{LOAD} = 24 Ω, input rise time < 0.1 µs)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
t_r	Rise time	see fig 3 : trise and tfall and fig 4 tPD(L-H) and tPD(H-L)		450	700	ns
t_f	Fall time			500	600	
$t_{PD(H-L)}$	Propagation delay time INx to LOADx, low to high			500	700	
$t_{PD(L-H)}$	Propagation delay time INx to LOADx, high to low			400	600	

Figure 3. t_{rise} and t_{fall}

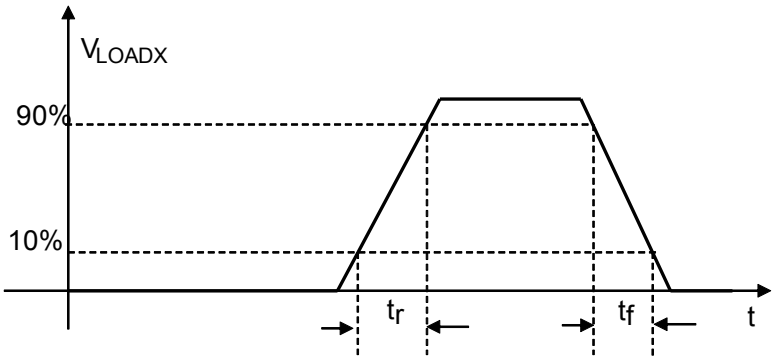


Figure 4. $t_{PD(L-H)}$ and $t_{PD(H-L)}$

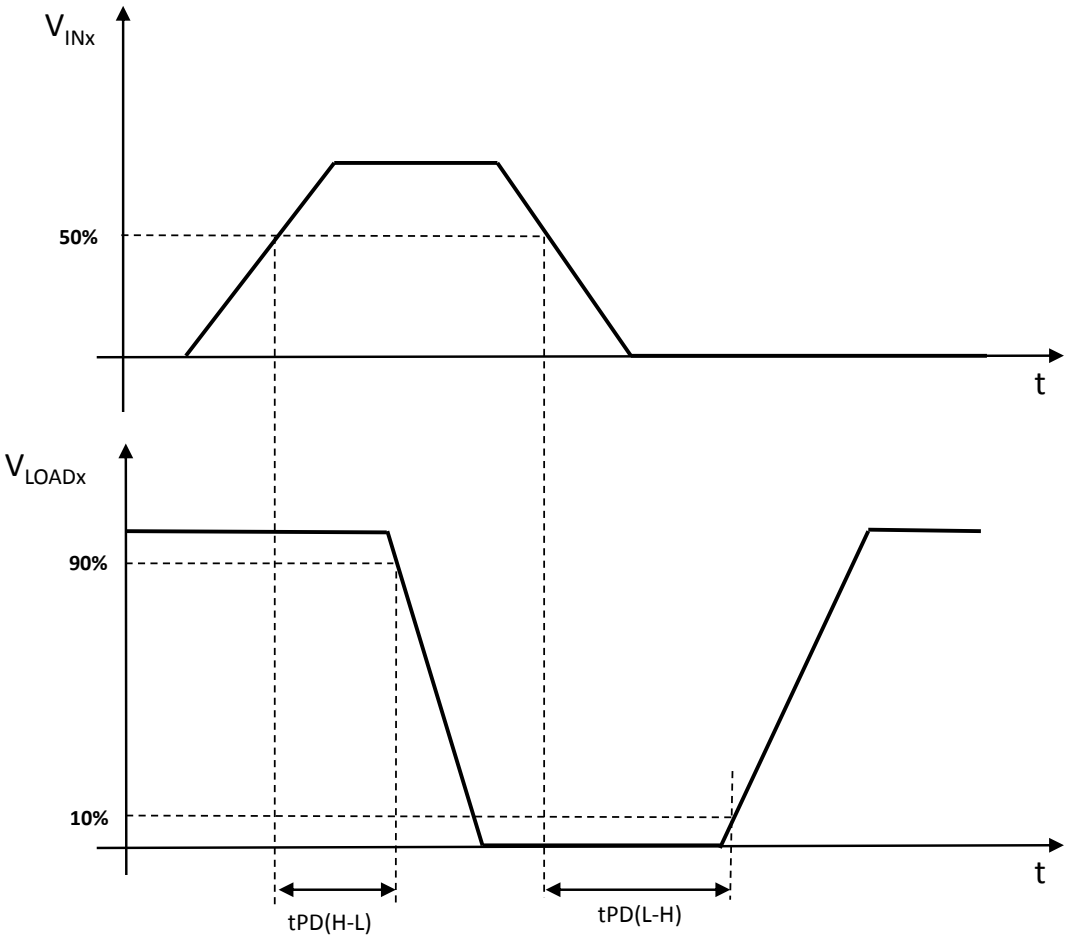


Table 7. Logic inputs

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{IL}	Input low level voltage	V_{IN} decreasing			0.8	V
V_{IH}	Input high level voltage	V_{IN} increasing	2.0			
$V_{I(HYST)}$	Input hysteresis voltage			0.4		
V_{OL}	Voltage drop on OL pin	I_{OL} = 5 mA V_{INx} = 0 V, OUTx = open load, R_{PD} between OUTx and GND			0.1	

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{FAULT}	Voltage drop on FAULT pin or INx pin	I_{FLT} = 5 mA V_{INx} = 0 V, (T_{JX} > T_{JSD} or cut-off event)			0.1	V
I_{INX}	All digital input/output pin current	V_{IN} = 5 V			70	µA

Table 8. Protection and diagnostic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{clamp}	V_{CC} clamp voltage	I_{CC} ≤ 10 mA	55	58	60	V
V_{demag}	Demagnetization voltage	I_{OUT} = 0.5 A; load ≥10 mH	55	58	60	
I_{peak}	Current limitation activation threshold.	I_{LOAD} increasing from 0A to short circuit.		I_{LIM} +20%		A
I_{LIM}	Current limitation level	30 kΩ ≤ R_{ILIM} < 120 kΩ	$60/R_{ILIM}$[kΩ] ± 30%			A
		0 < R_{ILIM} < 30 kΩ	3 ± 30%			
t_{coff}	Cut-off current delay time	Programmable by external resistor on "cut-off" pin (valid in the range from 60 kΩ to 240 kΩ).	R_{CoD}[kΩ]/120 ± 15%			ms
		R_{CoD}= 0 Ω cut-off disabled	The IC is protected against overheating by the thermal shutdown only.			
t_{res}	Power stage restart delay time		$31*t_{coff}$± 15%			ms
t_{BKT}	Open load blanking time		12.0	16.5	21	µs
I_{VD}	Vcc wire break power stage current	V_{INx} = V_{CC} =0 V; V_{LOADx} = 24 V, V_Z floating			50	µA
T_{JSD}	Junction temperature shutdown			160		°C
T_{JHYST}	Junction temperature thermal hysteresis			20		°C
V_{OLoff}	Open load (off-state) or short-to-ground detection threshold		Vcc-4.5	Vcc-3.5	Vcc-2.5	V

5 Power stage logic

Table 9. Power stage (LOADx pin) truth table

Operation	MCU_OUTx	INx	LOADx	$\overline{FLT}$	$\overline{OL}$
Normal	L	L	H	H	H
	H	H	L	H	H
Cut-off	L	L	H	L	H
	H	L	H	L	H
UVLO	L	L	H	X	X
	H	H	H	X	X
Open load/short-to-GND	L	L	L	H	L
	H	H	L	H	H
Overtemperature	L	L	H	L	H
	H	L	H	L	H

Figure 5. Application circuit (fast decay enabled by TVS between Vz and supply rail)

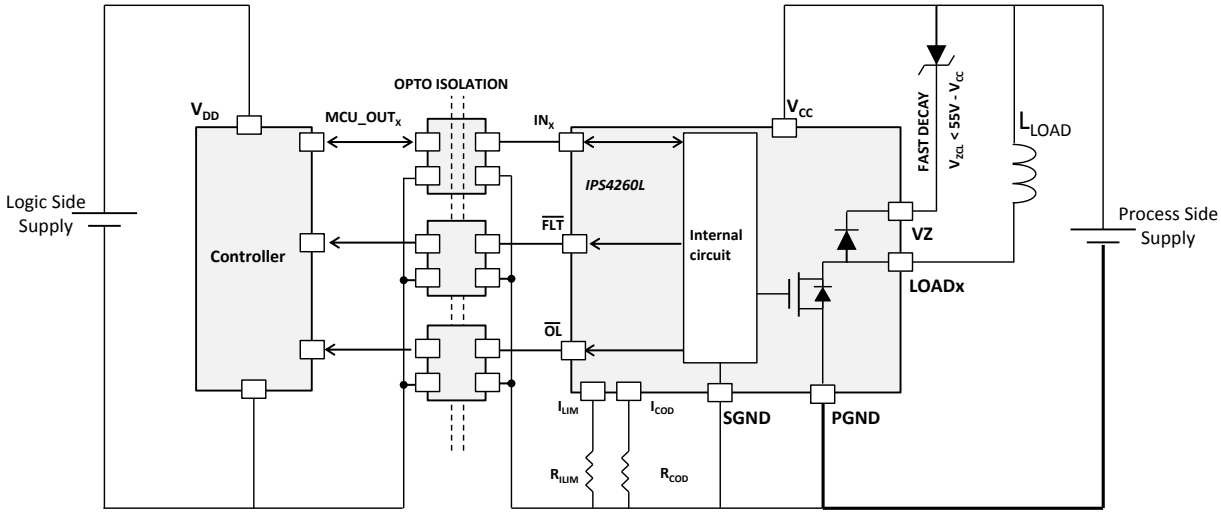


Figure 6. **Application circuit (fast decay enabled by TVS between VZ and PGND).**

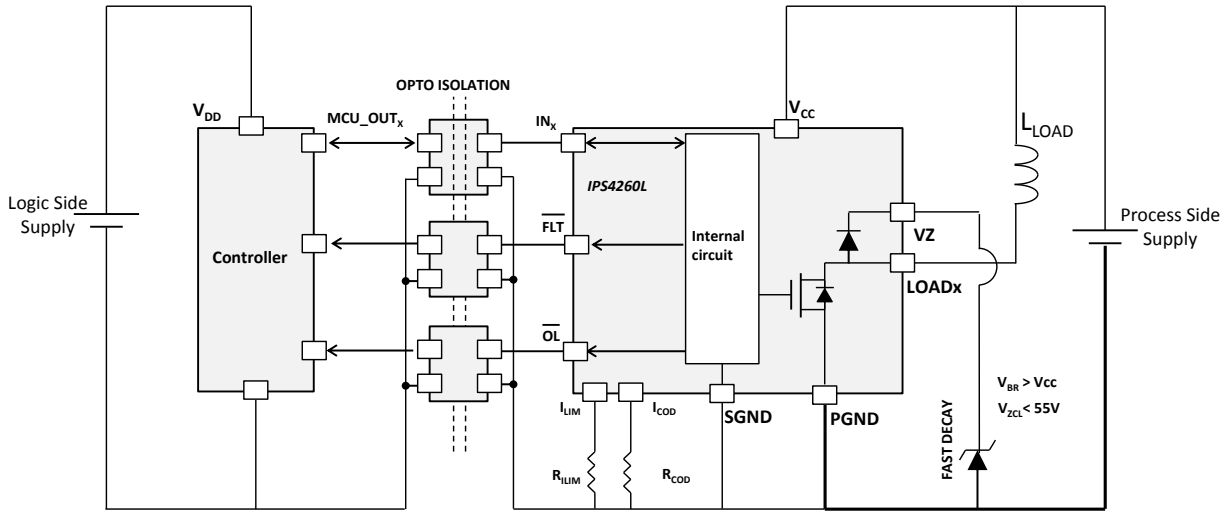
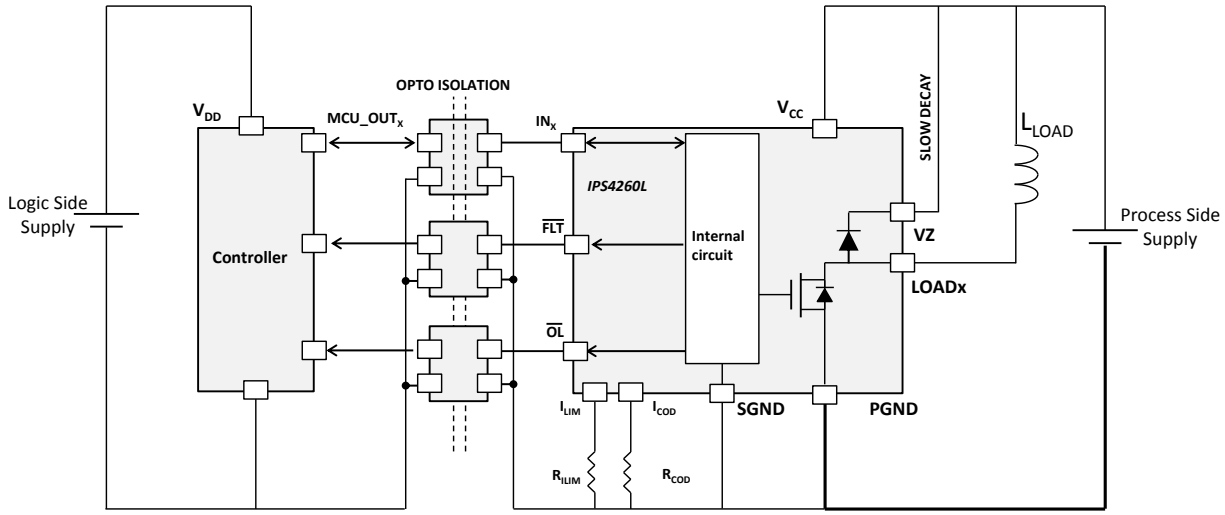


Figure 7. **Application circuit (fast decay disabled by Vz shorted to supply rail) .**



6 Protection and diagnostic

The IC integrates several protections to ease the design of a robust application.

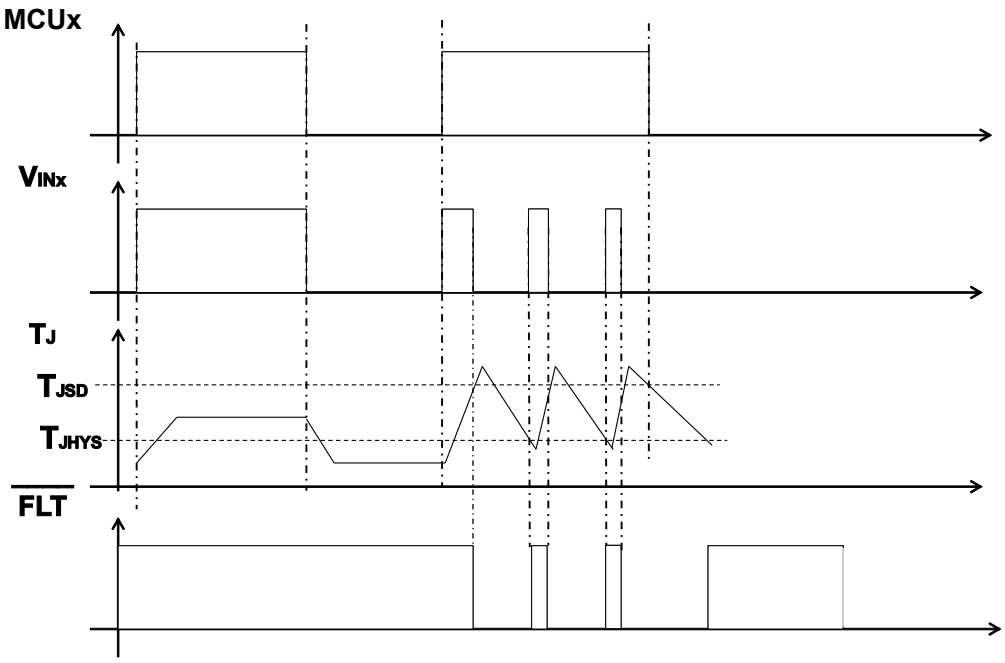
6.1 Undervoltage lock-out

The device turns off if the supply voltage falls below the turn-off threshold ($V_{UV(off)}$). Normal operation restarts after V_{CC} exceeds the turn-on threshold ($V_{UV(on)}$). Turn-on and turn-off thresholds are defined in Table 4. Supply.

6.2 Overtemperature

The power stage of each channel is turned off as its internal junction temperature (T_J) exceeds the shutdown threshold (T_{JSD}). Normal operation restarts when T_J comes back below the reset threshold (see Table 8. Protection and diagnostic). The internal fault signal is set when the channel is OFF due to thermal protection. The thermal fault is reported both on the FLT pin and on the INx pin of the corresponding LOADx in fault. Note that the FLT pin reports the logic OR of the four output channels faults.

Figure 8. Thermal protection signalization behavior on $\overline{FLT}$



6.3 Current limitation and cut-off

The load current flows through the integrated power stage and it is internally limited by the specific I_{LIM} threshold that can be set by an external resistor (R_{ILIM}) placed between I_{LIM} and SGND ground plane. The design rule for the R_{ILIM} resistor is:

Equation 1:

$$I_{LIM} = 60/R_{ILIM}[k\Omega] \quad (1)$$

The above design rule is valid in the range 30 kΩ ≤ R_{ILIM} ≤ 120 kΩ. For 0 ≤ R_{ILIM} < 30 kΩ, the current is internally limited up to 3 A (typical). For R_{ILIM} > 120 kΩ the current is anyway limited but the linearity is not guaranteed.

The IPS4260L implements the cut-off feature which limits the duration of the current limitation condition. The duration of the current limitation condition (T_{coff}) can be set by a resistor (R_{CoD}) placed between CoD and SGND ground plane. The design rule for RCoD is:

Equation 2:

(2)

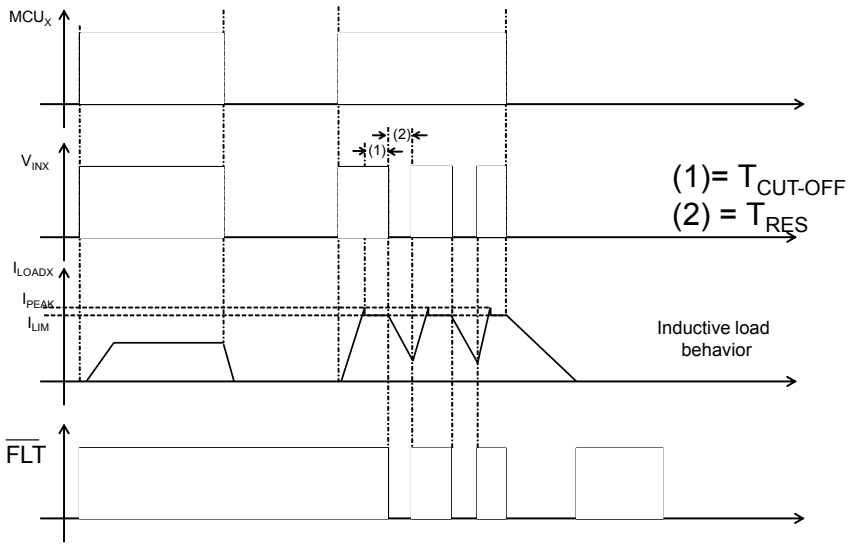
$T_{coff} = R_{CoD}[k\Omega]/120$

The above design rule is valid in the range 60 kΩ ≤ R_{CoD} ≤ 240 kΩ. As 0 < R_{CoD} < 60 kΩ, T_{coff} anyway decreases but the linearity of the above design rule is not guaranteed. As R_{CoD} = 0 Ω (short-to-ground plane) the cut-off feature is disabled, by means the IC is protected by thermal shutdown only. Concerning R_{CoD} > 240 kΩ, T_{coff} increases but linearity of equation 2 is not guaranteed.

In case I_{LIM} threshold is triggered, the power stage remains in the current limitation condition (I_{LOADx} = I_{LIM}) at least for t_{coff}. When t_{coff} elapses, the power stage is turned off and restarted after the t_{res} restart time. The fault condition is reported both on $\overline{FLT}$ pin and on the input pin (INx) corresponding to the channel in fault. The internal cut-off flag signal is latched at power stage switch-off and released after the time t_{res}. The same behavior is reported on $\overline{FLT}$ pin and on the INx pins related to the LOADx in fault. If one of the four channels is in overload protection, the other channels (in operating conditions) work properly. The status of $\overline{FLT}$ is independent of the INx pin status, and is low during the whole cut-off time (t_{res}). The same behavior has to be respected on fault signals on input pins.

If CoD pin is shorted to SGND ground plane (cut-off feature disabled) then the output channel remains ON, in current limitation condition, until the related input becomes LOW or the thermal protection threshold is triggered.

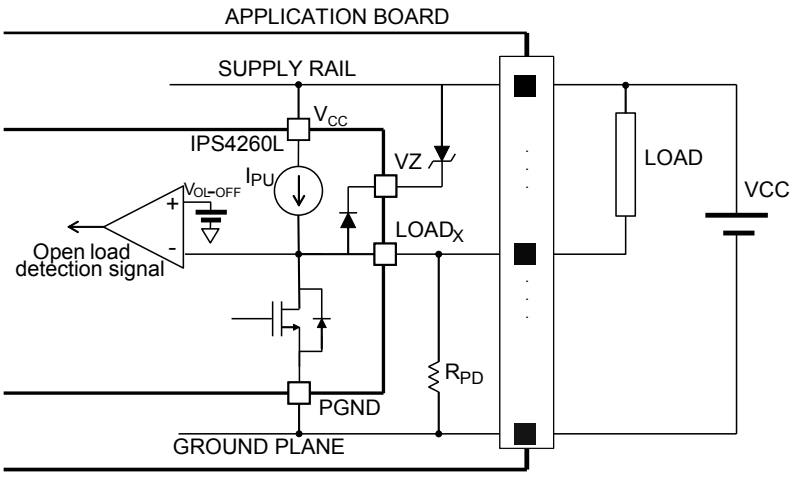
Figure 9. Cut-off signalization behavior on $\overline{FLT}$



6.4 Open load in off-state

The IPS4260L provides the open load detection feature, which detects if the load is disconnected (wire break) from the LOADx pin when in OFF-state (INx = LOW). This feature can be activated by placing a proper resistor (R_{PD}) between LOADx and PGND ground plane.

Figure 10. **Open load off-state**



The voltage on LOADx pin (V_{LOADx}) is internally compared with the V_{OLOFF} threshold: if the related INx pin is LOW and the V_{LOADX} goes lower than V_{OLOFF} then the open load condition is triggered. The fault condition is reported on the $\overline{OL}$ pin and the fault reset occurs when load is reconnected. If the channel is switched ON by the related INx pin, the fault condition is no longer detected.

In OFF state, the IPS4260L achieves the open load detection feature by forcing the internally generated current I_{PU} (= 20 µA) on the external pull-down resistor R_{PD}. The following design rule has to be followed in order to set the proper value of R_{PD}:

Equation 3:

$$R_{PD} < \frac{V_{OLOFF}(\min)}{I_{PU}} = \frac{V_{CC} - 4.5}{I_{PU}} \quad (3)$$

Note: When the load is connected the open load detection threshold must not be triggered:

Equation 4:

$$V_{LOADX} = V_{CC} * \frac{R_{PD}}{(R_{PD} + R_{LOAD})} > V_{OLOFF}(\max) \quad (4)$$

Therefore:

Equation 5:

$$R_{PD} > R_{LOAD} * \left[\frac{V_{OLOFF}(\max)}{(V_{CC} - V_{OLOFF}(\max))} \right] \quad (5)$$

*Note: if two or more channels are parallelized then R_{PD} must be calculated according to the n*Ipu (e.g. in case of 4 channels in parallel the total Ipu becomes 80uA).*

6.5 GND wire break protection

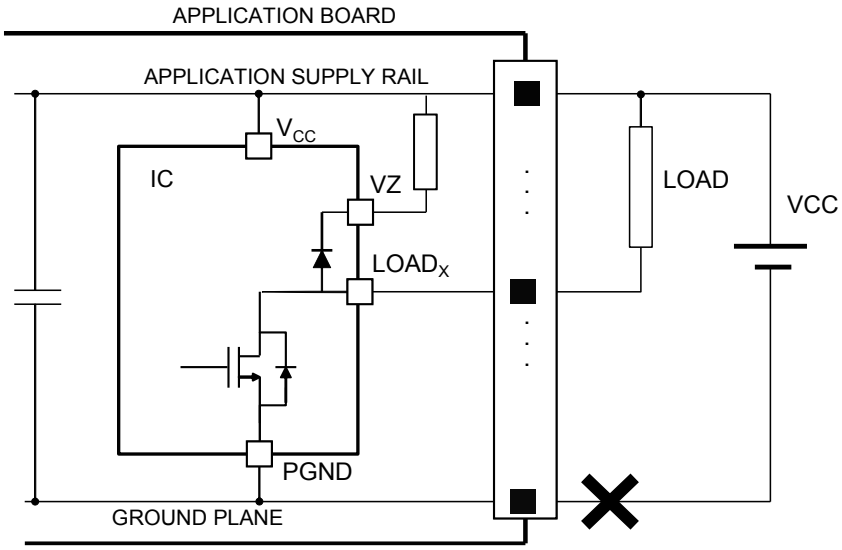
GND wire break is intended as the disconnection event of the application board ground (where both SGND and PGND signals are connected) from the system ground of the external supply rail (see fig 11 GND wire break, where the shape between VZ and supply rail represents one of the application configurations: open circuit, short circuit or an external TVS).

When this event happens, the supply voltage at Vcc pin decreases until Vuvoff is triggered and then all power stages are turned off independently of the input status.

In case of inductive load, if the ground disconnection event happens while one or more channels are active:

- in case of Vz pins floating, the residual current in the inductor flows through the integrated power switch, which is activated by active clamp as if the input had been deactivated.
- in case of Vz pins connected to supply rail (by short circuit or by TVS), the residual current in the inductor flows through the catch diodes. Similarly, the catch diodes allows the proper ground disconnection protection even in case of Vz pins connected by a TVS to ground layer.

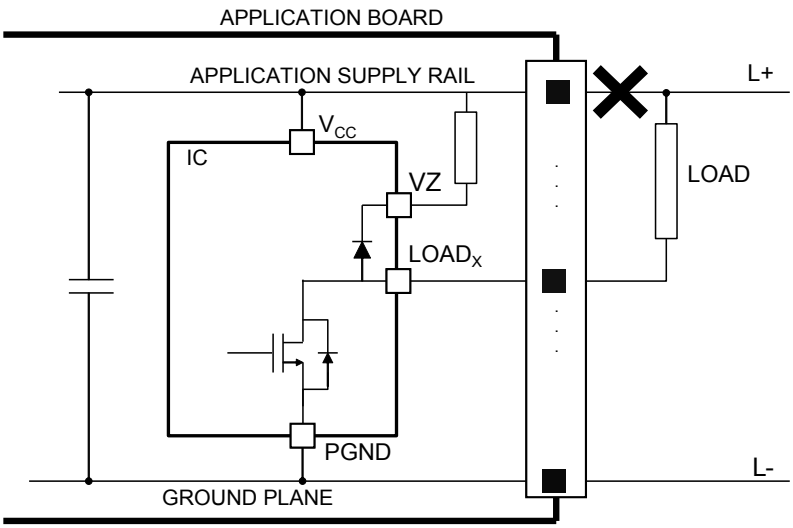
Figure 11. GND wire break



6.6 VCC wire break protection

VCC wire break is intended as the disconnection of the application board form rail supply (see Figure 13. VCC wire break , where the shape between VZ and supply rail represents one of the application configurations: open circuit, short circuit or an external TVS). When this condition is detected, all power stage channels are turned off independently of the input status. The maximum steady-state current measured through a channel in short to the supply voltage is not greater than I_{VD} (see Table 7. Logic inputs). The same behavior is guaranteed when all channels are simultaneously in short to the supply voltage. In case of inductive load, if the V_{cc} is disconnected while one or more channels are active, the current flows through the power, which is activated by the active clamp as if the input had been deactivated.

Figure 12. VCC wire break



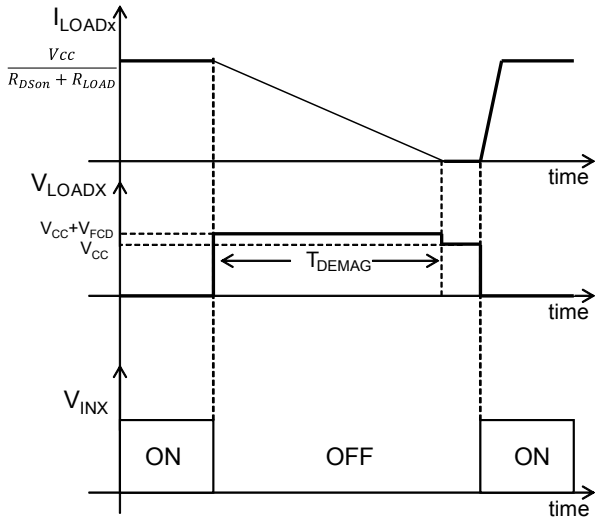
VCC wire break protection is guaranteed when VZ floats or when VZ is connected to GND by a proper TVS, while it is limited (see below) when VZ is shorted to V_{CC}.

If VZ is connected to V_{CC} by a TVS (with clamping voltage = V_{CL}), then V_{CC} wire break protection is limited by the following design rule: $V_{CL} > V_L + - (V_{LOAD}+V_D+V_{UVLO})$.

7 Active clamp

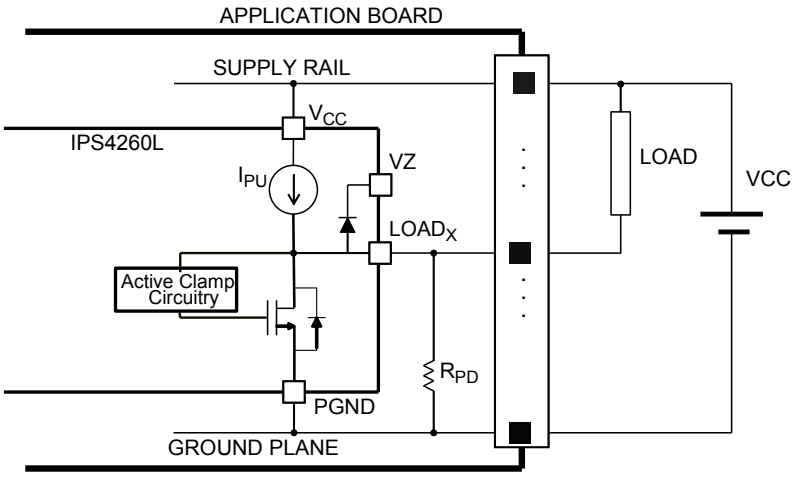
Active clamp is also known as fast demagnetization of inductive loads or fast current decay. When a low-side driver turns off an inductance, an overvoltage on load is detected. If VZ pins are directly shorted to the supply rail (see fig 7 Application circuit (fast decay disabled by Vz shorted to supply rail) .) then the fast current decay is disabled: the inductive load is demagnetized slowly and according to the forward voltage of the integrated clamp diodes (V_{FCD}). The figure below shows the typical waveforms of the load voltage and current in case of slow demagnetization.

Figure 13. V_{LOAD} and I_{LOAD} in case of slow demagnetization



If VZ pins are left floating (see fig 14 Active clamp equivalent principle schematic.) or connected by a Zener or TVS diode to supply rail (see fig 5 Application circuit (fast decay enabled by TVS between Vz and supply rail)) or PGND (see fig 6 Application circuit (fast decay enabled by TVS between VZ and PGND). then the fast decay is activated. When VZ pins are left floating the integrated clamping circuit protects the IC despite overvoltages: the conduction state of the integrated switches is modulated in order to keep the LOADx pin voltage < V_{demag} until the energy in the load has been dissipated. The demagnetization energy is dissipated in the IC and it is limited by the internal heatsink capability, see E_{AS} in Table 2. Absolute maximum ratings .

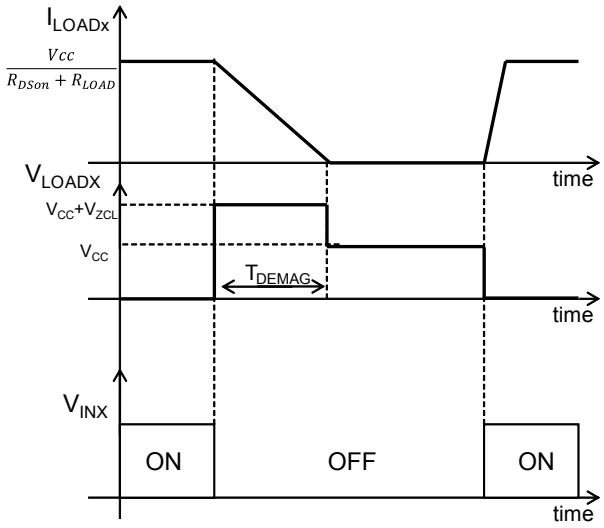
Figure 14. Active clamp equivalent principle schematic.



7.1 Fast current decay with TVS between VZ and supply rail

Being V_{CLZ} the clamping voltage of the external TVS, when the inductive load is turned off the LOADx pin is pulled up to V_{CC}+V_{CLZ}. In order to avoid any damage to the IPS4260L, the external diode must be selected such that V_{CLZ} < ($V_{DEMAG(MIN)}$ – V_{CC}). Furthermore, the external diode must be selected such that it is able to dissipate the power due to the demagnetization currents flowing from the active channels.

Figure 15. V_{LOAD} and I_{LOAD} in case of fast demagnetization (fast decay)



7.2 Fast current decay with TVS between VZ and PGND

Being V_{CLZ} the clamping voltage of the external TVS, when the inductive load is turned off the LOADx pin is clamped by the lower voltage between V_{CLZ} and $V_{DEMAG(MIN)}$. In order to avoid any leakage currrent on the external TVS has to be selected such that its V_{BR} results > V_{CC}, while in order to avoid any damage to the IPS4260L the V_{CLZ} of the external TVS must be selected such that V_{CLZ} < $V_{DEMAG(MIN)}$. Further, the external diode must be selected such that it is able to dissipate the power due to the demagnetization currents flowing from the active channels.

8

8.1 HTSSOP20 package information

Figure 16. **HTSSOP20 package outline**

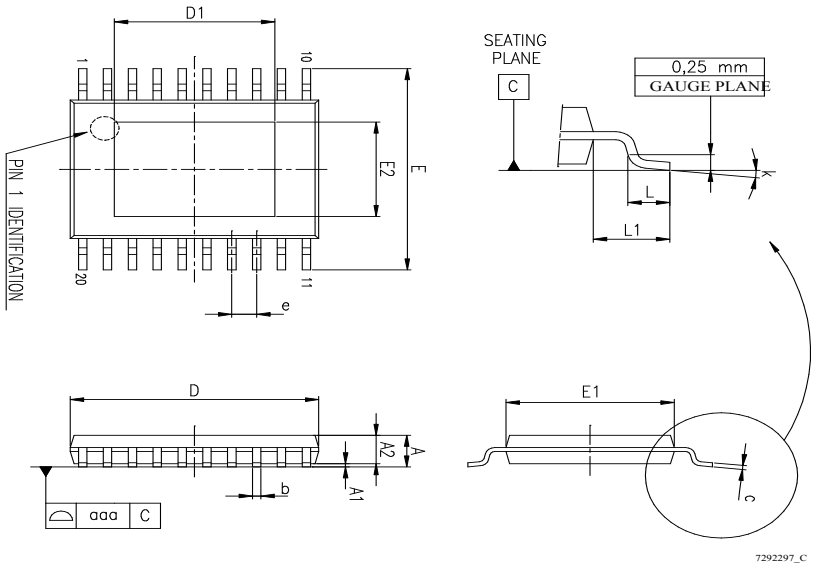


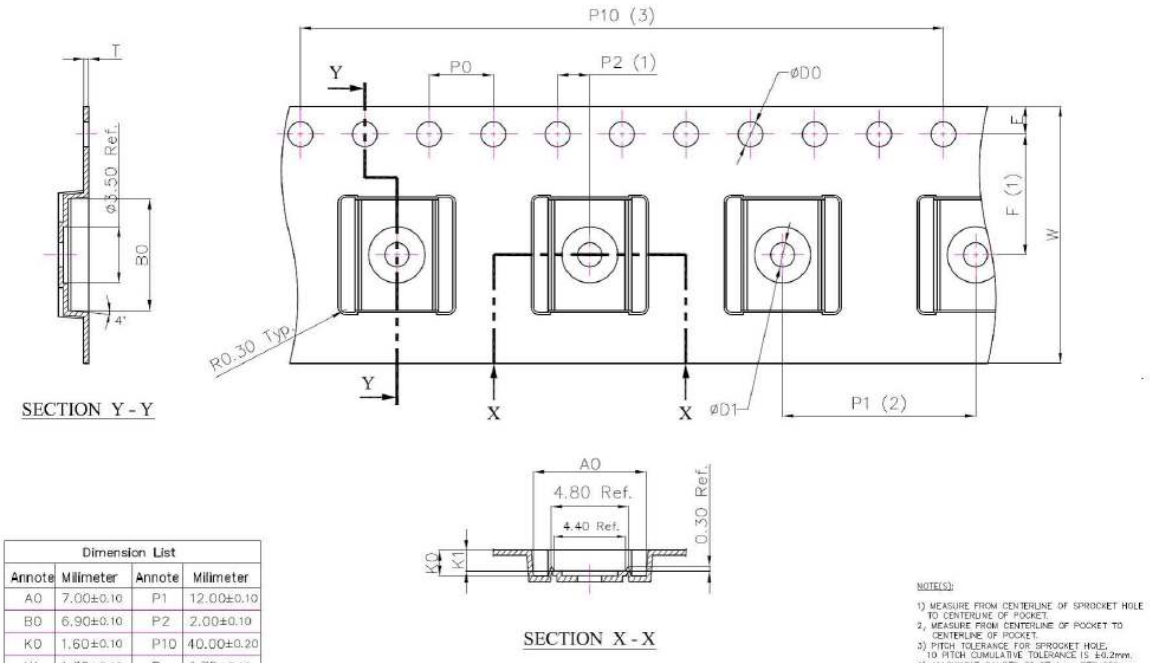
Table 10. **HTSSOP20 mechanical data**

Dim.	mm			inch		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.2			0.047
A1			0.15		0.004	0.006
A2	0.8	1	1.05	0.031	0.039	0.041
b	0.19		0.30	0.007		0.012
c	0.09		0.20	0.004		0.0089
D	6.4	6.5	6.6	0.252	0.256	0.260
D1	4.1	4.2	4.3	0.161	0.165	0.169
E	6.2	6.4	6.6	0.244	0.252	0.260
E1	4.3	4.4	4.5	0.169	0.173	0.177
E2	2.9	3.0	3.1	0.114	0.118	0.122
e		0.65			0.0256	
K	0°		8°	0°		8°
L	0.45	0.60	0.75	0.018	0.024	0.030

9 Packaging information

9.1 HTSSOP20 packaging information

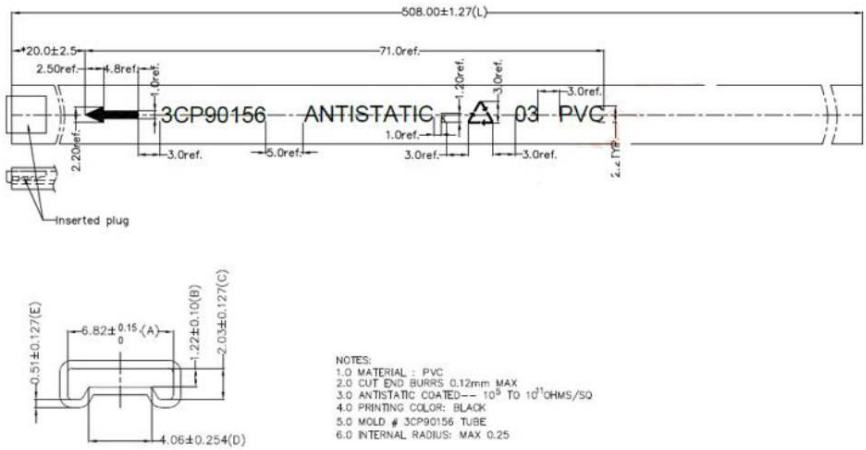
Figure 17. **Carrier Tape for HTSSOP20 20L**



Dimension List			
Annote	Millimeter	Annote	Millimeter
A0	7.00±0.10	P1	12.00±0.10
B0	6.90±0.10	P2	2.00±0.10
K0	1.60±0.10	P10	40.00±0.20
K1	1.30±0.10	E	1.75±0.10
D0	$1.50^{+0.10}_{-0}$	F	7.50±0.10
D1	$1.50^{+0.10}_{-0}$	W	16.00±0.30
P0	4.00±0.10	T	0.30±0.05

NOTE(S):
1) MEASURE FROM CENTERLINE OF SPROCKET HOLE TO CENTERLINE OF POCKET.
2) MEASURE FROM CENTERLINE OF POCKET TO CENTERLINE OF POCKET.
3) PITCH TOLERANCE FOR SPROCKET HOLE: 10 PITCH CUMULATIVE TOLERANCE IS ±0.2mm.
4) ALLOWABLE CAMBER TO BE 1mm PER 250mm IN LENGTH.

Figure 18. **HTSSOP20 Shipping Tube**



10 Ordering information

Table 11. **Ordering information**

Order code	Package	Packing
IPS4260L	HTSSOP20	Tube
IPS4260LTR		Tape and reel

Revision history

Table 12. **Document revision history**

Date	Revision	Changes
02-Oct-2017	1	Initial release.
20-Sep-2019	2	Modified Table 3. Thermal data, Features update () , Minor text updates inside Description , Rephrased Section 2.3 VZ , Rephrased Section 2.6 Open load in off-state, Updated Typ. in Table 5. Output stage, Updated Max. in Table 6. Switching (V_{CC} = 24 V; R_{LOAD} = 24 Ω, input rise time < 0.1 µs), Tcoff and IVD updated in Table 8. Protection and diagnostic , Rephrased Section 6.2 Overtemperature, Updated Equation 3: Equation 4: Equation 5: Added fig 18 HTSSOP20 Shipping Tube .
06-Apr-2020	3	Modified Table 4. Supply, Table 5. Output stage, Table 8. Protection and diagnostic, minor text updates inside the document.
29-Jun-2020	4	Correct thermal data values in Table 3
30-Jul-2021	5	Updated section Section 6.4 Open load in off-state

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