

FSUSB30

Low-Power, Two-Port, High-Speed USB 2.0 (480Mbps) Switch

Features

- ? Low On Capacitance: 3.7pF (Typical)
- ? Low On Resistance: 6.5Ω (Typical)
- ? Low Power Consumption: 1μA (Maximum)
 - 10μA Maximum I_{CCT} over an Expanded Control Voltage Range ($V_{IN} = 2.6V$, $V_{CC} = 4.3V$)
- ? Wide -3dB Bandwidth, >720MHz
- ? 8KV ESD Protection
- ? Power-Off Protection when $V_{CC} = 0V$; D+/D- Pins can Tolerate up to 5.5V
- ? Packaged in:
 - 10-lead MicroPak™ (1.6 x 2.1mm)
 - 14-lead DQFN
 - 10-lead MSOP
 - 10-lead UMLP (1.4 x 1.8mm)

Applications

- ? Cell phone, PDA, Digital Camera, and Notebook LCD Monitor, TV, and Set-top Box

Related Application Notes

- ? AN-6022 Using the FSUSB30 / FSUSB31 to Comply with USB 2.0 Fault Condition Requirements

Description

The FSUSB30 is a low-power, two-port, high-speed USB 2.0 switch. Configured as a double-pole double-throw (DPDT) switch, it is optimized for switching between two high-speed (480Mbps) sources or a Hi-Speed and Full-Speed (12Mbps) source. The FSUSB30 is compatible with the requirements of USB2.0 and features an extremely low on capacitance (C_{ON}) of 3.7pF. The wide bandwidth of this device (720MHz), exceeds the bandwidth needed to pass the third harmonic, resulting in signals with minimum edge and phase distortion. Superior channel-to-channel crosstalk minimizes interference.

The FSUSB30 contains special circuitry on the D+/D- pins which allows the device to withstand an overvoltage condition when powered off. This device is also designed to minimize current consumption even when the control voltage applied to the S pin, is lower than the supply voltage (V_{CC}). This feature is especially valuable to ultra-portable applications such as cell phones, allowing for direct interface with the general purpose I/Os of the baseband processor. Other applications include switching and connector sharing in portable cell phones, PDAs, digital cameras, printers, and notebook computers.

Ordering Information

Order Number	Package Number	Product Code Top Mark	Package Description
FSUSB30L10X	MAC010A	FJ	10-Lead MicroPak, 1.6 x 2.1mm
FSUSB30BQX	MLP014A	USB30	14-Terminal Depopulated Quad Very-Thin Flat Pack No Leads (DQFN), JEDEC MO-241, 2.5 x 3.0mm
FSUSB30MUX	MUA10A	FSUSB30	10-Lead Molded Small Outline Package (MSOP), JEDEC MO-187, 3.0mm Wide
FSUSB30UMX	MLP010A	GJ	10-Lead, Quad, Ultrathin, MLP (UMLP) 1.4 x 1.8mm

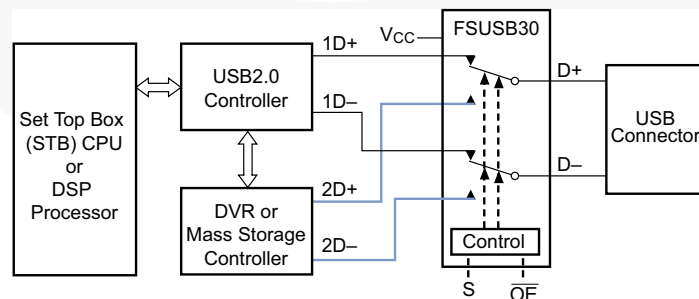
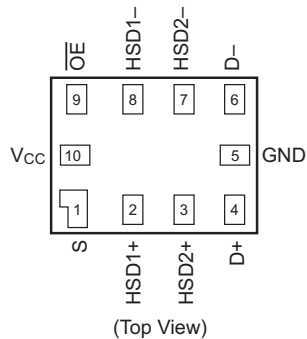


Figure 1. Typical Application

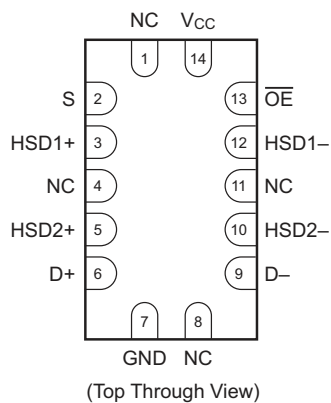
MicroPak™ is a trademark of Fairchild Semiconductor Corporation.

Connection Diagrams

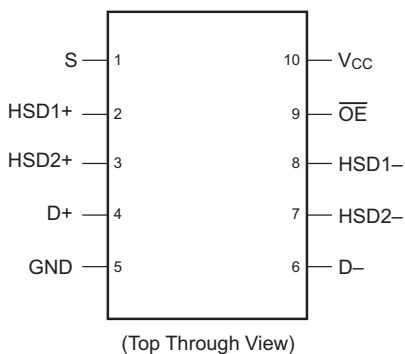
Pad Assignments for MicroPak



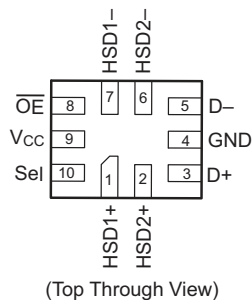
Pad Assignments for DQFN



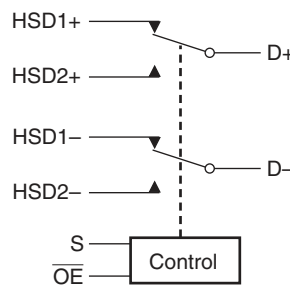
Pin Assignment for MSOP



Pad Assignments for μ MLP



Analog Symbol



Pin Descriptions

Pin Name	Description
\overline{OE}	Bus Switch Enable
S	Select Input
D+, D-, HSDn+, HSDn-	Data Ports
NC	No Connect

Truth Table

S	\overline{OE}	Function
X	HIGH	Disconnect
LOW	LOW	D+, D- = HSD1 _n
HIGH	LOW	D+, D- = HSD2 _n

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter	Minimum	Maximum	Unit	
V_{CC}	Supply Voltage	-0.5	+5.5	V	
V_{CNTRL}	DC Input Voltage ⁽¹⁾	-0.5	V_{CC}	V	
V_{SW}	DC Switch Voltage ⁽¹⁾	HSDnX	0.5	V_{CC}	V
		D+,D- when $V_{CC} > 0$	0.5	V_{CC}	V
		D+,D- when $V_{CC} = 0$	-0.50	V_{CC}	V
I_{IK}	DC Input Diode Current	-50		mA	
I_{OUT}	DC Output Current		50	mA	
T_{STG}	Storage Temperature	-65	+150	°C	
ESD	Human Body Model	All Pins		8	kV
		I/O to GND		8	kV

Note:

1. The input and output negative voltage ratings may be exceeded if the input and output diode current ratings are observed.

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to absolute maximum ratings.⁽²⁾

Symbol	Parameter	Minimum	Maximum	Unit
V_{CC}	Supply Voltage	3.0	4.3	V
V_{IN}	Control Input Voltage	0	V_{CC}	V
V_{SW}	Switch Input Voltage	0	V_{CC}	V
T_A	Operating Temperature	-40	+85	°C
Θ_{JA}	Thermal Resistance, 10 MicroPak		250	°C/W

Note:

2. Control input must be held HIGH or LOW and it must not float.

DC Electrical Characteristics

All typical values are at 25°C unless otherwise specified.

Symbol	Parameter	Conditions	V _{CC} (V)	T _A = -40°C to +85°C			Unit
				Min.	Typ.	Max.	
V _{IK}	Clamp Diode Voltage	I _{IN} = -18mA	3.0			-1.2	V
V _{IH}	Input Voltage HIGH		3.0 to 3.6	1.3			V
			4.3	1.7			V
V _{IL}	Input Voltage LOW		3.0 to 3.6			0.5	V
			4.3			0.7	V
I _{IN}	Control Input Leakage	V _{SW} = 0.0V to V _{CC}	4.3	-1.0		1.0	μA
I _{OZ}	OFF State Leakage	0 ≤ D _n , HSD1 _n , HSD2 _n ≤ V _{CC}	4.3	-2.0		2.0	μA
I _{OFF}	Power OFF Leakage Current (D+, D-)	V _{SW} = 0V to 4.3V, V _{CC} = 0V	0	-2.0		2.0	μA
R _{ON}	Switch On Resistance ⁽³⁾	V _{SW} = 0.4V, I _{ON} = -8mA	3.0		6.5	10.0	Ω
			3.6			7.0	Ω
ΔR _{ON}	Delta R _{ON} ⁽⁴⁾	V _{SW} = 0.4V, I _{ON} = -8mA	3.0		0.35		Ω
R _{ON} Flatness	R _{ON} Flatness ⁽³⁾	V _{SW} = 0.0V - 1.0V, I _{ON} = -8mA	3.0		2.0		Ω
I _{CC}	Quiescent Supply Current	V _{CNTRL} = 0.0V or V _{CC} , I _{OUT} = 0	4.3			1.0	μA
I _{CCT}	Increase in I _{CC} Current per Control Voltage	V _{CNTRL} (control input) = 2.6V	4.3			10.0	μA

Notes:

3. Measured by the voltage drop between D_n, HSD1_n, HSD2_n pins at the indicated current through the switch. On resistance is determined by the lower of the voltage on the two ports.
4. Guaranteed by characterization.

AC Electrical Characteristics

All typical values are for V_{CC} = 3.3V at 25°C unless otherwise specified.

Symbol	Parameter	Conditions	V _{CC} (V)	T _A = -40°C to +85°C			Unit	Figure Number
				Min.	Typ.	Max.		
t _{ON}	Turn-On Time S, OE to Output	HD1 _n , HD2 _n = 0.8V, R _L = 50Ω, C _L = 5pF	3.0 to 3.6		13	30	ns	Figure 9
t _{OFF}	Turn-Off Time S, OE to Output	HD1 _n , HD2 _n = 0.8V, R _L = 50Ω, C _L = 5pF	3.0 to 3.6		12	25	ns	Figure 9
t _{PD}	Propagation Delay ⁽⁴⁾	R _L = 50Ω, C _L = 5pF	3.3		0.25		ns	Figure 7 Figure 8
t _{BBM}	Break-Before-Make	R _L = 50Ω, C _L = 5pF, V _{IN} = 0.8V	3.0 to 3.6	2.0		6.5	ns	Figure 10
O _{IRR}	Off Isolation (Non-Adjacent)	f = 240MHz, R _T = 50Ω	3.0 to 3.6		-30		dB	Figure 13
Xtalk	Non-Adjacent Channel Crosstalk	R _T = 50Ω, f = 240MHz	3.0 to 3.6		-45		dB	Figure 14
BW	-3dB Bandwidth	R _T = 50Ω, C _L = 0pF	3.0 to 3.6		720		MHz	Figure 12
		R _T = 50Ω, C _L = 5pF			550			

USB Hi-Speed Related AC Electrical Characteristics

Symbol	Parameter	Conditions	V _{CC} (V)	T _A = -40°C to +85°C			Units	Figure Number
				Min.	Typ.	Max.		
t _{SK(O)}	Channel-to-Channel Skew ⁽⁵⁾	R _L = 50Ω, C _L = 5pF	3.0 to 3.6		50		ps	Figure 7 Figure 11
t _{SK(P)}	Skew of Opposite Transitions of the Same Output ⁽⁵⁾	R _L = 50Ω, C _L = 5pF	3.0 to 3.6		20		ps	Figure 7 Figure 11
t _J	Total Jitter ⁽⁵⁾	R _L = 50Ω, C _L = 5pF, t _R = t _F = 500ps at 480 Mbps (PRBS = 2 ¹⁵ - 1)	3.0 to 3.6		200		ps	

Note:

5. Guaranteed by characterization.

Capacitance

Symbol	Parameter	Conditions	T _A = -40°C to +85°C			Units	Figure Number
			Min.	Typ.	Max.		
C _{IN}	Control Pin Input Capacitance	V _{CC} = 0V		1.5		pF	Figure 16
C _{ON}	D1 _n , D2 _n , Dn On Capacitance	V _{CC} = 3.3, \overline{OE} = 0V		3.7		pF	Figure 15
C _{OFF}	D1 _n , D2 _n Off Capacitance	V _{CC} and \overline{OE} = 3.3		2.5		pF	Figure 16

Typical Characteristics

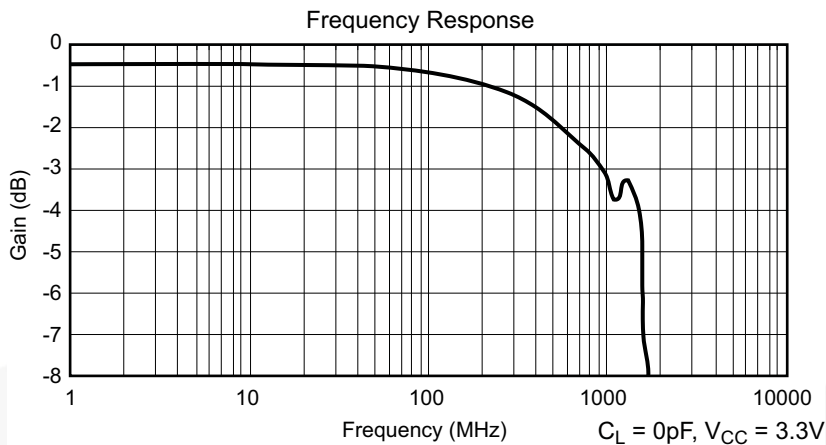


Figure 2. Gain vs. Frequency

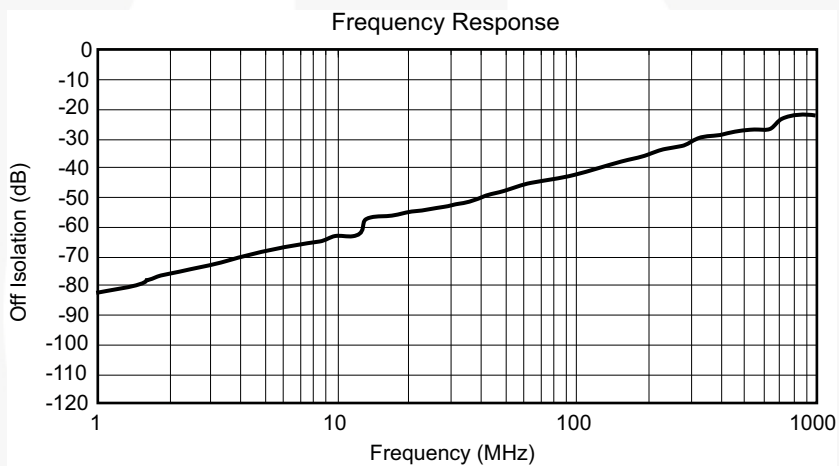


Figure 3. Off Isolation

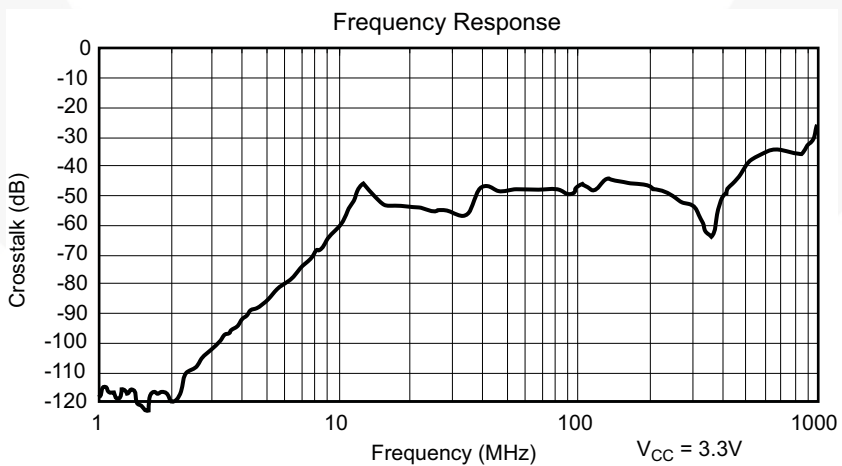


Figure 4. Crosstalk

Test Diagrams

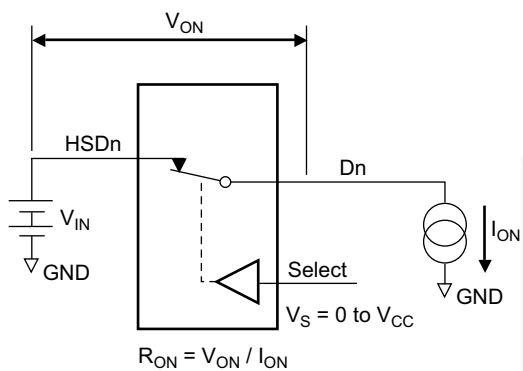
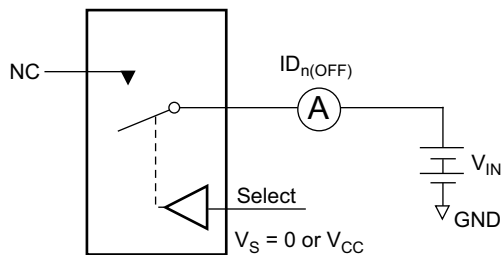
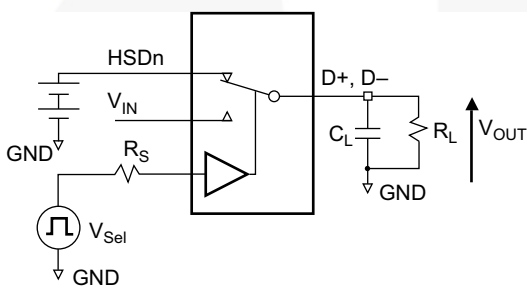


Figure 5. On Resistance



Each switch port is tested separately.

Figure 6. Off Leakage



R_L , R_S , and C_L are functions of the application environment (see AC Electrical tables for specific values).

C_L includes test fixture and stray capacitance.

Figure 7. AC Test Circuit Load

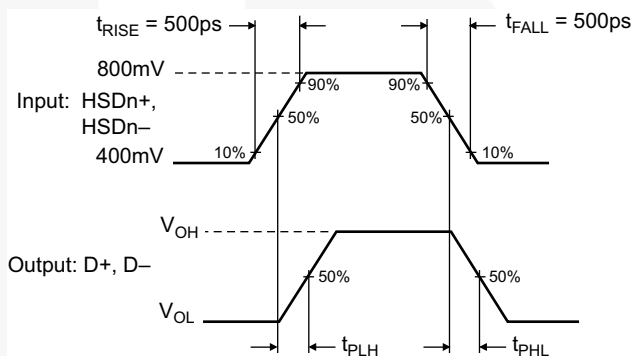


Figure 8. Switch Propagation Delay Waveforms

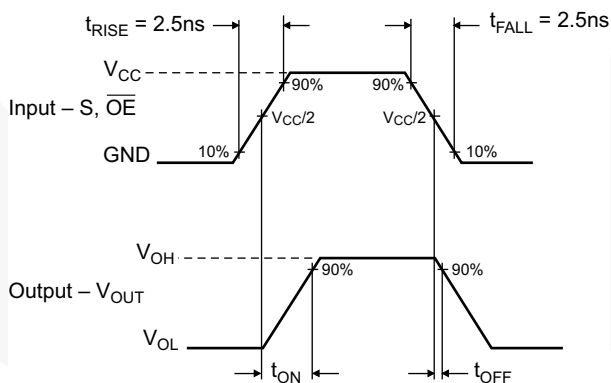
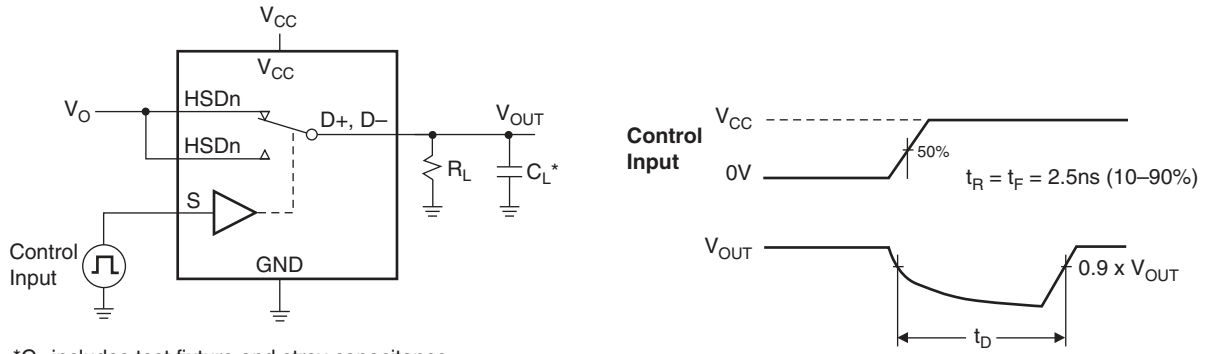
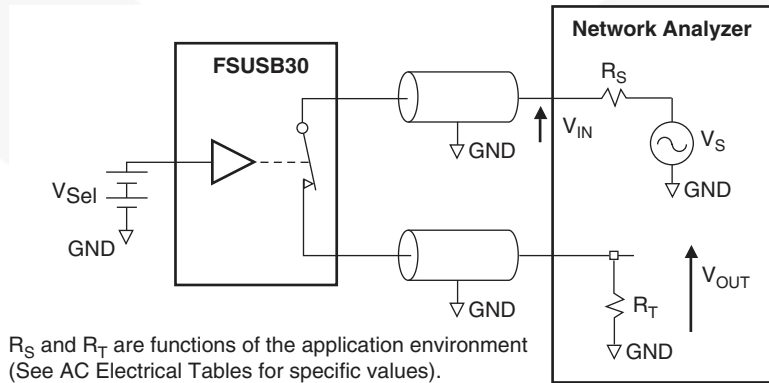
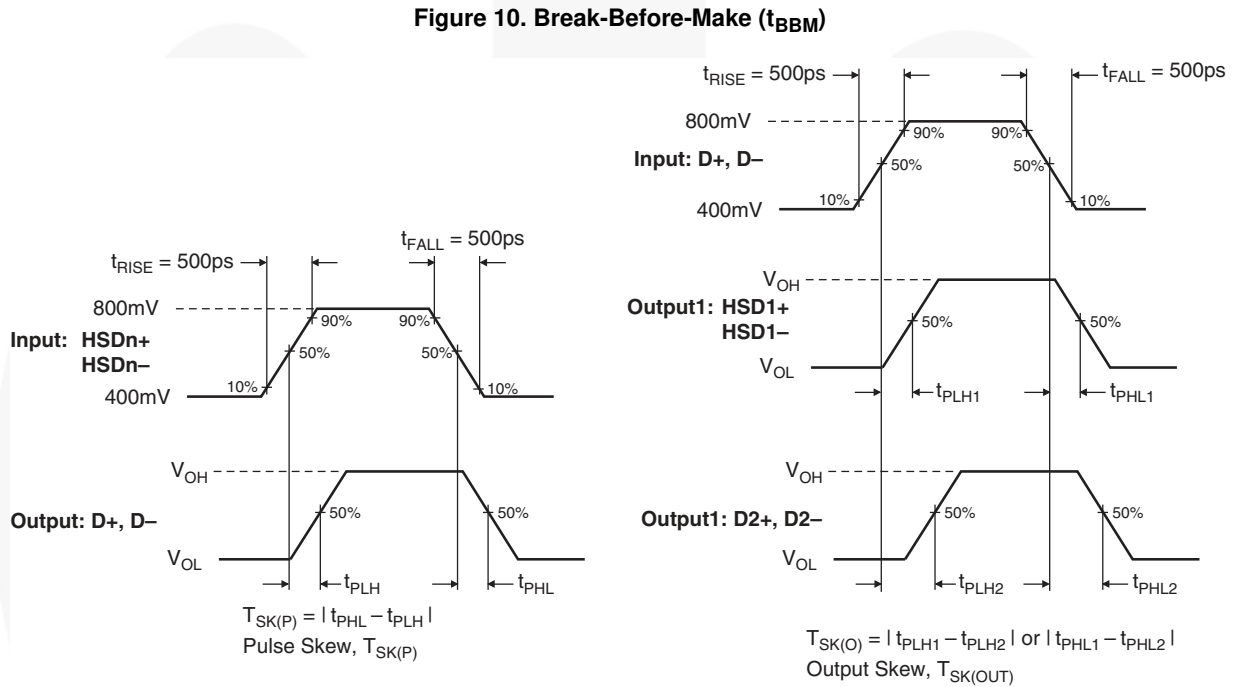


Figure 9. Turn-On / Turn-Off Waveform



* C_L includes test fixture and stray capacitance.



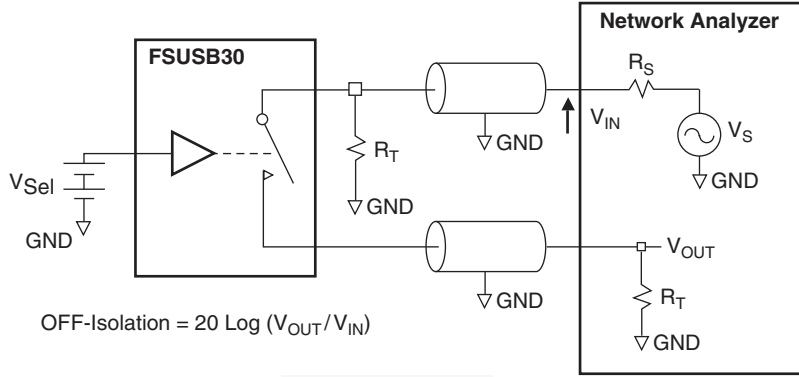


Figure 13. Channel Off Isolation

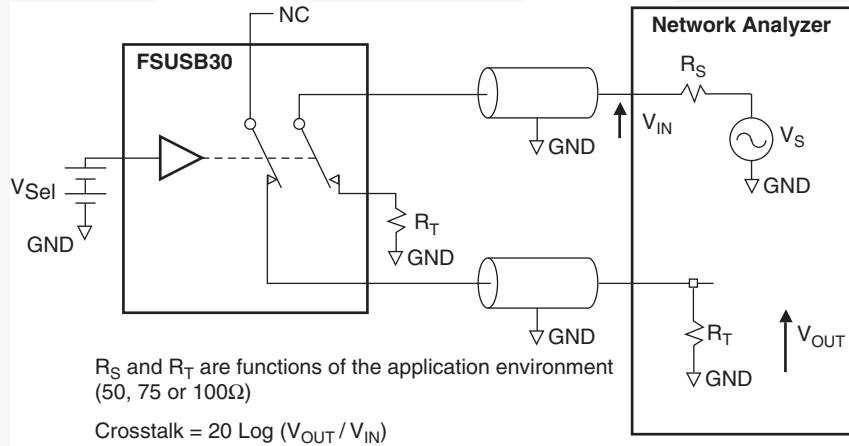


Figure 14. Non-Adjacent Channel-to-Channel Crosstalk

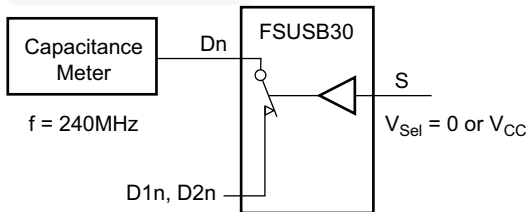


Figure 15. Channel On Capacitance

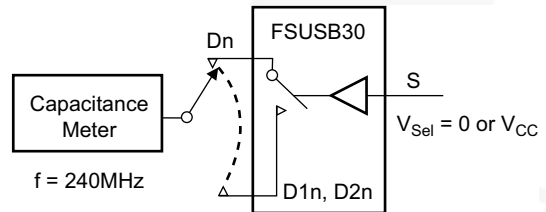


Figure 16. Channel Off Capacitance

Application Guidance: Meeting USB 2.0 Vbus Short Requirements

In section 7.1.1 of the USB 2.0 specification, it notes that USB devices must be able to withstand a Vbus short to D+ or D- when the USB devices is either powered off or powered on. The FSUSB30 can be successfully configured to meet both these requirements.

Power-Off Protection

For a Vbus short circuit, the switch is expected to withstand such a condition for at least 24 hours. The FSUSB30 has specially designed circuitry which prevents unintended signal bleed through as well as guaranteed system reliability during a power-down, over-voltage condition. The protection has been added to the common pins (D+, D-).

Power-On Protection

The USB 2.0 specification also notes that the USB device should be capable of withstanding a Vbus short during transmission of data. Fairchild recommends adding a 100Ω series resistor between the switch VCC pin and supply rail to protect against this case. This modification works by limiting current flow back into the V_{CC} rail during the over-voltage event so current remains within the safe operating range. In this application, the switch passes the full 5.25V input signal through to the selected output, while maintaining specified off isolation on the un-selected pins.

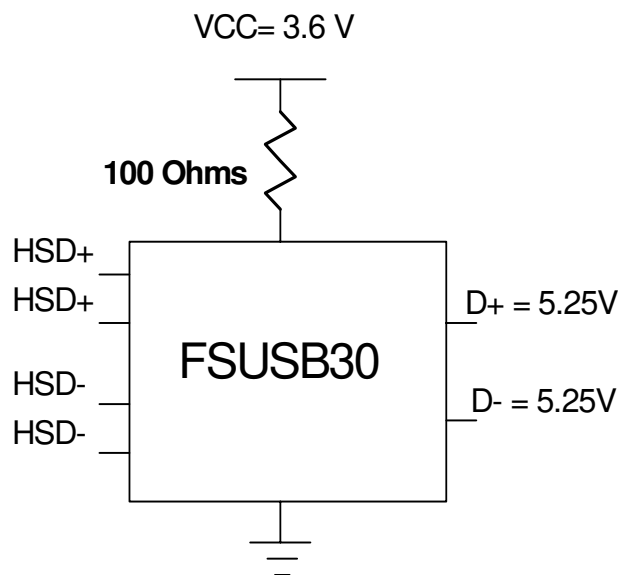


Figure 17. Adding 100Ω resistor in series with the V_{CC} supply allows the FSUSB30 to withstand a Vbus short when powered up

For more information, see Applications Note *AN-6022 Using the FSUSB30 to Comply with USB 2.0 Fault Condition Requirements* at www.fairchildsemi.com

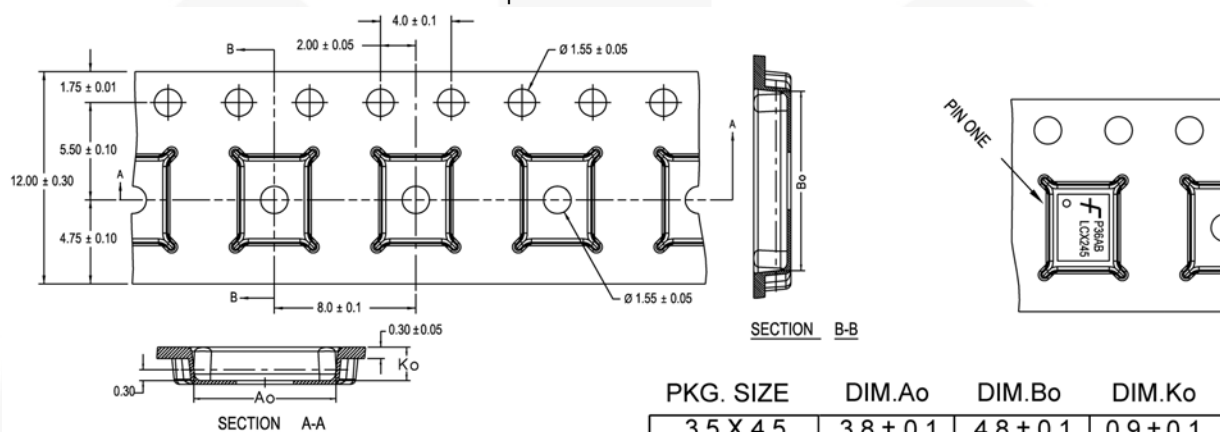
Tape and Reel Specifications

Tape Format for DQFN

Package Designator	Tape Section	Number Cavities	Cavity Status	Cover Tape Status
BQX	Leader (Start End)	125 (typ)	Empty	Sealed
	Carrier	2500/3000	Filled	Sealed
	Trailer (Hub End)	75 (typ)	Empty	Sealed

Tape Dimensions

Dimensions are in millimeters unless otherwise specified.



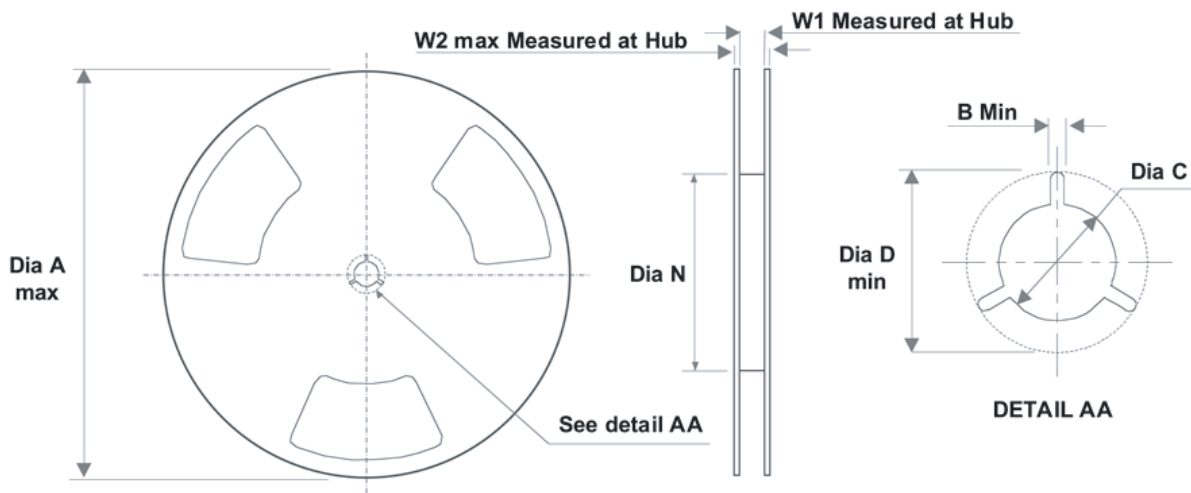
DIMENSIONS ARE IN MILLIMETERS

NOTES: unless otherwise specified

1. Cumulative pitch for feeding holes and cavities (chip pockets) not to exceed 0.008[0.20] over 10 pitch span.
2. Smallest allowable bending radius.
3. Thru hole inside cavity is centered within cavity.
4. Tolerance is ±0.002[0.05] for these dimensions on all 12mm tapes.
5. Ao and Bo measured on a plane 0.120[0.30] above the bottom of the pocket.
6. Ko measured from a plane on the inside bottom of the pocket to the top surface of the carrier.
7. Pocket position relative to sprocket hole measured as true position of pocket. Not pocket hole.
8. Controlling dimension is millimeter. Dimension in inches rounded.

Reel Dimensions for DQFN

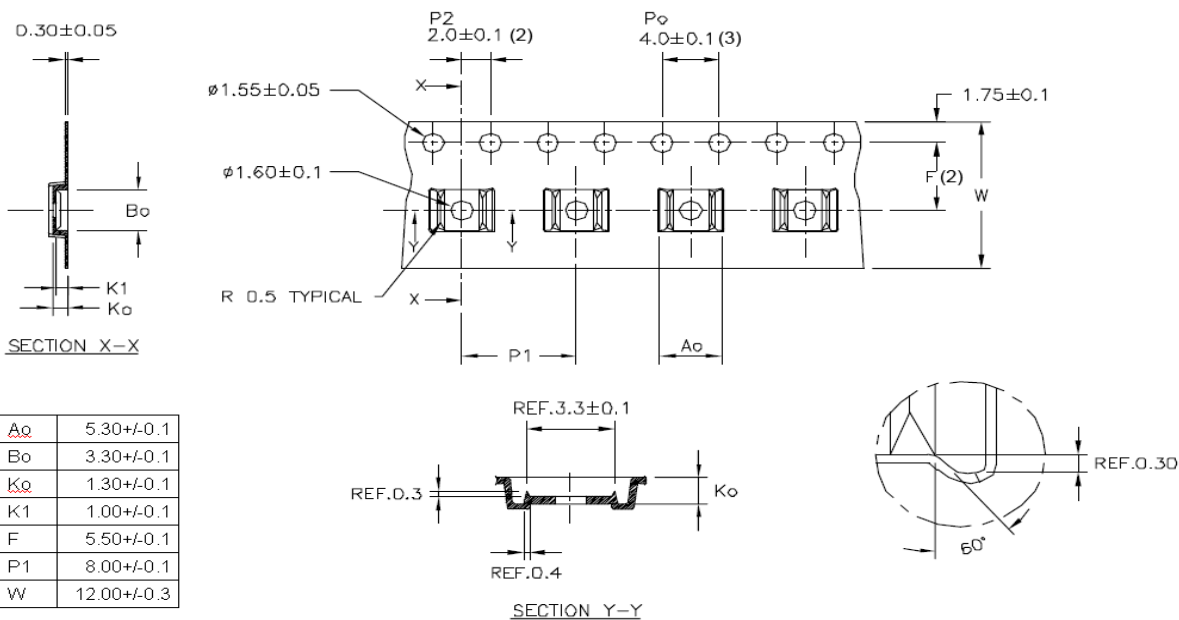
Dimensions are in inches (millimeters) unless otherwise specified.



Tape Size	A	B	C	D	N	W1	W2
(12mm)	13.0 (330)	0.059 (1.50)	0.512 (13.00)	0.795 (20.20)	7.008 (178)	0.488 (12.4)	0.724 (18.4)

Tape Dimensions for MSOP

Dimensions are in inches (millimeters) unless otherwise specified.



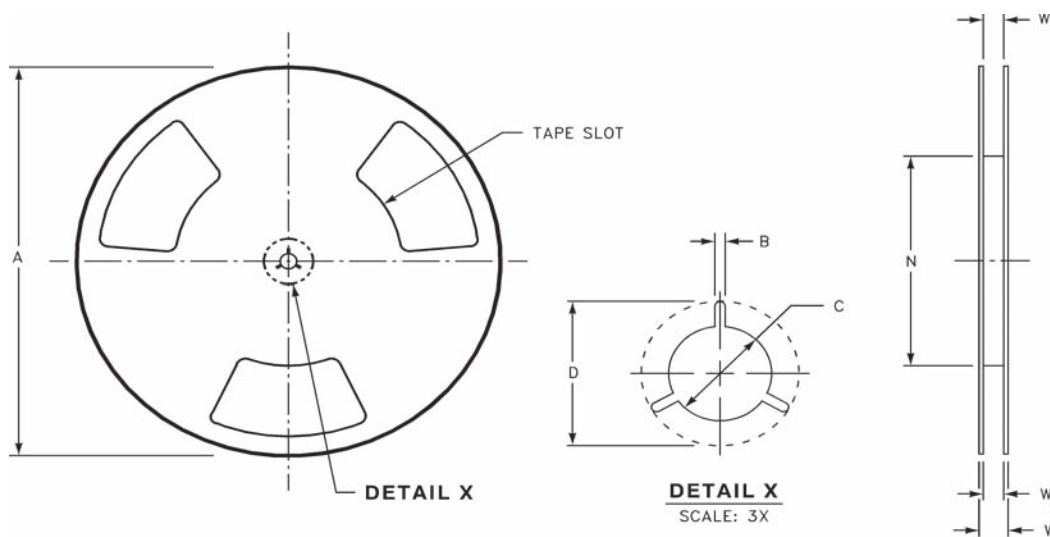
A ₀	5.30±0.1
B ₀	3.30±0.1
K ₀	1.30±0.1
K ₁	1.00±0.1
F	5.50±0.1
P ₁	8.00±0.1
W	12.00±0.3

Notes:

1. All dimensions are in millimeters.
2. Measured from centerline of sprocket hole to centerline of pocket.
3. Cumulative tolerance of ten sprocket holes is ±0.20mm.
4. Other material available.

Reel Dimensions for MSOP

Dimensions are in inches (millimeters) unless otherwise specified.



Tape Size	A	B	C	D	N	W1	W2	W3
(12mm)	13 (330)	0.059 (1.5)	0.512 (13)	0.795 (20.2)	7.008 (178)	0.448 (12.4)	0.724 (18.4)	0.468-0.606 (11.9 -15.4)

Physical Dimensions

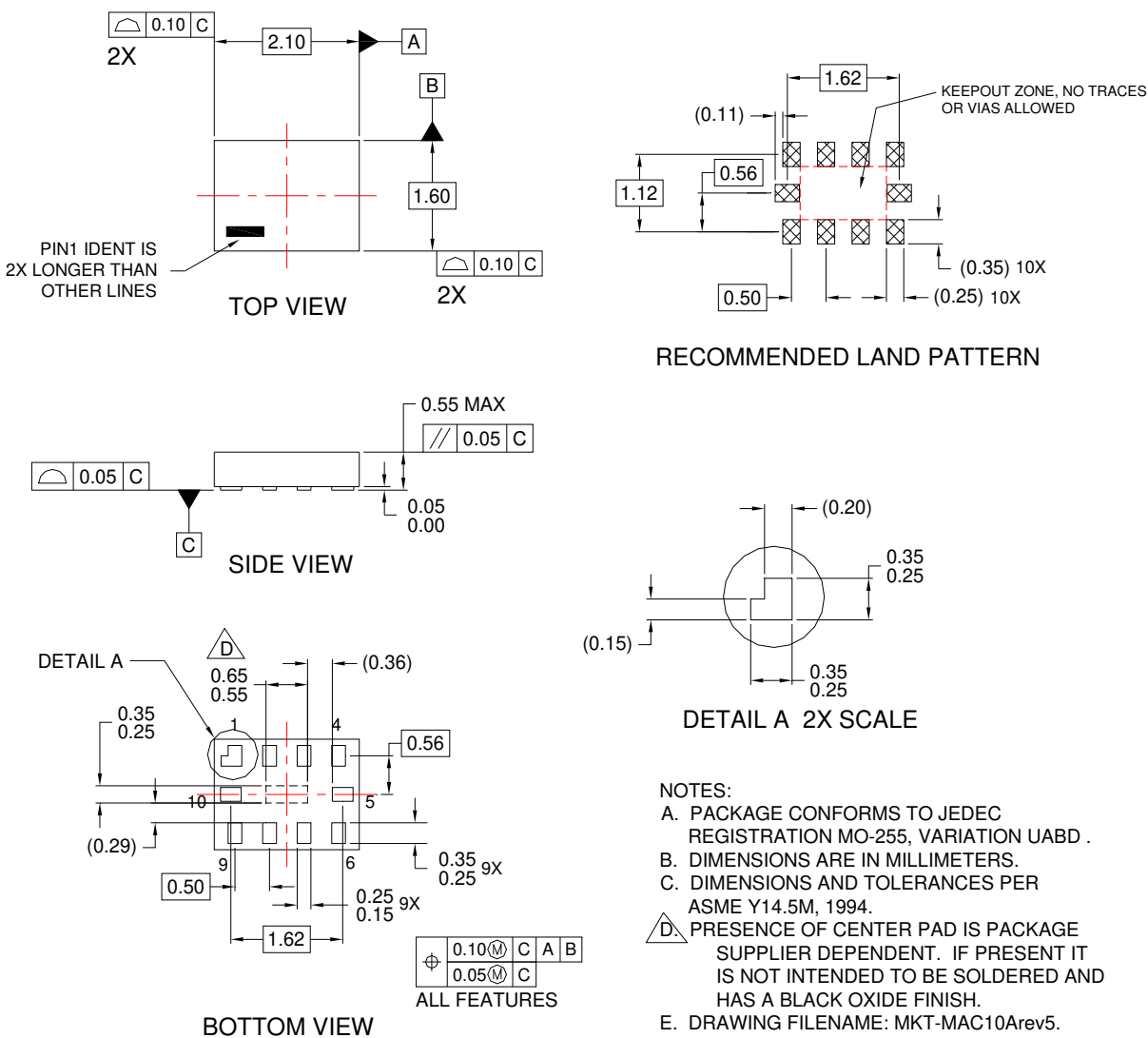


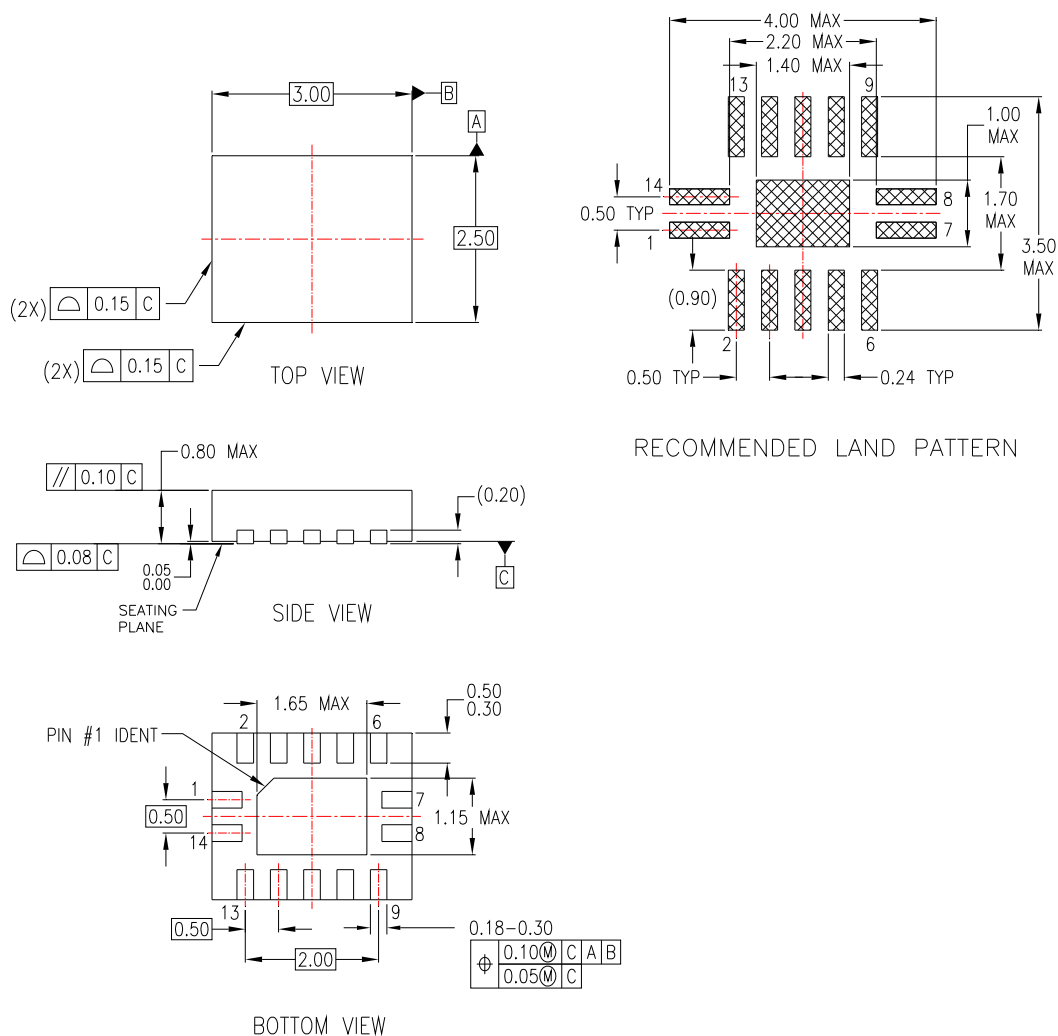
Figure 17. 10-Lead MicroPak, 1.6 x 2.1mm

For tape and reel specifications, visit Fairchild's website: http://www.fairchildsemi.com/products/logic/pdf/micropak_tr.pdf.

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Physical Dimensions



NOTES:

- A. CONFORMS TO JEDEC REGISTRATION MO-241, VARIATION AA
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994

MLP14ArevA

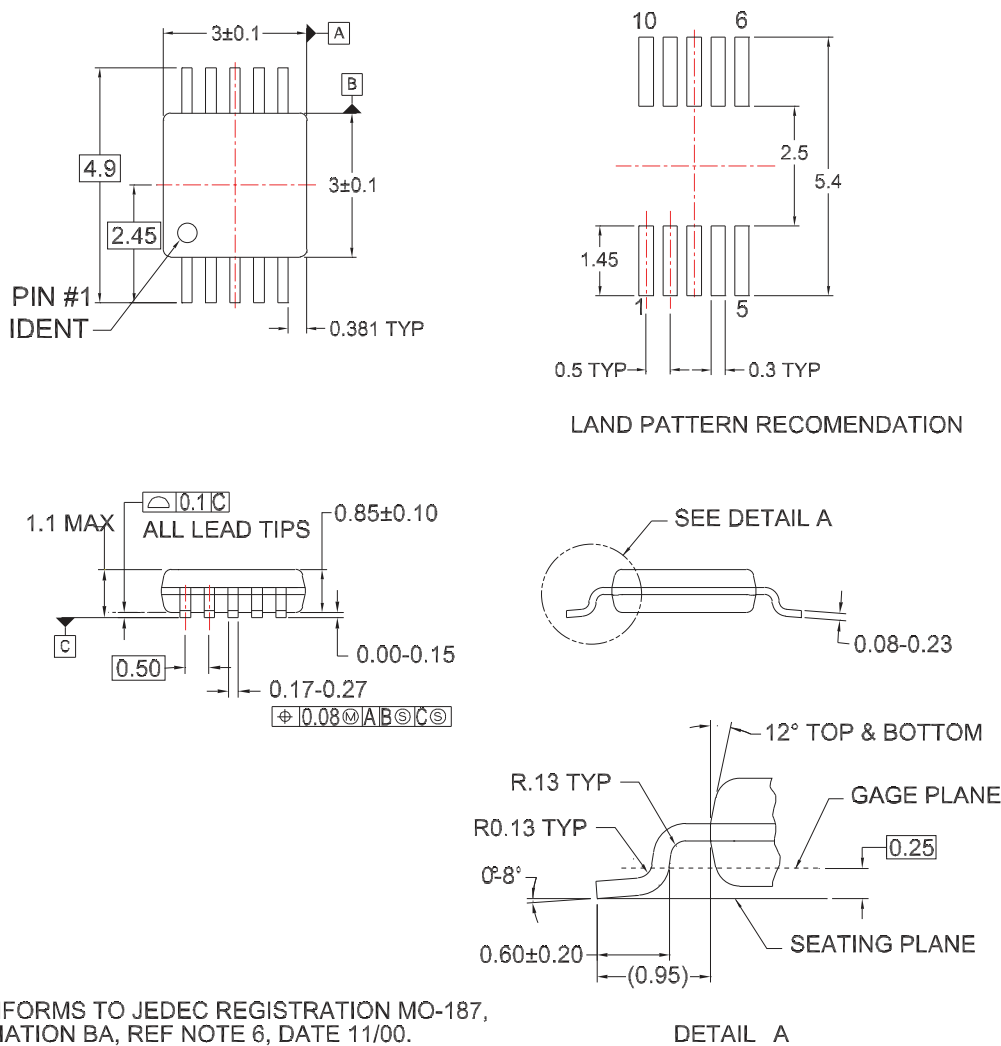
Figure 18. 14-Terminal De-populated Quad Very-Thin Flat Pack No Leads (DQFN), JEDEC MO-241, 2.5 x 3.0mm

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Physical Dimensions



NOTES:

- A. CONFORMS TO JEDEC REGISTRATION MO-187, VARIATION BA, REF NOTE 6, DATE 11/00.
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.
- D. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.

MUA10AREVA

Figure 19. 10-Lead Molded Small Outline Package (MSOP), JEDEC MO-187, 3.0mm Wide

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Physical Dimensions

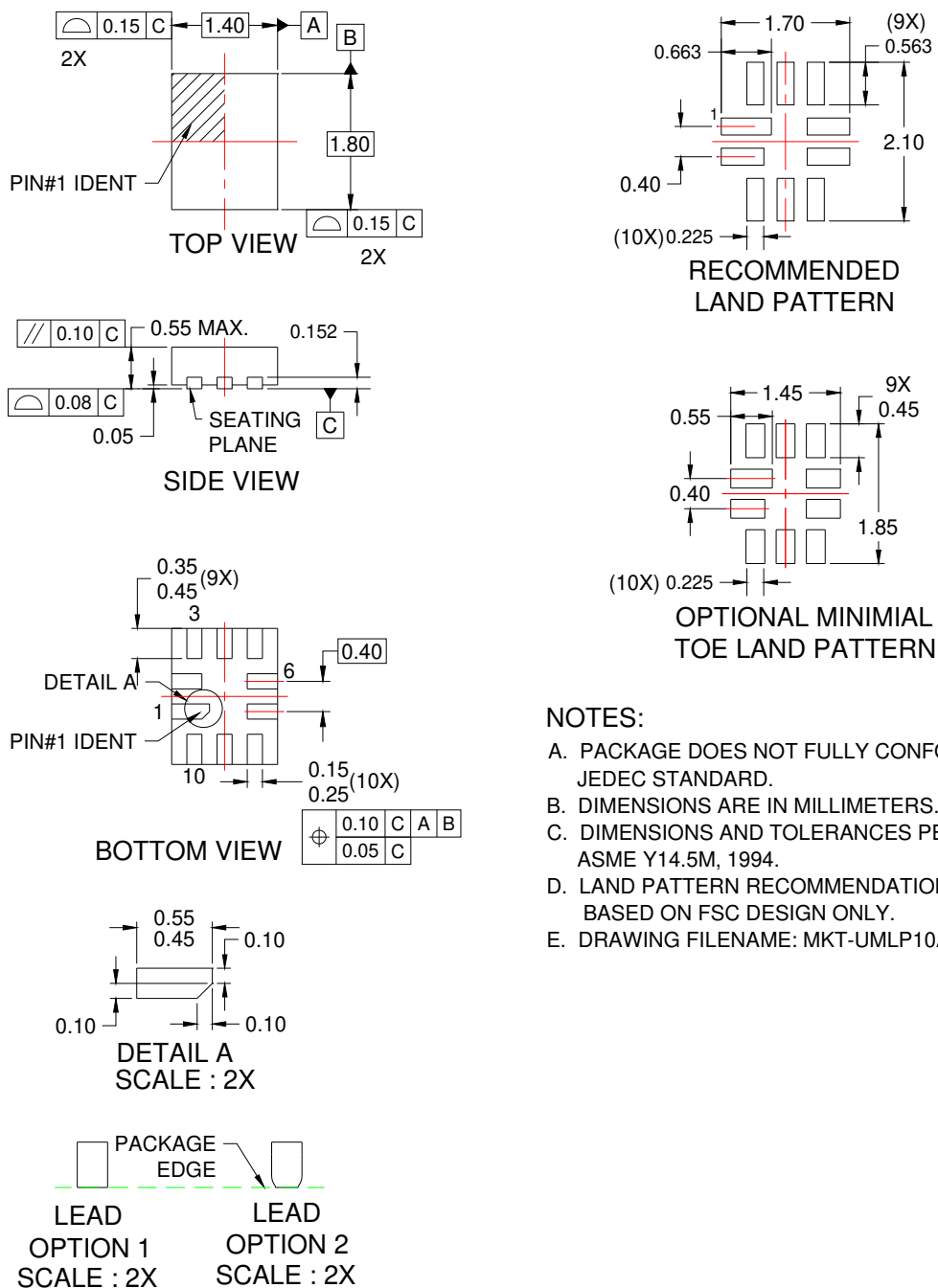


Figure 20. 10-Lead, Quad, Ultrathin Molded Leadless Package (UMLP), 1.4 x 1.8mm



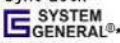
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| AX-CAP™* | Global Power Resource™ | Programmable Active Droop™ | TinyBoost™ |
| BITSiC™ | GreenBridge™ | QFET® | TinyBuck™ |
| Build it Now™ | Green FPS™ | QS™ | TinyCalc™ |
| CorePLUS™ | Green FPS™ e-Series™ | Quiet Series™ | TinyLogic® |
| CorePOWER™ | Gmax™ | RapidConfigure™ | TINYOPTO™ |
| CROSSVOLT™ | GTO™ |  ™ | TinyPower™ |
| CTL™ | IntelliMAX™ | Saving our world, 1mW/WkW at a time™ | TinyPwm™ |
| Current Transfer Logic™ | ISOPLANAR™ | SignalWise™ | TinyWire™ |
| DEUXPEED® | Making Small Speakers Sound Louder and Better™ | SmartMax™ | TransiC™ |
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| EcoSPARK® | MICROCOUPLER™ | Solutions for Your Success™ | TRUECURRENT®* |
| EfficientMax™ | MicroFET™ | SPM® | µSerDes™ |
| ESBC™ | MicroPak™ | STEALTH™ |  SerDes™ |
|  Fairchild® | MicroPak2™ | SuperFET® | UHC™ |
| Fairchild Semiconductor® | MillerDrive™ | SuperSOT™-3 | Ultra FRFET™ |
| FACT Quiet Series™ | MotionMax™ | SuperSOT™-6 | UniFET™ |
| FACT® | Motion-SPM™ | SuperSOT™-8 | VCX™ |
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Definition of Terms

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Preliminary	First Production	Datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
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