9-Channel RGBW LED Driver with Buck Regulator and I²C Interface

Features

- 2.7V to 5.5V Input Voltage Operating Range
- Nine High-Precision Current Sinks
  - LED Current Up to 32mA per Channel
  - ±1% Typical Current Matching
  - ±2% Typical Current Accuracy at 32mA
  - 6-bit Current Dimming Control with I²C
  - Independent On/Off Control
  - Supports both Independent and Global Dimming
- High Efficiency Buck Regulator
  - Integrated 200mΩ / 100mΩ High / Low-Side FET
  - Adaptive On-Time Control with default 1MHz Switching Frequency, with factory programmable 1.5MHz, 2MHz, and 2.5MHz options.
  - Adaptive VOUT Control Based on the Headroom Voltages of the LED Current Sinks.
  - Selectable Auto-Skip Mode or Forced-PWM mode at Light Loads
- 140µA Typical No-Load Supply Current
- Open-Drain $\overline{\text{FAULT}}$ Signal Output and Fault Reset
- Extensive Fault Diagnostics
- -40°C - 85°C Operating Ambient Temperature Range
- Small UQFN-20 (3mm x 3mm) Package

Applications

- RGBW LED Drivers
- Video Door Bells
- Security Cameras
- IRIS Recognition Cameras

Brief Description

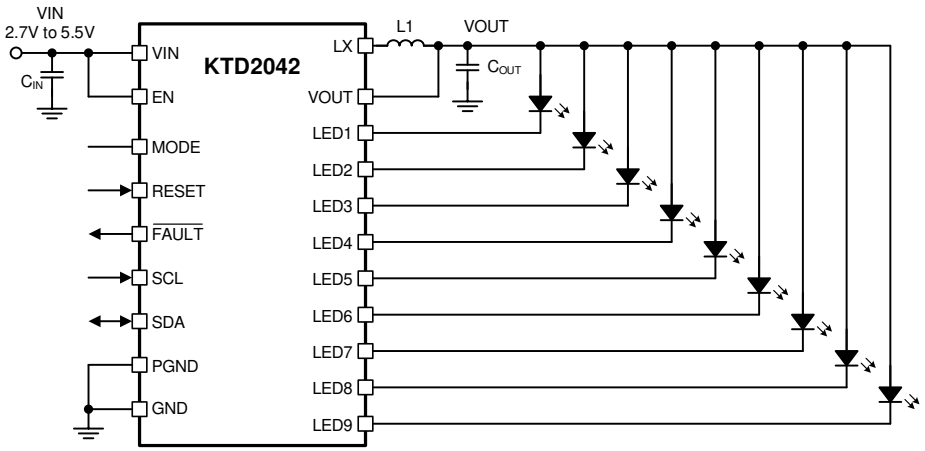
The KTD2042 is an ideal power solution for RGBW LED driver with an integrated buck regulator. It has 9 high-precision current sinks that can be independently controlled via I²C interface.

The buck regulator has an input voltage operating range from 2.7V to 5.5V to accommodate 1-cell lithium-ion batteries or 5V voltage rail. It has adaptive output voltage control based on the headroom voltages of the LED current sinks to minimize the power consumption. It has integrated high-side and low-side power FET. The buck regulator features advanced adaptive On-Time control with 1MHz switching frequency, which minimizes external component counts and allows the use of a very small inductor and capacitor.

The KTD2042 has 9 built-in current sinks, which features independent On/Off control and 6-bit independent current dimming via I²C interface. The KTD2042 has extensive built-in protection features including cycle-by-cycle current limit, input undervoltage Lockout (UVLO), output over-voltage protection, LED fault (open) protection and thermal shutdown protection.

The KTD2042 is available in a RoHS and Green compliant 3mm x 3mm UQFN package.

Typical Application

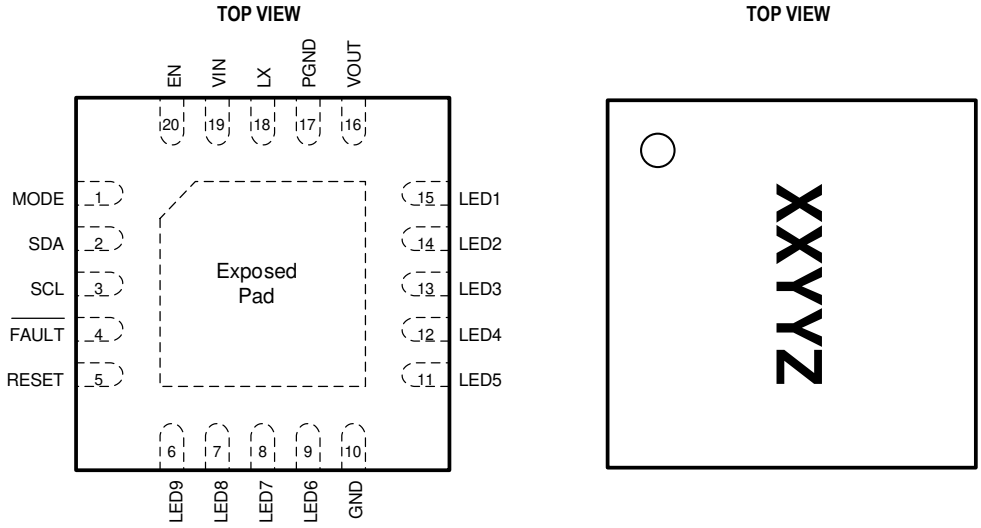


Pin Descriptions

Pin #	Name	Function
1	MODE	Mode selection logic input pin. Low for Forced-PWM mode, High for Auto-Skip mode at light loads.
2	SDA	I^2C Serial Interface Data.
3	SCL	I^2C Serial Interface Clock.
4	$\overline{FAULT}$	Fault signal open-drain output. Logic low output indicates fault conditions, logic high indicates no fault.
5	RESET	Fault Reset pin, connected to GND if not used.
6	LED9	LED9 current sink.
7	LED8	LED8 current sink.
8	LED7	LED7 current sink.
9	LED6	LED6 current sink.
10	GND	Analog Ground.
11	LED5	LED5 current sink.
12	LED4	LED4 current sink.
13	LED3	LED3 current sink.
14	LED2	LED2 current sink.
15	LED1	LED1 current sink.
16	VOUT	Buck regulator output voltage sense input.
17	PGND	Power Ground.
18	LX	Inductor connection for buck regulator.
19	VIN	Voltage Input for buck regulator and IC power.
20	EN	Chip enable logic input.
--	EP	Exposed Paddle -- connect to PCB ground plane using multiple vias directly under the IC.

Pinout Diagram

UQFN33-20



20-Pin 3mm x 3mm x 055mm
UQFN Package, 0.4mm pitch
Top Mark
XX = Device ID Code, YWZ = Date and Assembly Code

Absolute Maximum Ratings[1]

(T_A = 25°C unless otherwise noted)

Symbol	Description	Value	Units
	VIN, EN, SCL, SDA, $\overline{FAULT}$, RESET, MODE, VOUT, LED1 to LED9	-0.3 to 6	V
	LX	-0.3 to VIN+0.3	V
T_J	Operating Junction Temperature Range	-40 to 150	°C
T_s	Storage Temperature Range	-55 to 150	°C
T_{LEAD}	Maximum Soldering Temperature (at leads, 10 sec)	260	°C

ESD Ratings[2]

Symbol	Description	Value	Units
V_{ESD_HBM}	ANSI/ESDA/JEDEC JS-001 Human Body Model (HBM, all pins)	±2000	V
V_{ESD_CDM}	JESD22-C101 Charge Device Model (CDM, all pins)	±1000	V

Thermal Capabilities[3]

Symbol	Description	Value	Units
Θ_{JA}	Thermal Resistance – Junction to Ambient	48	°C/W
P_D	Maximum Continuous Power Dissipation at 25°C (T_J = 125°C)	2.08	W
$\Delta P_D/\Delta T$	Derating Factor Above T_A = 25°C	-20.8	mW/°C

Ordering Information

Part Number	Marking[4]	Operating Temperature	Package
KTD2042EUAC-TR	IKYWZ	-40°C to +85°C	UQFN33-20

1. Stresses above those listed in Absolute Maximum Ratings may cause permanent damage to the device. Functional operation at conditions other than the operating conditions specified is not implied. Only one Absolute Maximum rating should be applied at any one time.
2. ESD Ratings conform to JEDEC industry standards. Some pins may actually have higher performance. Ratings apply with chip enabled, disabled, or unpowered, unless otherwise noted.
3. Junction to Ambient thermal resistance is highly dependent on PCB layout. Values are based on thermal properties of the device when soldered to an EV board.
4. XX = Device ID Code, YWZ = Date and Assembly Code.

Electrical Characteristics[5]

Unless otherwise noted, the *Min* and *Max* specs are applied over the full operation temperature range of -40°C to +85°C and V_{CC} = V_{IN} = 2.5V to 5.5V. Typical values are specified at T_A = +25°C with V_{IN} = 3.6V.

Symbol	Description	Conditions	Min	Typ	Max	Units
IC Supply						
VIN	Input Operating Range		2.7		5.5	V
V_{UVLO}	Under-Voltage Lockout Threshold	V_{IN} Rising	2.5	2.6	2.7	V
		V_{IN} Hysteresis		200		mV
V_{POR}	Power-On-Reset Threshold	V_{IN} Rising		1.8		V
		V_{IN} Rising		100		mV
I_q	No-Load Supply Current (EN = High)	Not Switching, all LEDs off		140		µA
		FPWM Mode, all LEDs off		1.6		mA
I_{SHDN}	Shutdown Current	EN = Low		0.6	1	µA
Logic Pin Specifications (EN, MODE, $\overline{FAULT}$)						
V_{IH}	Input Logic High (EN, MODE)		1.1			V
V_{IL}	Input Logic Low (EN, MODE)				0.4	V
I_{I_LK}	Input Logic Leakage (EN, MODE)	T_A = 25°C, V_I = 0V or V_{IN}	-1	±0.01	1	µA
R_{I_PD}	Input Logic Pull-Down (EN, MODE)	Only connected when $V_I \le V_{IL}$ (disconnected when $V_I \ge V_{IH}$)		250		kΩ
V_{OL}	Output Logic Low ($\overline{FAULT}$)				0.4	V
Buck Regulator						
R_{DSON_H}	High-Side FET On-Resistance			200		mΩ
R_{DSON_L}	Low-Side FET On-Resistance			100		mΩ
I_{LIM}	Peak Current Limit Threshold			750		mA
I_{ZCD}	Zero Crossing Threshold	Skip Mode		50		mA
F_{SW}	Switching Frequency			1		MHz
Current Sink						
I_{LED_SET}	Current Setting Range	64 steps of 0.5mA/step	0		32	mA
I_{LED_ACC}	Current Sink Accuracy	I_{LED_ON} = 32mA setting		±2		%
I_{LED_MATCH}	Current Sink Matching	I_{LED_ON} = 32mA setting		±1		%
V_{SINK}	Headroom Voltage of Current Sink	I_{LED_ON} = 25mA setting		0.10		V
I_{LED_LK}	Current Sink Leakage	0mA setting or shutdown		0.01	1	µA
Thermal Shutdown						
T_{SD}	Junction Thermal Shutdown Threshold	T_J rising		150		°C
	Junction Thermal Shutdown Hysteresis	Hysteresis		20		°C

5. Device is guaranteed to meet performance specifications over the -40°C to +85°C operating temperature range by design, characterization and correlation with statistical process controls.

Electrical Characteristics (continued)[5]

Unless otherwise noted, the *Min* and *Max* specs are applied over the full operation temperature range of -40°C to +85°C and V_{CC} = V_{IN} = 2.5V to 5.5V. Typical values are specified at T_A = +25°C with V_{IN} = 3.6V.

Symbol	Description	Conditions	Min	Typ	Max	Units
I²C-Compatible Interface Specifications (SCL, SDA), see Figure 1						
V_{IH}	Input Logic High Threshold		1.1			V
V_{IL}	Input Logic Low Threshold				0.4	V
V_{OL}	SDA Output Logic Low	I_{SDA} = 3mA			0.4	V
t_1	SCL clock period		2.5			µs
t_2	Data in setup time to SCL high		100			ns
t_3	Data out stable after SCL low		0			ns
t_4	SDA low setup time to SCL low (Start)		100			ns
t_5	SDA high hold time after SCL high (Stop)		100			ns

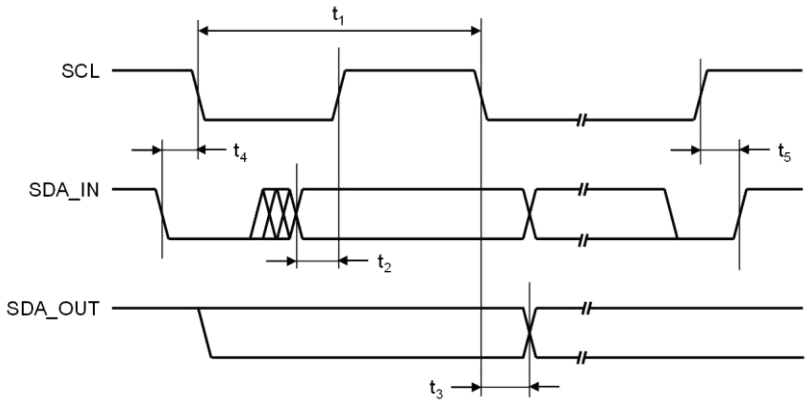
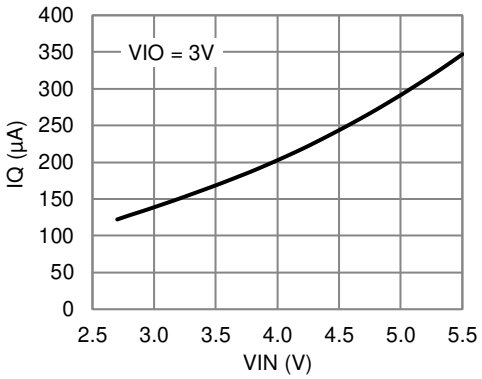


Figure 1. I²C Compatible Interface Timing Diagram

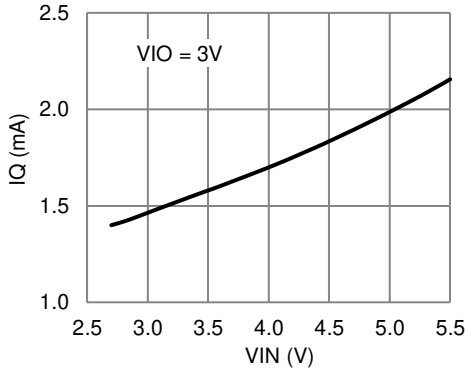
Typical Characteristics

Unless otherwise noted, V_{IN} = 3.6V, Global LED mode, EN = High, MODE = High (Skip mode), RESET = Low, COUT = 22µF, L = 4.7µH (DFE252012P-4R7M=P2 from Murata) and T_A = 25°C.

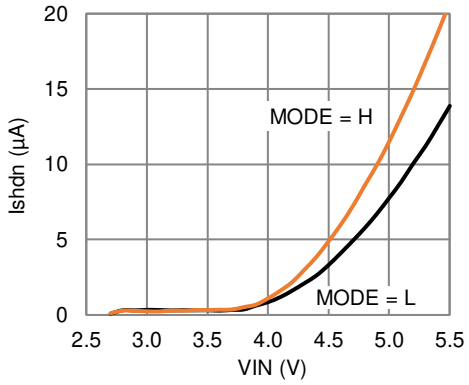
IQ vs. VIN
(Skip Mode, No Load)



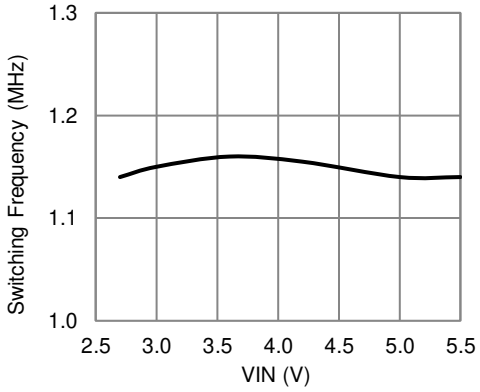
IQ vs. VIN
(Fixed PWM Mode, No Load)



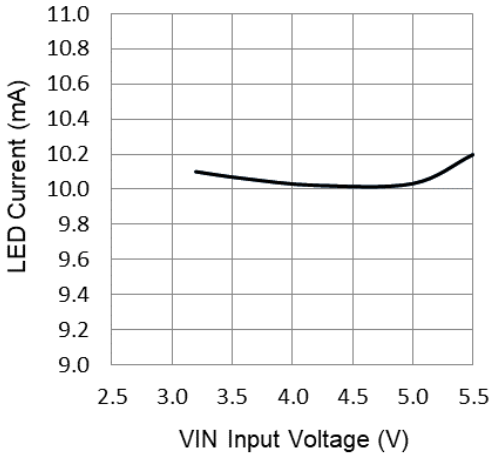
Shutdown Current vs. VIN
(VIO = 3V)



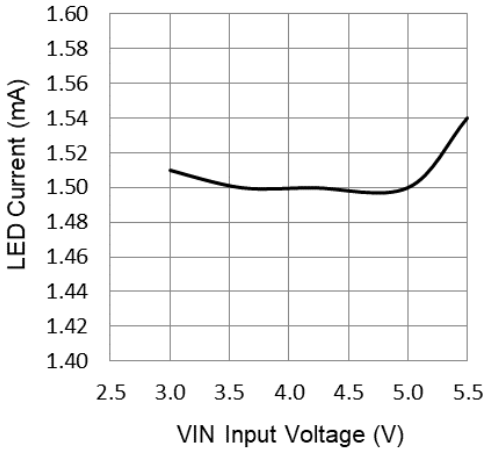
Switching Frequency vs. VIN
(Global ILED = 10mA)



LED Current vs. VIN
(Global ILED = 10mA, VOUT = 3.1V)



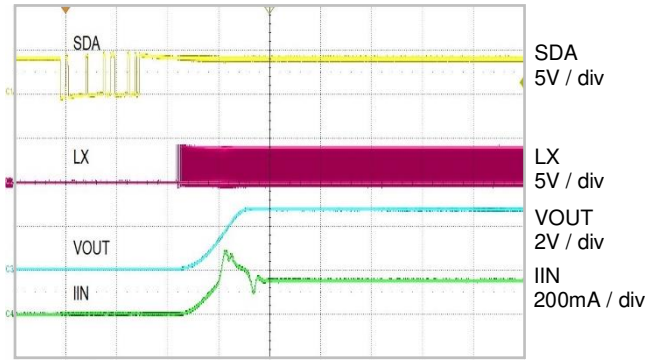
LED Current vs. VIN
(Global ILED = 1.5mA, VOUT = 2.8V)



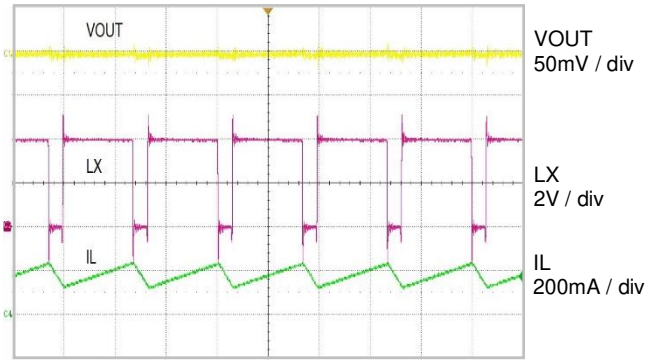
Typical Characteristics

Unless otherwise noted, V_{IN} = 4.0V, Global LED mode, EN = High, MODE = High (Skip mode), RESET = Low, COUT = 22µF, L = 4.7µH (DFE252012P-4R7M=P2 from Murata) and T_A = 25°C.

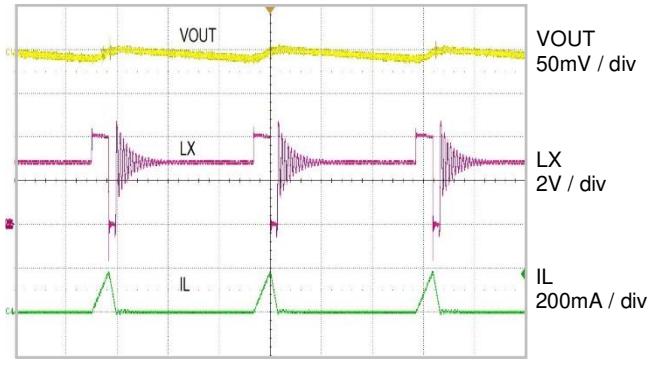
Turn on by I2C Global LED
(9 channels at 20mA, Skip mode)



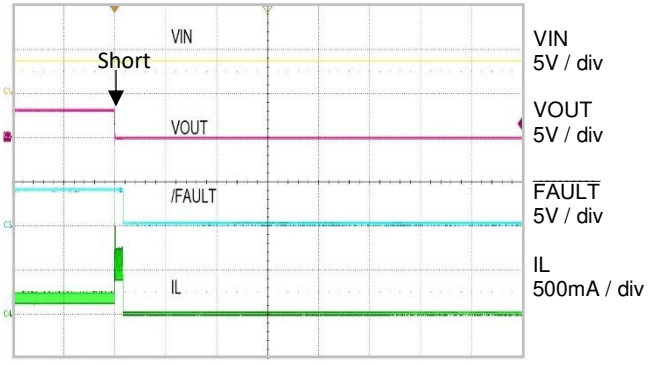
Switching Waveform Global LED
(9 channels at 20mA, fixed PWM mode)



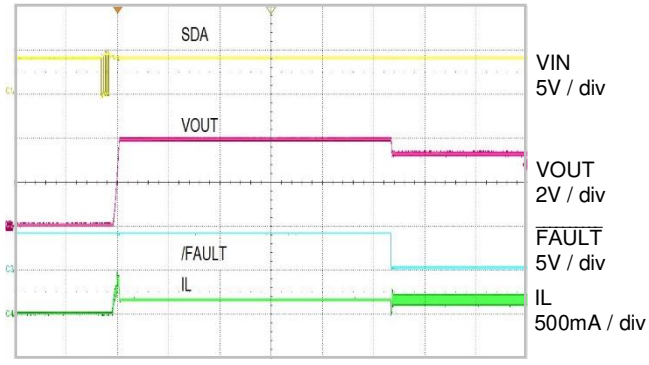
Switching waveform Global LED
(9 LEDs at 1.5mA/channel, Skip mode)



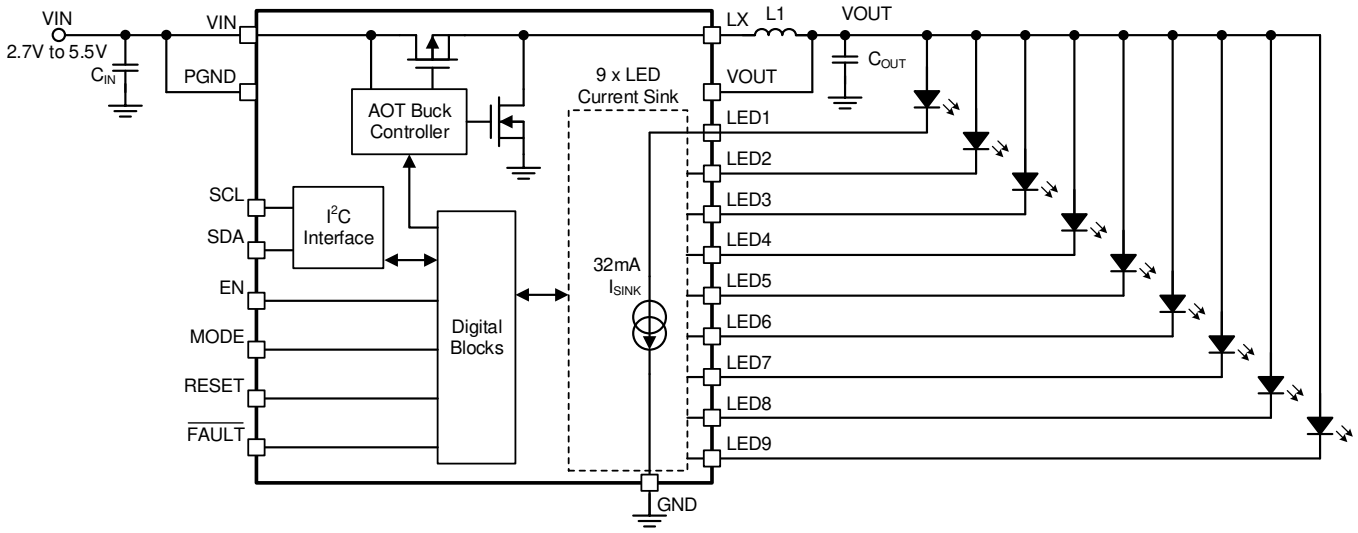
VOUT short to GND Response



Turn on with an Open LED
(9 LEDs at 20mA, Global LED)



Functional Block Diagram



Functional Block Diagram

Functional Description

Overview

KTD2042 is a 9-channel LED driver with integrated buck converter with independent control of each channel. It can be powered from a Li-ion battery or a supply voltage up to 5.5V to provide a lower output voltage for driving the LEDs with a minimum sink voltage around 100mV.

High switching frequency of the step-down converter allows the use of smaller inductors and capacitors.

The LED driver nine regulated current sinks can support current up to 32mA per channel with 6-bit linear dimming resolution programmable via I^2C bus.

Various protection features are built into KTD2042, including inductor current limit protection, output short circuit protection, output over-voltage protection, LED fault (open) protection and thermal shutdown protection. The device is equipped with I^2C interface for various controls and status monitor.

Hardware Enable

KTD2042 has a logic input EN pin to enable/disable the device. When EN pin is set low, the device goes into shutdown mode, but the I^2C registers are not reset to their default values and the I^2C bus remains enabled. Under this condition, it is possible to write and read to the registers.
When EN pin goes from low to high, the device becomes enabled and configured according to the current register values.

Buck Configuration

When EN pin is high, the buck can be enabled or disabled by programming the register 0x11 bit [3] to 1 and bit [2] to 1 for Enable or 0 to Disable.
The buck switching mode can be set to Forced-PWM or Auto-skip mode by the MODE pin or by software.
To select buck mode by MODE pin, set MODE pin Low for Forced-PWM or set MODE pin High for Auto-Skip mode at light load.
To select buck mode by software, write register 0x11 bit [1] to 1 and bit [0] to 0 for Forced-PWM, or bit [0] to 1 for Auto-Skip mode.

LED Current Setting

The nine LED current sinks can be controlled globally or individually.

Global LED mode

To control the LEDs globally, select Global LED mode by setting LED_CONFIG register 0x02 bit [7] to 1.
To identify how many LEDs are included in the Global LED mode, write to register 0x02 bits [2:5] as follows.

- 0000 = All 9 channels are used
- 0001 = 1 channel (LED9) is not used
- 0010 = 2 channels (LED9, LED8) are not used
- …
- 1111 = 8 channels (LED9, LED8, LED7, LED6, LED5, LED4, LED3, LED2) are not used

To select Global LED Current setting between 0.5mA and 32mA, write the brightness code in register 0x04 bits [5:0].
To program the LED current (I_{LED}), the Global Current register code is set according to the following formula:

I_{LED} = (1 + code) x 0.5mA
code = 39 decimal = 0x27 corresponds to ILED = 20mA

To enable Global LEDs, write register 0x02 bit [1] to 1. To disable the Global LEDs, write register 0x02 bit [1] to 0.

Individual LED mode

To control the LEDs individually, select individual LED mode by setting register 0x02 bit [7] to 0.
To set individual LED Current settings between 0.5mA and 32mA, write the brightness codes in registers 0x05 to 0x0D bits [5:0] for respectively LED1 to LED9 settings.
To program each individual LED current (I_{LEDX}), the Individual Current registers are set according to the following formula:

I_{LEDX} = (1 + code) x 0.5mA
For example, code = 33 decimal = 0x21 corresponds to ILEDX = 17mA

To enable the individual LED1, write register 0x02 bit [0] to 1. To enable the individual LED2 to LED9, write register 0x03 bits [7:0] to 1.
To disable individual LEDs, write the corresponding bits of registers 0x02 or 0x03 to 0.

Open LED

Each current sink is protected against LED open conditions.
In case of an LED open condition, the current sink voltage of the open channel remains close to 0V and the converter drives the output voltage as high as possible operating in linear mode (not switching) with VOUT following VIN. With the sink pin voltage failing to regulate, a fault is triggered with the /FAULT output going low. The Open LED channel is turned off, the buck converter regulates VOUT voltage lower and drive the other channels normally.
The Open LED channel is ignored until the open LED condition is removed and the fault is cleared by either writing register 0x10 Bit [0] to 1, or by toggling the RESET pin high.

Fault Status

Open LED fault status is stored in two Fault Status registers 0x0E and 0x0F.
When an Open LED fault is triggered, Fault Status 0x0E bit [7] is set to 1 and the associated register 0x0E or 0x0F LED channel bits are set to 1 to report the Open channels.

LED faults can be cleared by either writing to a register bit or toggling the RESET pin as follows.

- Writing a 1 into register 0x10 bit [0]. This is a Write only bit.
- Toggling the RESET pin high.

VIN supply voltage and device operation fault status are stored in registers 0x0F and 0x13. For more details, please refer to the register description.

Fault Output Pin

When an Open LED fault is triggered, the open-drain output /FAULT pin is pulled low.
Once all Open LED fault conditions are removed and LED faults are cleared, the /FAULT output is released and return high.

Application Information

I²C Serial Data Bus

KTD2042 supports the I²C bus protocol. A device that sends data onto the bus is defined as a transmitter and a device receiving data as a receiver. The device that controls the bus is called a master, whereas the devices controlled by the master are known as slaves. A master device must generate the serial clock (SCL), control bus access and generate START and STOP conditions to control the bus. KTD2042 operates as a slave on the I²C bus. Within the bus specifications a standard mode (100kHz maximum clock rate) and a fast mode (400kHz maximum clock rate) are defined. KTD2042 works in both modes. Connections to the bus are made through the open-drain I/O lines SDA and SCL.

The following bus protocol has been defined in Figure 2:

- Data transfer may be initiated only when the bus is not busy.
- During data transfer, the data line must remain stable whenever the clock line is HIGH. Changes in the data line while the clock line is high are interpreted as control signals.

Accordingly, the following bus conditions have been defined:

Bus Not Busy

Both data and clock lines remain HIGH.

Start Data Transfer

A change in the state of the data line, from HIGH to LOW, while the clock is HIGH, defines a START condition.

Stop Data Transfer

A change in the state of the data line, from LOW to HIGH, while the clock line is HIGH, defines the STOP condition.

Data Valid

The state of the data line represents valid data when, after a START condition, the data line is stable for the duration of the HIGH period of the clock signal. The data on the line must be changed during the LOW period of the clock signal. There is one clock pulse per bit of data.

Each data transfer is initiated with a START condition and terminated with a STOP condition. The number of data bytes transferred between START and STOP conditions are not limited and are determined by the master device. The information is transferred byte-wise and each receiver acknowledges with a ninth bit.

Acknowledge

Each receiving device, when addressed, is obliged to generate an acknowledge after the reception of each byte. The master device must generate an extra clock pulse that is associated with this acknowledge bit.

A device that acknowledges must pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is stable LOW during the HIGH period of the acknowledge-related clock pulse. Setup and hold times must also be taken into account.

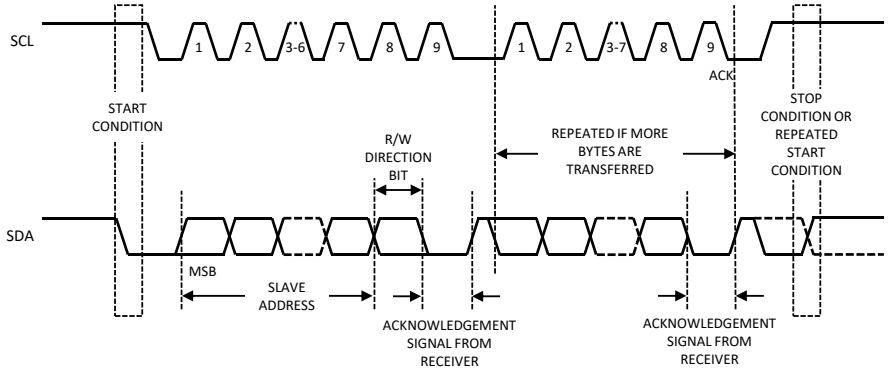


Figure 2. Data Transfer on I²C Serial Bus

KTD2042 7-bit slave device address is 0100000 binary (0x20h).

There are two kinds of I²C data transfer cycles: write cycle and read cycle.

I²C Write Cycle

For I²C write cycle, data is transferred from a master to a slave. The first byte transmitted is the 7-bit slave address plus one bit of '0' for write. Next follows a number of data bytes. The slave returns an acknowledge bit after each received byte. Data is transferred with the most significant bit (MSB) first. Figure 3 shows the sequence of the I²C write cycle.

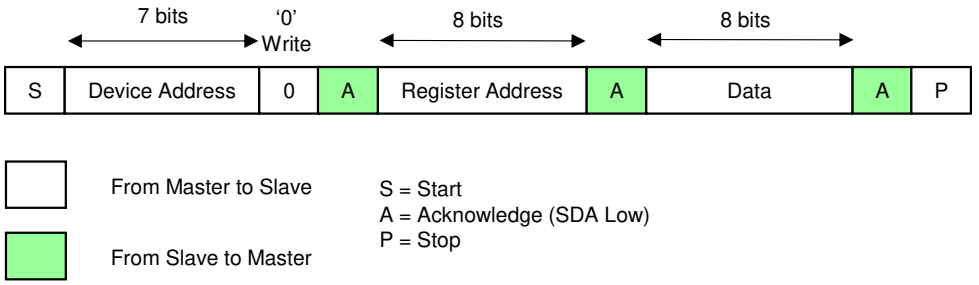


Figure 3. I²C Write Cycle

I²C Write Cycle Steps:

- Master generates start condition.
- Master sends 7-bit slave address (0100000 for KTD2042) and 1-bit data direction '0' for write.
- Slave sends acknowledge if the slave address is matched.
- Master sends 8-bit register address.
- Slave sends acknowledge.
- Master sends 8-bit data for that addressed register.
- Slave sends acknowledge.
- If master sends more data bytes, the register address will be incremented by one after each acknowledge.
- Master generates stop condition to finish the write cycle.

I²C Read Cycle

For I²C read cycle, data is transferred from a slave to a master. But to start the read cycle, master needs to write the register address first to define which register data to read. Figure 4 shows the steps of the I²C read cycle.

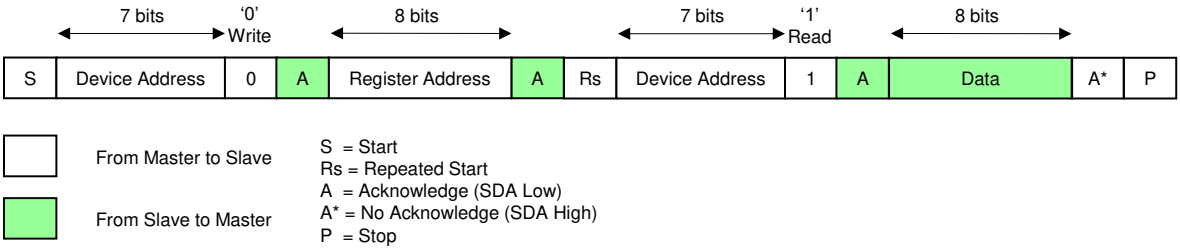


Figure 4. I²C Read Cycle

I²C Read Cycle Steps:

- Master generates start condition.
- Master sends 7-bit slave address (0100000 for KTD2042) and 1-bit data direction '0' for write.
- Slave sends acknowledge if the slave address is matched.
- Master sends 8-bit register address.
- Slave sends acknowledge.
- Master generates repeated start condition.
- Master sends 7-bit slave address (0100000 for KTD2042) and 1-bit data direction '1' for read.
- Slave sends acknowledge if the slave address is matched.
- Slave sends the data byte of that addressed register.

- If master sends acknowledge, the register address will be incremented by one after each acknowledge and the slave will continue to send the data for the updated addressed register.
- If master sends no acknowledge, the slave will stop sending the data.
- Master generates stop condition to finish the read cycle.

I²C Register Map

Table 1 summarizes KTD2042 I²C registers, their read/write settings and default values. The registers can only be reset to their default values by VIN power on reset. Toggling EN pin does not reset the registers to their default values.

Table 1. I²C Register Map

Hex Address	Register Name	Access	Default Value
0x00	CHIP_ID	R	0xA9
0x01	MONITOR	R	0x00
0x02	LED_CONFIG	R/W	0x00
0x03	LED_EN_IDVD	R/W	0x00
0x04	LED_GBAL_SET	R/W	0x00
0x05	LED1_SET	R/W	0x00
0x06	LED2_SET	R/W	0x00
0x07	LED3_SET	R/W	0x00
0x08	LED4_SET	R/W	0x00
0x09	LED5_SET	R/W	0x00
0x0A	LED6_SET	R/W	0x00
0x0B	LED7_SET	R/W	0x00
0x0C	LED8_SET	R/W	0x00
0x0D	LED9_SET	R/W	0x00
0x0E	FAULT_STAT1	R	0x00
0x0F	FAULT_STAT2	R	0x00
0x10	FAULT_CLEAR	W/C	0x00
0x11	BUCK_CONFIG	R/W	0x00
0x13	STATUS	R	0x00

Table 2. CHIP_ID Register

ADDRESS	MODE		RESET VALUE: 0xA9
0x00	R		
BIT	NAME	POR	DESCRIPTION
7:5	VENDOR	101	Vendor Identification 101 = Kinetic Technologies
4:0	DIE_ID	01001	Die identification

Note: POR for Power-on reset or reset value

Table 3. MONITOR Register

ADDRESS	MODE		RESET VALUE: 0x00
0x01	R		
BIT	NAME	POR	DESCRIPTION
7:4	RSVD	000	Reserved
3:0	DIE_REV	xxxx	Die revision identification

Table 4. LED_CONFIG Register

ADDRESS	MODE		RESET VALUE: 0x00
0x02	R/W		
BIT	NAME	POR	DESCRIPTION
7	Ctrl_Mode_LED	0	0 : individual, 1 : global LED control
6	RSVD	0	Reserved
5	Global_LED_Channel [3:0]	0	0000 = All 9 channels are used
4		0	0001 = 1 channel (LED9) is not used
3		0	0010 = 2 channels (LED9, LED8) are not used
2		0	1111 = 8 channels (LED9, LED8, LED7, LED6, LED5, LED4, LED3, LED2) are not used
1	Global_EN_LED	0	LEDx enable in global control mode, 0 = Disable, 1 = Enable
0	EN_LED1	0	LED1 enable in individual control mode, 0 = Disable, 1 = Enable

Table 5. LED_EN_IDVD Register

ADDRESS	MODE		RESET VALUE: 0x00
0x03	R/W		
BIT	NAME	POR	DESCRIPTION
7	EN_LED2	0	LED2 enable in individual control mode, 0 = Disable, 1 = Enable
6	EN_LED3	0	LED3 enable in individual control mode, 0 = Disable, 1 = Enable
5	EN_LED4	0	LED4 enable in individual control mode, 0 = Disable, 1 = Enable
4	EN_LED5	0	LED5 enable in individual control mode, 0 = Disable, 1 = Enable
3	EN_LED6	0	LED6 enable in individual control mode, 0 = Disable, 1 = Enable
2	EN_LED7	0	LED7 enable in individual control mode, 0 = Disable, 1 = Enable
1	EN_LED8	0	LED8 enable in individual control mode, 0 = Disable, 1 = Enable
0	EN_LED9	0	LED9 enable in individual control mode, 0 = Disable, 1 = Enable

Table 6. LED_GBAL_SET Register

ADDRESS	MODE		RESET VALUE: 0x00
0x04	R/W		
BIT	NAME	POR	DESCRIPTION
7:6	RSVD	0	Reserved
5:0	LED_Global_Current [5:0]	0	Set LED current in Global Control Mode ILED = (DEC ([5:0]) * 0.5mA) + 0.5mA 000000 = 0.5mA 000001 = 1mA … 111110 = 31.5mA 111111 = 32mA

Table 7. LED1_SET Register

ADDRESS	MODE		RESET VALUE: 0x00
0x05	R/W		
BIT	NAME	POR	DESCRIPTION
7:6	RSVD	0	Reserved
5:0	LED1_Current [5:0]	0	Set LED current in Individual control mode ILED = (DEC ([5:0]) * 0.5mA) + 0.5mA 000000 = 0.5mA 000001 = 1mA … 111110 = 31.5mA 111111 = 32mA

Table 8. LED2_SET Register

ADDRESS	MODE		RESET VALUE: 0x00
0x06	R/W		
BIT	NAME	POR	DESCRIPTION
7:6	RSVD	0	Reserved
5:0	LED2_Current [5:0]	0	Set LED current in Individual control mode ILED = (DEC ([5:0]) * 0.5mA) + 0.5mA 000000 = 0.5mA 000001 = 1mA … 111110 = 31.5mA 111111 = 32mA

Table 9. LED3_SET Register

ADDRESS	MODE		RESET VALUE: 0x00
0x06	R/W		
BIT	NAME	POR	DESCRIPTION
7:6	RSVD	0	Reserved
5:0	LED3 Current [5:0]	0	Set LED current in Individual control mode ILED = (DEC ([5:0]) * 0.5mA) + 0.5mA 000000 = 0.5mA 000001 = 1mA … 111110 = 31.5mA 111111 = 32mA

Table 10. LED4_SET Register

ADDRESS	MODE		RESET VALUE: 0x00
0x06	R/W		
BIT	NAME	POR	DESCRIPTION
7:6	RSVD	0	Reserved
5:0	LED4_Current [5:0]	0	Set LED current in Individual control mode ILED = (DEC ([5:0]) * 0.5mA) + 0.5mA 000000 = 0.5mA 000001 = 1mA … 111110 = 31.5mA 111111 = 32mA

Table 11. LED5_SET Register

ADDRESS	MODE		RESET VALUE: 0x00
0x06	R/W		
BIT	NAME	POR	DESCRIPTION
7:6	RSVD	0	Reserved
5:0	LED5_Current [5:0]	0	Set LED current in Individual control mode ILED = (DEC ([5:0]) * 0.5mA) + 0.5mA 000000 = 0.5mA 000001 = 1mA … 111110 = 31.5mA 111111 = 32mA

Table 12. LED6_SET Register

ADDRESS	MODE		RESET VALUE: 0x00
0x07	R/W		
BIT	NAME	POR	DESCRIPTION
7:6	RSVD	0	Reserved
5:0	LED6_Current [5:0]	0	Set LED current in Individual control mode ILED = (DEC ([5:0]) * 0.5mA) + 0.5mA 000000 = 0.5mA 000001 = 1mA … 111110 = 31.5mA 111111 = 32mA

Table 13. LED7_SET Register

ADDRESS	MODE		RESET VALUE: 0x00
0x08	R/W		
BIT	NAME	POR	DESCRIPTION
7:6	RSVD	0	Reserved
5:0	LED7_Current [5:0]	0	Set LED current in Individual control mode ILED = (DEC ([5:0]) * 0.5mA) + 0.5mA 000000 = 0.5mA 000001 = 1mA … 111110 = 31.5mA 111111 = 32mA

Table 14. LED8_SET Register

ADDRESS	MODE		RESET VALUE: 0x00
0x09	R/W		
BIT	NAME	POR	DESCRIPTION
7:6	RSVD	0	Reserved
5:0	LED8_Current [5:0]	0	Set LED current in Individual control mode ILED = (DEC ([5:0]) * 0.5mA) + 0.5mA 000000 = 0.5mA 000001 = 1mA … 111110 = 31.5mA 111111 = 32mA

Table 15. LED9_SET Register

ADDRESS	MODE		RESET VALUE: 0x00
0x10	R/W		
BIT	NAME	POR	DESCRIPTION
7:6	RSVD	0	Reserved
5:0	LED9_Current [5:0]	0	Set LED current in Individual control mode ILED = (DEC ([5:0]) * 0.5mA) + 0.5mA 000000 = 0.5mA 000001 = 1mA … 111110 = 31.5mA 111111 = 32mA

Table 16. FAULT_STAT1 Register

ADDRESS	MODE		RESET VALUE: 0x00
0x0E	R		
BIT	NAME	POR	DESCRIPTION
7	OPEN_LED	0	Open LED Fault, 0 = No fault, 1 = Fault detected
6	RSVD	0	Reserved
5	LED1_Fault	0	Report LED1 Channel has open LED, 0 = No fault, 1 = Fault detected
4	LED2_Fault	0	Report LED2 Channel has open LED, 0 = No fault, 1 = Fault detected
3	LED3_Fault	0	Report LED3 Channel has open LED, 0 = No fault, 1 = Fault detected
2	LED4_Fault	0	Report LED4 Channel has open LED, 0 = No fault, 1 = Fault detected
1	LED5_Fault	0	Report LED5 Channel has open LED, 0 = No fault, 1 = Fault detected
0	LED6_Fault	0	Report LED6 Channel has open LED, 0 = No fault, 1 = Fault detected

Table 17. FAULT_STAT2 Register

ADDRESS	MODE		RESET VALUE: 0x00
0x0F	R		
BIT	NAME	POR	DESCRIPTION
7	LED7_Fault	0	Report LED7 Channel has open LED, 0 = No fault, 1 = Fault detected
6	LED8_Fault	0	Report LED8 Channel has open LED, 0 = No fault, 1 = Fault detected
5	LED9_Fault	0	Report LED9 Channel has open LED, 0 = No fault, 1 = Fault detected
4	RSVD	0	Reserved for future use
3	VIN_OVLO_Fault	0	Buck input OVLO Fault
2	BUCK_OCP_Fault	0	Buck output OCP Fault
1	TJ_OVERTEMP_Fault	0	over temperature Fault, die temperature is greater than 150°C
0	RSVD	0	Reserved for future use

Table 18. FAULT_CLEAR Register

ADDRESS	MODE		RESET VALUE: 0x00
0x10	W/C		
BIT	NAME	POR	DESCRIPTION
7:1	RSVD	0	Reserved for future use
0	Clear_Faults		Write high (1) to clear faults, WRITE only

Table 19. BUCK_CONFIG Register

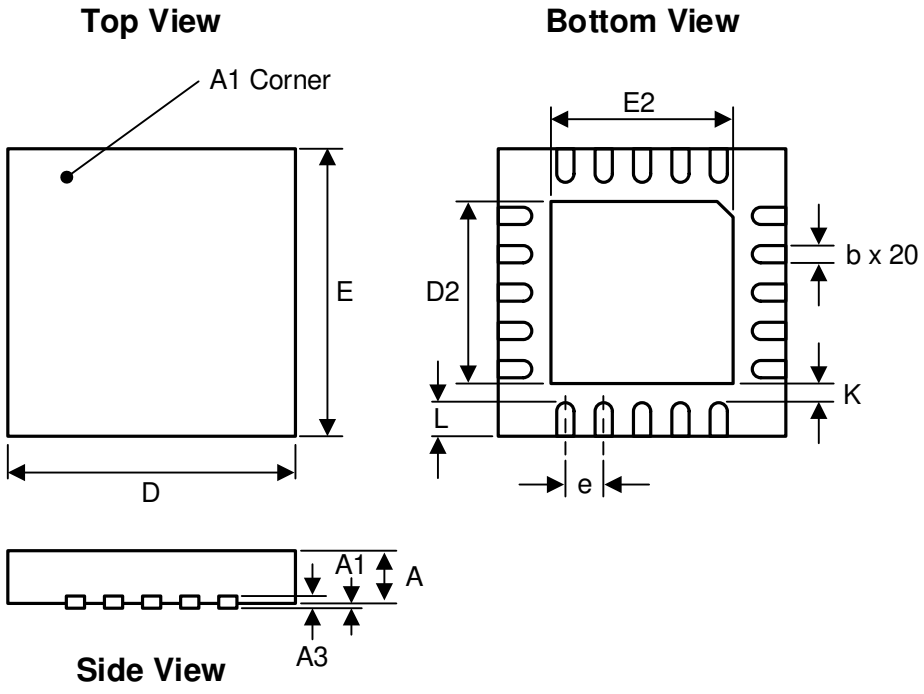
ADDRESS	MODE		RESET VALUE: 0x00
0x11	W/R		
BIT	NAME	POR	DESCRIPTION
7:4	RSVD	0	Reserved for future use
3	Sel_en_sw	0	Select the enable buck, 0: by Pin, 1: by Register
2	Buck_en_sw	0	Enable Buck by soft ware when Sel_en_sw = 1 and EN pin is High
1	Sel_mode	0	Select the mode control, 0: by Pin, 1: by Register
0	Mode_sw	0	Mode control bit with Sel_mode = 1, 0: Forced-PWM, 1: Auto-Skip

Table 20. STATUS Register

ADDRESS	MODE		RESET VALUE: 0x00
0x13	R		
BIT	NAME	POR	DESCRIPTION
7:5	RSVD	0	Reserved for future use
4	VIN_UVLO_STAT	0	VIN under voltage status; 1 when VIN < UVLO
3	VIN_OVLO_STAT	0	VIN over voltage status; 1 when VIN > OVLO
2	BUCK_OCP_STAT	0	Buck output over current protection status; 1 when IOUT > OC
1	TJ_OVERTEMP_STAT	0	Junction over temperature status; 1 when T_J > 150°C
0	RSVD	0	Reserved for future use

Packaging Information

UQFN33-20 (3.00mm x 3.00mm x 0.55mm)



Dimension	mm		
	Min.	Typ.	Max.
A	0.45	0.55	0.60
A1	0.00	–	0.05
A3	0.127 REF		
b	0.13	0.18	0.23
D	2.90	3.00	3.10
D2	1.80	1.90	2.00
E	2.90	3.00	3.10
E2	1.80	1.90	2.00
e	0.40 BSC		
L	0.30	0.35	0.40
K	0.20 REF		

Recommended Footprint