

## FEATURES

- 12-bit plus sign SAR ADC
- True bipolar input ranges
- Software-selectable input ranges  
 $\pm 10\text{ V}$ ,  $\pm 5\text{ V}$ ,  $\pm 2.5\text{ V}$ ,  $0\text{ V}$  to  $+10\text{ V}$
- 500 kSPS throughput rate
- 8 analog input channels with channel sequencer
- Single-ended, true differential, and pseudo differential analog input capability
- High analog input impedance
- Low power: 18 mW
- Temperature indicator
- Full power signal bandwidth: 22 MHz
- Internal 2.5 V reference
- High speed serial interface
- Power-down modes
- 20-lead TSSOP package
- iCMOS process technology

## ENHANCED PRODUCT FEATURES

- Supports defense and aerospace applications (AQEC standard)
- Military temperature range:  $-55^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$
- Controlled manufacturing baseline
- One assembly/test site
- One fabrication site
- Product change notification
- Qualification data available on request

## GENERAL DESCRIPTION

The AD7327-EP<sup>1</sup> is an 8-channel, 12-bit plus sign successive approximation ADC designed on the iCMOS<sup>®</sup> (industrial CMOS) process. It enables the development of a wide range of high performance analog ICs capable of 33 V operation in a footprint that no previous generation of high voltage devices achieved. Unlike analog ICs using conventional CMOS processes, iCMOS components can accept bipolar input signals while providing increased performance, dramatically reduced power consumption, and reduced package size.

The AD7327-EP can accept true bipolar analog input signals, software-selectable from  $\pm 10\text{ V}$ ,  $\pm 5\text{ V}$ ,  $\pm 2.5\text{ V}$ , and  $0\text{ V}$  to  $+10\text{ V}$ . Each analog input channel can be independently programmed to one of the four input ranges. The analog input channels on the AD7327-EP can be programmed to be single-ended, true differential, or pseudo differential.

<sup>1</sup> Protected by U.S. Patent No. 6,731,232.

## FUNCTIONAL BLOCK DIAGRAM

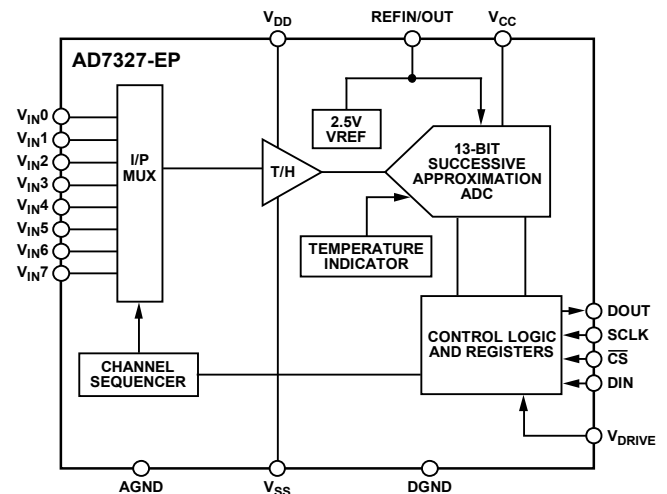


Figure 1.

The ADC contains a 2.5 V internal reference. The AD7327-EP also allows external reference operation. If a 3 V reference is applied to the REFIN/OUT pin, the AD7327-EP can accept a true bipolar  $\pm 12\text{ V}$  analog input. Minimum  $\pm 12\text{ V}$   $V_{DD}$  and  $V_{SS}$  supplies are required for the  $\pm 12\text{ V}$  input range. The ADC has a high speed serial interface that can operate at throughput rates up to 500 kSPS.

The AD7327-EP is housed in a 20-lead TSSOP with operation specified from  $-55^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$ . Additional application and technical information can be found in the [AD7327](#) data sheet.

## PRODUCT HIGHLIGHTS

1. The AD7327-EP can accept true bipolar analog input signals,  $\pm 10\text{ V}$ ,  $\pm 5\text{ V}$ ,  $\pm 2.5\text{ V}$ , and  $0\text{ V}$  to  $+10\text{ V}$  (unipolar).
2. The eight analog inputs can be configured as eight single-ended inputs, four true differential inputs, four pseudo differential inputs, or seven pseudo differential inputs.
3. 500 kSPS serial interface. SPI<sup>®</sup>-/QSPI<sup>™</sup>-/DSP-/MICROWIRE<sup>™</sup>-compatible interface.
4. Low power, 18 mW, at a maximum throughput rate of 500 kSPS.
5. Channel sequencer.

## TABLE OF CONTENTS

|                                 |   |  |    |
|---------------------------------|---|--|----|
| Features .....                  | 1 | Absolute Maximum Ratings .....                   | 8  |
| Enhanced Product Features ..... | 1 | ESD Caution.....                                 | 8  |
| General Description .....       | 1 | Pin Configuration and Function Descriptions..... | 9  |
| Functional Block Diagram .....  | 1 | Typical Performance Characteristics .....        | 10 |
| Product Highlights .....        | 1 | Outline Dimensions .....                         | 14 |
| Revision History .....          | 2 | Ordering Guide .....                             | 14 |
| Specifications.....             | 3 |  |    |
| Timing Specifications .....     | 7 |  |    |

## REVISION HISTORY

### 4/2018—Rev. B to Rev. C

|                                  |    |
|----------------------------------|----|
| Changes to Features Section..... | 1  |
| Changes to Ordering Guide .....  | 14 |

### 9/2015—Rev. A to Rev. B

|  |   |
|--|---|
| Added Enhanced Product Features Section..... | 1 |
|--|---|

### 10/2014—Rev. 0 to Rev. A

|   |   |
|---|---|
| Changes to Operating Temperature Range, Table 3 ..... | 8 |
|---|---|

### 9/2014—Revision 0: Initial Version

## SPECIFICATIONS

$V_{DD} = 12\text{ V to }16.5\text{ V}$ ,  $V_{SS} = -12\text{ V to }-16.5\text{ V}$ ,  $V_{CC} = 2.7\text{ V to }5.25\text{ V}$ ,  $V_{DRIVE} = 2.7\text{ V to }5.25\text{ V}$ ,  $V_{REF} = 2.5\text{ V to }3.0\text{ V}$  internal/external,  $f_{SCLK} = 10\text{ MHz}$ ,  $f_s = 500\text{ kSPS}$ ,  $T_A = T_{MAX}$  to  $T_{MIN}$ , unless otherwise noted.

Table 1.

| Parameter <sup>1</sup>                              | Min                | Typ | Max   | Unit | Test Conditions/Comments   |
|---|--------------------|-----|-------|------|--|
| <b>DYNAMIC PERFORMANCE</b>                          |                    |     |       |      |  |
| Signal-to-Noise Ratio (SNR) <sup>2</sup>            | 76                 |     |       | dB   | $f_{IN} = 50\text{ kHz}$ sine wave<br>Differential mode, $V_{CC} = 4.75\text{ V to }5.25\text{ V}$   |
|   | 75.5               |     |       | dB   | Differential mode, $V_{CC} < 4.75\text{ V}$  |
|   | 72                 |     |       | dB   | Single-ended/pseudo differential mode; $\pm 10\text{ V}$ ,<br>$\pm 2.5\text{ V}$ and $\pm 5\text{ V}$ ranges, $V_{CC} = 4.75\text{ V to }5.25\text{ V}$    |
|   | 71.7               |     |       | dB   | Single-ended/pseudo differential mode; $0\text{ V to }10\text{ V}$<br>$V_{CC} = 4.75\text{ V to }5.25\text{ V}$ and all ranges at $V_{CC} < 4.75\text{ V}$ |
| Signal-to-Noise + Distortion (SINAD) <sup>2</sup>   | 75                 |     |       | dB   | Differential mode; $\pm 2.5\text{ V}$ and $\pm 5\text{ V}$ ranges  |
|   | 74                 |     |       | dB   | Differential mode; $0\text{ V to }10\text{ V}$   |
|   | 70.7               | 76  |       | dB   | Differential mode; $\pm 10\text{ V}$ range   |
|   |                    |     | 72.5  | dB   | Single-ended/pseudo differential mode; $\pm 2.5\text{ V}$ and<br>$\pm 5\text{ V}$ ranges   |
| Total Harmonic Distortion (THD) <sup>2</sup>        |                    |     | -79.3 | dB   | Single-ended/pseudo differential mode; $0\text{ V to }+10\text{ V}$<br>and $\pm 10\text{ V}$ ranges  |
|   |                    |     | -78.8 | dB   | Differential mode; $\pm 2.5\text{ V}$ and $\pm 5\text{ V}$ ranges  |
|   |                    | -82 |       | dB   | Differential mode; $0\text{ V to }10\text{ V}$ ranges  |
|   |                    |     | -76   | dB   | Differential mode; $\pm 10\text{ V}$ range   |
|   |                    |     | -77.3 | dB   | Single-ended/pseudo differential mode; $\pm 5\text{ V}$ range  |
|   |                    | -80 |       | dB   | Single-ended/pseudo differential mode; $\pm 2.5\text{ V}$ range  |
| Peak Harmonic or Spurious Noise (SFDR) <sup>2</sup> |                    |     | -80   | dB   | Single-ended/pseudo differential mode; $0\text{ V to }+10\text{ V}$<br>and $\pm 10\text{ V}$ ranges  |
|   |                    |     | -80   | dB   | Differential mode; $\pm 2.5\text{ V}$ and $\pm 5\text{ V}$ ranges  |
|   |                    | -82 |       | dB   | Differential mode; $0\text{ V to }10\text{ V}$ ranges  |
|   |                    |     | -77.2 | dB   | Differential mode; $\pm 10\text{ V}$ ranges  |
|   |                    |     | -78.9 | dB   | Single-ended/pseudo differential mode; $\pm 5\text{ V}$ range  |
|   |                    | -79 |       | dB   | Single-ended/pseudo differential mode; $\pm 2.5\text{ V}$ range  |
| Intermodulation Distortion (IMD) <sup>2</sup>       |                    |     |       |      | Single-ended/pseudo differential mode; $0\text{ V to }+10\text{ V}$<br>and $\pm 10\text{ V}$ ranges<br>$f_A = 50\text{ kHz}$ , $f_B = 30\text{ kHz}$       |
|   | Second-Order Terms | -88 |       | dB   |  |
|   | Third-Order Terms  | -90 |       | dB   |  |
| Aperture Delay <sup>3</sup>                         |                    | 7   |       | ns   |  |
| Aperture Jitter <sup>3</sup>                        |                    | 50  |       | ps   |  |
| Common-Mode Rejection (CMRR) <sup>2</sup>           |                    | -79 |       | dB   | Up to $100\text{ kHz}$ ripple frequency; see Figure 17   |
| Channel-to-Channel Isolation <sup>2</sup>           |                    | -72 |       | dB   | $f_{IN}$ on unselected channels up to $100\text{ kHz}$ ; see Figure 14   |
| Full Power Bandwidth                                |                    | 22  |       | MHz  | At $3\text{ dB}$   |
|   |                    | 5   |       | MHz  | At $0.1\text{ dB}$   |

| Parameter <sup>1</sup>  | Min                        | Typ       | Max        | Unit | Test Conditions/Comments   |
|---|----------------------------|-----------|------------|------|--|
| DC ACCURACY <sup>4</sup>  |                            |           |            |      | Single-ended/pseudo differential mode 1 LSB = FSR/4096, unless otherwise noted; differential mode 1 LSB = FSR/8192, unless otherwise noted |
| Resolution  | 13                         |           |            | Bits |  |
| No Missing Codes  | 12-bit plus sign (13 bits) |           |            | Bits | Differential mode  |
|   | 11-bit plus sign (12 bits) |           |            | Bits | Single-ended/pseudo differential mode  |
| Integral Nonlinearity <sup>2</sup>                                    |                            |           | ±1.25      | LSB  | Differential mode; V <sub>CC</sub> = 3 V to 5.25 V, typical for V <sub>CC</sub> = 2.7 V  |
|   |                            |           | ±1.2       | LSB  | Single-ended/pseudo differential mode, V <sub>CC</sub> = 3 V to 5.25 V, typical for V <sub>CC</sub> = 2.7 V                                |
|   |                            | -0.7/+1.2 |            | LSB  | Single-ended/pseudo differential mode (LSB = FSR/8192)   |
| Differential Nonlinearity <sup>2</sup>                                |                            |           | -0.99/+1.2 | LSB  | Differential mode; guaranteed no missing codes to 13 bits  |
|   |                            |           | ±0.99      | LSB  | Single-ended mode; guaranteed no missing codes to 12 bits  |
|   |                            | -0.7/+1   |            | LSB  | Single-ended/pseudo differential mode (LSB = FSR/8192)   |
| Offset Error <sup>2,5</sup>   |                            |           | -6/+10     | LSB  | Single-ended/pseudo differential mode  |
|   |                            |           | -7/+11     | LSB  | Differential mode  |
| Offset Error Match <sup>2,5</sup>                                     |                            |           | ±0.8       | LSB  | Single-ended/pseudo differential mode  |
|   |                            |           | ±0.5       | LSB  | Differential mode  |
| Gain Error <sup>2,5</sup>   |                            |           | ±8         | LSB  | Single-ended/pseudo differential mode  |
|   |                            |           | ±15        | LSB  | Differential mode  |
| Gain Error Match <sup>2,5</sup>                                       |                            |           | ±0.5       | LSB  | Single-ended/pseudo differential mode  |
|   |                            |           | ±0.5       | LSB  | Differential mode  |
| Positive Full-Scale Error <sup>2,6</sup>                              |                            |           | ±4         | LSB  | Single-ended/pseudo differential mode  |
|   |                            |           | ±8         | LSB  | Differential mode  |
| Positive Full-Scale Error Match <sup>2,6</sup>                        |                            |           | ±0.5       | LSB  | Single-ended/pseudo differential mode  |
|   |                            |           | ±0.5       | LSB  | Differential mode  |
| Bipolar Zero Error <sup>2,6</sup>                                     |                            |           | ±9         | LSB  | Single-ended/pseudo differential mode  |
|   |                            |           | ±8         | LSB  | Differential mode  |
| Bipolar Zero Error Match <sup>2,6</sup>                               |                            |           | ±0.5       | LSB  | Single-ended/pseudo differential mode  |
|   |                            |           | ±0.5       | LSB  | Differential mode  |
| Negative Full-Scale Error <sup>2,6</sup>                              |                            |           | ±4         | LSB  | Single-ended/pseudo differential mode  |
|   |                            |           | ±7         | LSB  | Differential mode  |
| Negative Full-Scale Error Match <sup>2,6</sup>                        |                            |           | ±0.5       | LSB  | Single-ended/pseudo differential mode  |
|   |                            |           | ±0.5       | LSB  | Differential mode  |
| ANALOG INPUT  |                            |           |            |      |  |
| Input Voltage Ranges <sup>2</sup><br>(Programmed via Range Registers) |                            | ±10       |            | V    | Reference = 2.5 V<br>V <sub>DD</sub> = +10 V min, V <sub>SS</sub> = -10 V min, V <sub>CC</sub> = +2.7 V to +5.25 V                         |
|   |                            | ±5        |            | V    | V <sub>DD</sub> = +5 V min, V <sub>SS</sub> = -5 V min, V <sub>CC</sub> = +2.7 V to +5.25 V  |
|   |                            | ±2.5      |            | V    | V <sub>DD</sub> = +5 V min, V <sub>SS</sub> = -5 V min, V <sub>CC</sub> = +2.7 V to +5.25 V  |
|   |                            | 0 to 10   |            | V    | V <sub>DD</sub> = +10 V min, V <sub>SS</sub> = AGND min, V <sub>CC</sub> = +2.7 V to +5.25 V   |
| Pseudo Differential V <sub>IN(-)</sub><br>Input Range <sup>2</sup>    |                            | ±3.5      |            | V    | V <sub>DD</sub> = +16.5 V, V <sub>SS</sub> = -16.5 V, V <sub>CC</sub> = +5 V<br>Reference = 2.5 V; range = ±10 V                           |
|   |                            | ±6        |            | V    | Reference = 2.5 V; range = ±5 V  |
|   |                            | ±5        |            | V    | Reference = 2.5 V; range = ±2.5 V  |
|   |                            | +3/-5     |            | V    | Reference = 2.5 V; range = 0 V to +10 V  |

| Parameter <sup>1</sup>                          | Min                 | Typ  | Max   | Unit   | Test Conditions/Comments   |
|---|---------------------|--|-------|--------|--|
| DC Leakage Current                              |                     | 3  | ±80   | nA     | $V_{IN} = V_{DD}$ or $V_{SS}$  |
| Input Capacitance <sup>3</sup>                  |                     | 13.5                                       |       | nA     | Per input channel, $V_{IN} = V_{DD}$ or $V_{SS}$                                   |
|   |                     | 16.5                                       |       | pF     | When in track, ±10 V range   |
|   |                     | 21.5                                       |       | pF     | When in track, ±5 V and 0 V to +10 V ranges  |
|   |                     | 3  |       | pF     | When in track, ±2.5 V range  |
|   |                     |  |       |        | When in hold, all ranges   |
| REFERENCE INPUT/OUTPUT                          |                     |  |       |        |  |
| Input Voltage Range                             | 2.5                 |  | 3     | V      |  |
| Input DC Leakage Current                        |                     |  | ±1    | μA     |  |
| Input Capacitance                               |                     | 10   |       | pF     |  |
| Reference Output Voltage                        |                     | 2.5  |       | V      |  |
| Reference Output Voltage Error at 25°C          |                     |  | ±5    | mV     |  |
| Reference Output Voltage $T_{MIN}$ to $T_{MAX}$ |                     |  | ±10   | mV     |  |
| Reference Temperature Coefficient               |                     |  | 25    | ppm/°C |  |
|   |                     | 3  |       | ppm/°C |  |
| Reference Output Impedance                      |                     | 7  |       | Ω      |  |
| LOGIC INPUTS                                    |                     |  |       |        |  |
| Input High Voltage, $V_{INH}$                   | 2.4                 |  |       | V      |  |
| Input Low Voltage, $V_{INL}$                    |                     |  | 0.8   | V      | $V_{CC} = 4.75$ V to 5.25 V  |
|   |                     |  | 0.4   | V      | $V_{CC} = 2.7$ to 3.6 V  |
| Input Current, $I_{IN}$                         |                     |  | ±1    | μA     | $V_{IN} = 0$ V or $V_{DRIVE}$  |
| Input Capacitance, $C_{IN}^3$                   |                     | 10   |       | pF     |  |
| LOGIC OUTPUTS                                   |                     |  |       |        |  |
| Output High Voltage, $V_{OH}$                   | $V_{DRIVE} - 0.2$ V |  |       | V      | $I_{SOURCE} = 200$ μA  |
| Output Low Voltage, $V_{OL}$                    |                     |  | 0.4   | V      | $I_{SINK} = 200$ μA  |
| Floating-State Leakage Current                  |                     |  | ±1    | μA     |  |
| Floating-State Output Capacitance <sup>3</sup>  |                     | 5  |       | pF     |  |
| Output Coding                                   |                     | Straight natural binary<br>Twos complement |       |        | Coding bit set to 1 in control register<br>Coding bit set to 0 in control register |
| CONVERSION RATE                                 |                     |  |       |        |  |
| Conversion Time                                 |                     |  | 1.6   | μs     | 16 SCLK cycles with SCLK = 10 MHz  |
| Track-and-Hold Acquisition Time <sup>2,3</sup>  |                     |  | 305   | ns     | Full-scale step input  |
| Throughput Rate                                 |                     |  | 500   | kSPS   |  |
| POWER REQUIREMENTS                              |                     |  |       |        |  |
| $V_{DD}^2$                                      | 12                  |  | 16.5  | V      | Digital inputs = 0 V or $V_{DRIVE}$  |
| $V_{SS}^2$                                      | -12                 |  | -16.5 | V      |  |
| $V_{CC}^2$                                      | 2.7                 |  | 5.25  | V      |  |
| $V_{DRIVE}$                                     | 2.7                 |  | 5.25  | V      |  |
| Normal Mode (Static)                            |                     | 0.9  |       | mA     | $V_{DD}/V_{SS} = ±16.5$ V, $V_{CC}/V_{DRIVE} = 5.25$ V                             |
| Normal Mode (Operational)                       |                     |  |       |        | $f_{SAMPLE} = 500$ kSPS  |
| $I_{DD}$  |                     |  | 195   | μA     | $V_{DD} = 16.5$ V  |
| $I_{SS}$  |                     |  | 215   | μA     | $V_{SS} = -16.5$ V   |
| $I_{CC}$ and $I_{DRIVE}$                        |                     |  | 2.3   | mA     | $V_{CC}/V_{DRIVE} = 5.25$ V  |
| Autostandby Mode (Dynamic)                      |                     |  |       |        | $f_{SAMPLE} = 250$ kSPS  |
| $I_{DD}$  |                     |  | 100   | μA     | $V_{DD} = 16.5$ V  |
| $I_{SS}$  |                     |  | 110   | μA     | $V_{SS} = -16.5$ V   |
| $I_{CC}$ and $I_{DRIVE}$                        |                     |  | 0.87  | mA     | $V_{CC}/V_{DRIVE} = 5.25$ V  |

| Parameter <sup>1</sup>                 | Min | Typ | Max   | Unit | Test Conditions/Comments  |
|--|-----|-----|-------|------|---|
| Autoshutdown Mode (Static)             |     |     |       |      | SCLK on or off  |
| I <sub>DD</sub>                        |     |     | 1     | μA   | V <sub>DD</sub> = 16.5 V  |
| I <sub>SS</sub>                        |     |     | 1     | μA   | V <sub>SS</sub> = -16.5 V   |
| I <sub>CC</sub> and I <sub>DRIVE</sub> |     |     | 1     | μA   | V <sub>CC</sub> /V <sub>DRIVE</sub> = 5.25 V                                    |
| Full Shutdown Mode                     |     |     |       |      | SCLK on or off  |
| I <sub>DD</sub>                        |     |     | 1     | μA   | V <sub>DD</sub> = 16.5 V  |
| I <sub>SS</sub>                        |     |     | 1     | μA   | V <sub>SS</sub> = -16.5 V   |
| I <sub>CC</sub> and I <sub>DRIVE</sub> |     |     | 1     | μA   | V <sub>CC</sub> /V <sub>DRIVE</sub> = 5.25 V                                    |
| POWER DISSIPATION                      |     |     |       |      |   |
| Normal Mode (Operational)              |     |     | 19    | mW   | V <sub>DD</sub> = +16.5 V, V <sub>SS</sub> = -16.5 V, V <sub>CC</sub> = +5.25 V |
| Full Shutdown Mode                     |     |     | 38.25 | μW   | V <sub>DD</sub> = +16.5 V, V <sub>SS</sub> = -16.5 V, V <sub>CC</sub> = +5.25 V |

<sup>1</sup> Temperature range is -55°C to +125°C.

<sup>2</sup> See the terminology section of the [AD7327](#) data sheet.

<sup>3</sup> Sample tested during initial release to ensure compliance.

<sup>4</sup> For dc accuracy specifications, the LSB size for differential mode is FSR/8192. For single-ended mode/pseudo differential mode, the LSB size is FSR/4096, unless otherwise noted.

<sup>5</sup> Unipolar 0 V to 10 V range with straight binary output coding.

<sup>6</sup> Bipolar range with twos complement output coding.

**TIMING SPECIFICATIONS**

$V_{DD} = 1.2\text{ V to }16.5\text{ V}$ ,  $V_{SS} = -12\text{ V to }-16.5\text{ V}$ ,  $V_{CC} = 2.7\text{ V to }5.25\text{ V}$ ,  $V_{DRIVE} = 2.7\text{ V to }5.25\text{ V}$ ,  $V_{REF} = 2.5\text{ V to }3.0\text{ V}$  internal/external,  $T_A = T_{MAX}$  to  $T_{MIN}$ . Timing specifications apply with a 32 pF load, unless otherwise noted. Sample tested during initial release to ensure compliance. All input signals are specified with  $t_r = t_f = 5\text{ ns}$  (10% to 90% of  $V_{DRIVE}$ ) and timed from a voltage level of 1.6 V.

**Table 2.**

| Parameter      | Limit at $T_{MIN}, T_{MAX}$ |   | Unit              | Description<br>$V_{DRIVE} \leq V_{CC}$  |
|----------------|-----------------------------|---|-------------------|---|
|                | $V_{CC} < 4.75\text{ V}$    | $V_{CC} = 4.75\text{ V to }5.25\text{ V}$ |                   |   |
| $f_{SCLK}$     | 50                          | 50  | kHz min           |   |
|                | 10                          | 10  | MHz max           |   |
| $t_{CONVERT}$  | $16 \times t_{SCLK}$        | $16 \times t_{SCLK}$                      | ns max            | $t_{SCLK} = 1/f_{SCLK}$   |
| $t_{QUIET}$    | 75                          | 60  | ns min            | Minimum time between end of serial read and next falling edge of $\overline{CS}$  |
| $t_1$          | 12                          | 5   | ns min            | Minimum $\overline{CS}$ pulse width   |
| $t_2^1$        | 25                          | 20  | ns min            | $\overline{CS}$ to SCLK set-up time; bipolar input ranges ( $\pm 10\text{ V}$ , $\pm 5\text{ V}$ , $\pm 2.5\text{ V}$ ) |
|                | 45                          | 35  | ns min            | Unipolar input range (0 V to 10 V)  |
| $t_3$          | 26                          | 14  | ns max            | Delay from $\overline{CS}$ until DOUT three-state disabled  |
| $t_4$          | 57                          | 43  | ns max            | Data access time after SCLK falling edge  |
| $t_5$          | $0.4 \times t_{SCLK}$       | $0.4 \times t_{SCLK}$                     | ns min            | SCLK low pulse width  |
| $t_6$          | $0.4 \times t_{SCLK}$       | $0.4 \times t_{SCLK}$                     | ns min            | SCLK high pulse width   |
| $t_7$          | 13                          | 8   | ns min            | SCLK to data valid hold time  |
| $t_8$          | 40                          | 22  | ns max            | SCLK falling edge to DOUT high impedance  |
|                | 10                          | 9   | ns min            | SCLK falling edge to DOUT high impedance  |
| $t_9$          | 4                           | 4   | ns min            | DIN set-up time prior to SCLK falling edge  |
| $t_{10}$       | 2                           | 2   | ns min            | DIN hold time after SCLK falling edge   |
| $t_{POWER-UP}$ | 750                         | 750                                       | ns max            | Power-up from autostandby   |
|                | 500                         | 500                                       | $\mu\text{s}$ max | Power-up from full shutdown/autoshtutdown mode, internal reference  |
|                | 25                          | 25  | $\mu\text{s}$ typ | Power-up from full shutdown/autoshtutdown mode, external reference  |

<sup>1</sup> When using the 0 V to 10 V unipolar range, running at 500 kSPS throughput rate with  $t_2$  at 20 ns, the mark space ratio needs to be limited to 50:50.

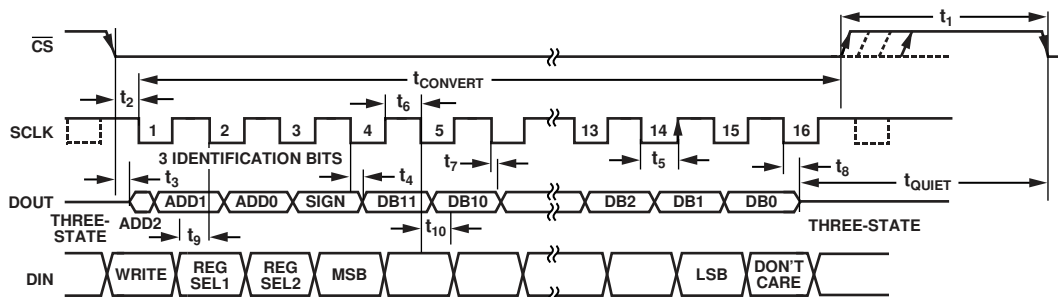


Figure 2. Serial Interface Timing Diagram

12481-002

## ABSOLUTE MAXIMUM RATINGS

$T_A = 25^\circ\text{C}$ , unless otherwise noted.

Table 3.

| Parameter   | Rating                               |
|---|--------------------------------------|
| $V_{DD}$ to AGND, DGND                                | -0.3 V to +16.5 V                    |
| $V_{SS}$ to AGND, DGND                                | +0.3 V to -16.5 V                    |
| $V_{DD}$ to $V_{CC}$                                  | $V_{CC} - 0.3$ V to +16.5 V          |
| $V_{CC}$ to AGND, DGND                                | -0.3 V to +7 V                       |
| $V_{DRIVE}$ to AGND, DGND                             | -0.3 V to +7 V                       |
| AGND to DGND  | -0.3 V to +0.3 V                     |
| Analog Input Voltage to AGND                          | $V_{SS} - 0.3$ V to $V_{DD} + 0.3$ V |
| Digital Input Voltage to DGND                         | -0.3 V to +7 V                       |
| Digital Output Voltage to GND                         | -0.3 V to $V_{DRIVE} + 0.3$ V        |
| REFIN to AGND   | -0.3 V to $V_{CC} + 0.3$ V           |
| Input Current to Any Pin Except Supplies <sup>1</sup> | $\pm 10$ mA                          |
| Operating Temperature Range                           | -55°C to +125°C                      |
| Storage Temperature Range                             | -65°C to +150°C                      |
| Junction Temperature                                  | 150°C                                |
| Thermal Impedance                                     |                                      |
| $\theta_{JA}$   | 143°C/W                              |
| $\theta_{JC}$   | 45°C/W                               |
| Pb-Free Temperature, Soldering                        |                                      |
| Reflow  | 260(0)°C                             |
| ESD   | 2.5 kV                               |

<sup>1</sup> Transient currents of up to 100 mA do not cause SCR latch-up.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

### ESD CAUTION



**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.



## PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

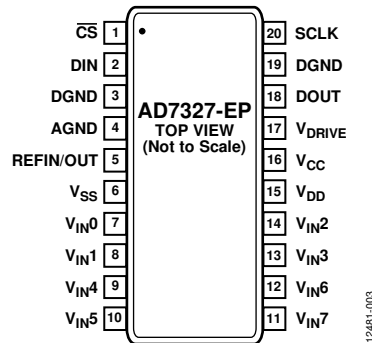


Figure 3. Pin Configuration

Table 4. Pin Function Descriptions

| Pin No. | Mnemonic                             | Description   |
|---------|--------------------------------------|---|
| 1       | CS                                   | Chip Select. Active low logic input. This input provides the dual function of initiating conversions on the AD7327-EP and frames the serial data transfer.  |
| 2       | DIN                                  | Data In. Data to be written to the on-chip registers is provided on this input and is clocked into the AD7327-EP on the falling edge of SCLK (see the Registers section of <a href="#">AD7327</a> data sheet).  |
| 3, 19   | DGND                                 | Digital Ground. Ground reference point for all digital circuitry on the AD7327-EP. The DGND and AGND voltages, ideally, share the same potential and must not be more than 0.3 V apart, even on a transient basis.  |
| 4       | AGND                                 | Analog Ground. Ground reference point for all analog circuitry on the AD7327-EP. Refer all analog input signals and any external reference signal to this AGND voltage. The AGND and DGND voltages, ideally, share the same potential and must not be more than 0.3 V apart, even on a transient basis.   |
| 5       | REFIN/OUT                            | Reference Input/Reference Output. The on-chip reference is available on this pin for external use to the AD7327-EP. The nominal internal reference voltage is 2.5 V, which appears at this pin. Place a 680 nF capacitor on the reference pin (see the Reference section of the <a href="#">AD7327</a> data sheet). Alternatively, the internal reference can be disabled and an external reference applied to this input. On power-up, the external reference mode is the default condition.   |
| 6       | V <sub>SS</sub>                      | Negative Power Supply Voltage. V <sub>SS</sub> is the negative supply voltage for the analog input section.   |
| 7 to 14 | V <sub>IN0</sub> to V <sub>IN7</sub> | Analog Input 0 to Analog Input 7. The analog inputs are multiplexed into the on-chip track-and-hold. The analog input channel for conversion is selected by programming the Channel Address Bit ADD2 through Channel Address Bit ADD0 in the control register. The inputs can be configured as eight single-ended inputs, four true differential input pairs, four pseudo differential inputs, or seven pseudo differential inputs. The configuration of the analog inputs is selected by programming the mode bits, Bit Mode 1 and Bit Mode 0, in the control register. The input range on each input channel is controlled by programming the range registers. Input ranges of ±10 V, ±5 V, ±2.5 V, and 0 V to +10 V can be selected on each analog input channel when a +2.5 V reference voltage is used (see the Registers section of <a href="#">AD7327</a> data sheet). |
| 15      | V <sub>DD</sub>                      | Positive Power Supply Voltage. V <sub>DD</sub> is the positive supply voltage for the analog input section.   |
| 16      | V <sub>CC</sub>                      | Analog Supply Voltage, 2.7 V to 5.25 V. V <sub>CC</sub> is the supply voltage for the ADC core on the AD7327-EP. Decouple this supply to AGND.  |
| 17      | V <sub>DRIVE</sub>                   | Logic Power Supply Input. The voltage supplied at this pin determines at what voltage the interface operates. Decouple this pin to DGND. The voltage at this pin may be different to that at V <sub>CC</sub> , but V <sub>DRIVE</sub> must not exceed V <sub>CC</sub> by more than 0.3 V.   |
| 18      | DOUT                                 | Serial Data Output. The conversion output data is supplied to this pin as a serial data stream. The bits are clocked out on the falling edge of the SCLK input, and 16 SCLKs are required to access the data. The data stream consists of three channel identification bits, the sign bit, and 12 bits of conversion data. The data is provided MSB first (see the Serial Interface section of <a href="#">AD7327</a> data sheet).  |
| 20      | SCLK                                 | Serial Clock, Logic Input. A serial clock input provides the SCLK used for accessing the data from the AD7327-EP. This clock is also used as the clock source for the conversion process.   |

# TYPICAL PERFORMANCE CHARACTERISTICS

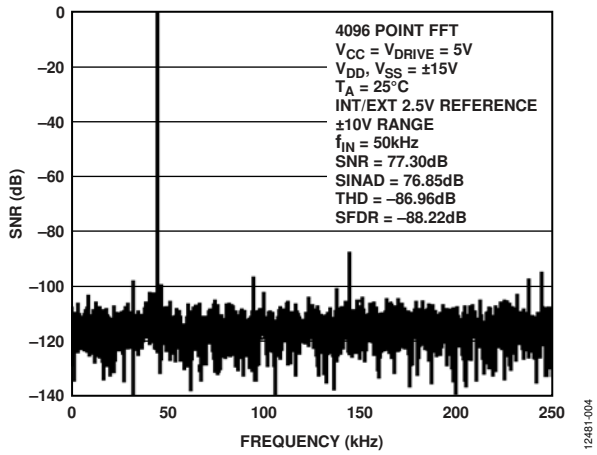


Figure 4. FFT True Differential Mode

12481-004

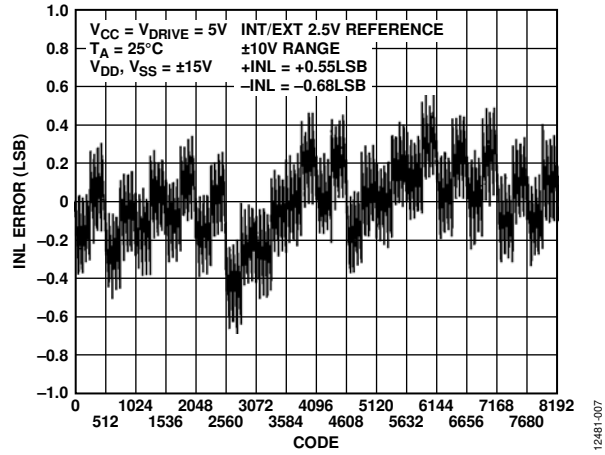


Figure 7. Typical INL True Differential Mode

12481-007

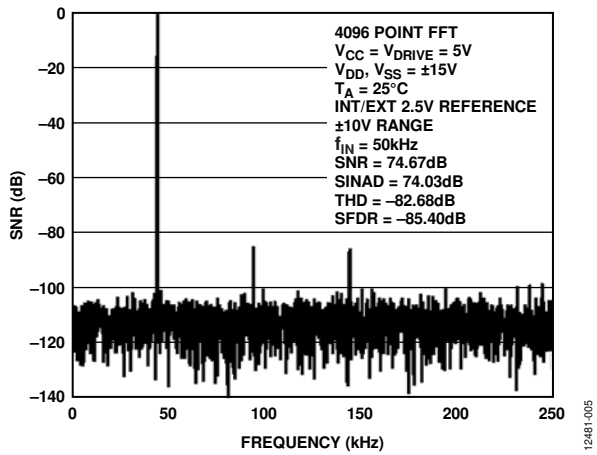


Figure 5. FFT Single-Ended Mode

12481-005

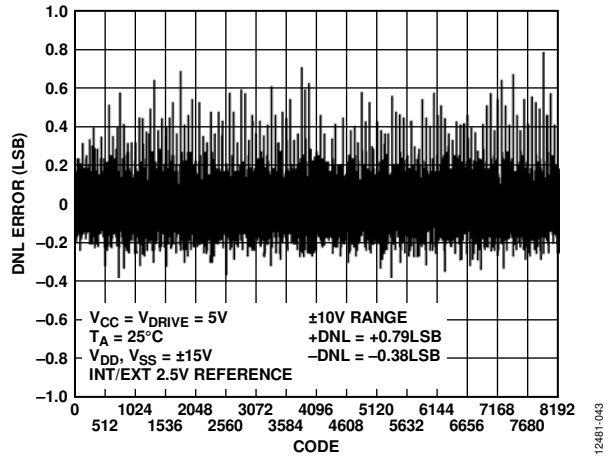


Figure 8. Typical DNL Single-Ended Mode

12481-003

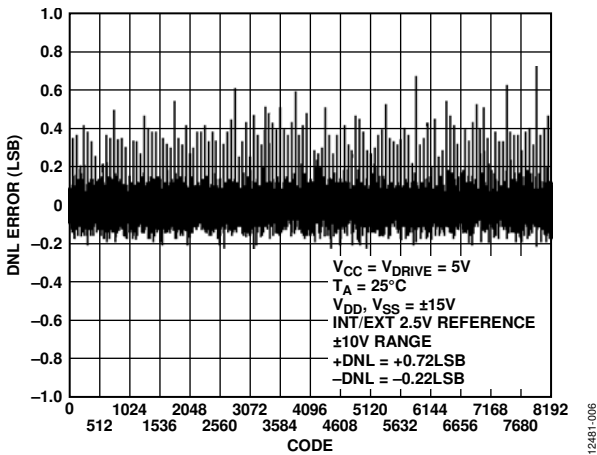


Figure 6. Typical DNL True Differential Mode

12481-006

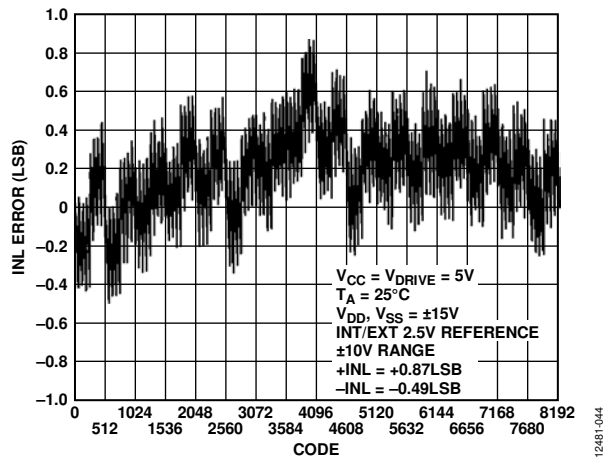


Figure 9. Typical INL Single-Ended Mode

12481-004

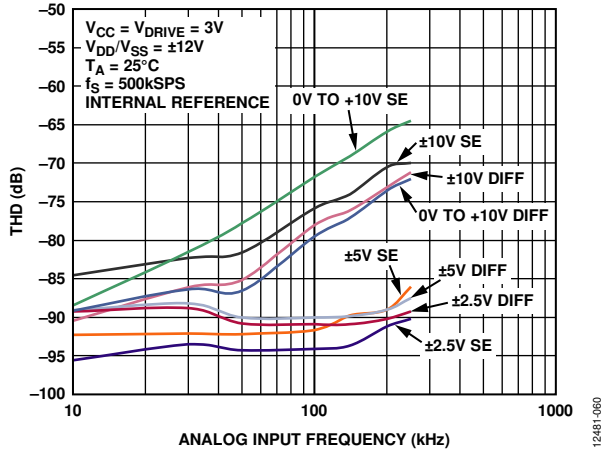


Figure 10. THD vs. Analog Input Frequency for Single-Ended (SE) and True Differential (Diff) Mode at 3 V  $V_{CC}$

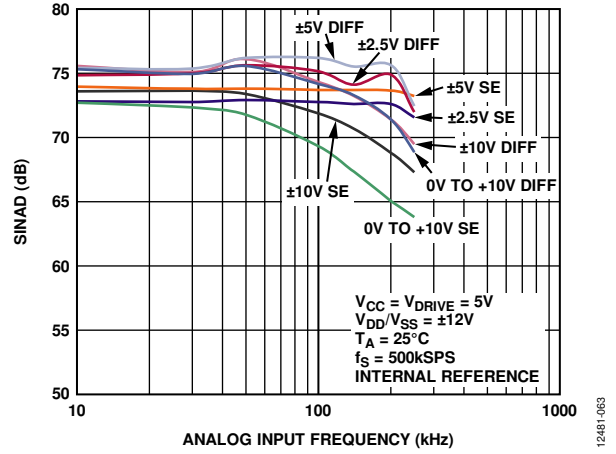


Figure 13. SINAD vs. Analog Input Frequency for Single-Ended (SE) and True Differential (Diff) Mode at 5 V  $V_{CC}$

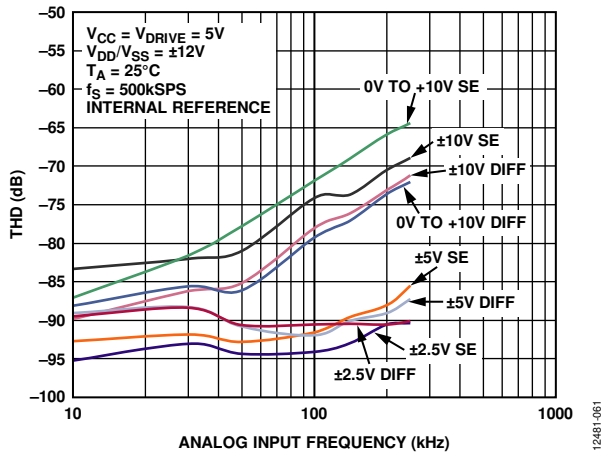


Figure 11. THD vs. Analog Input Frequency for Single-Ended (SE) and True Differential (Diff) Mode at 5 V  $V_{CC}$

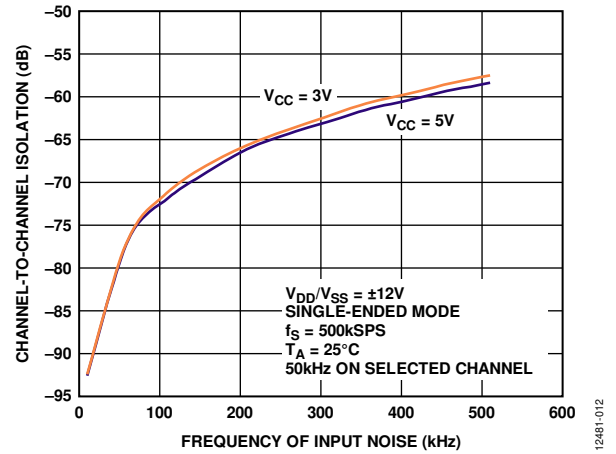


Figure 14. Channel-to-Channel Isolation

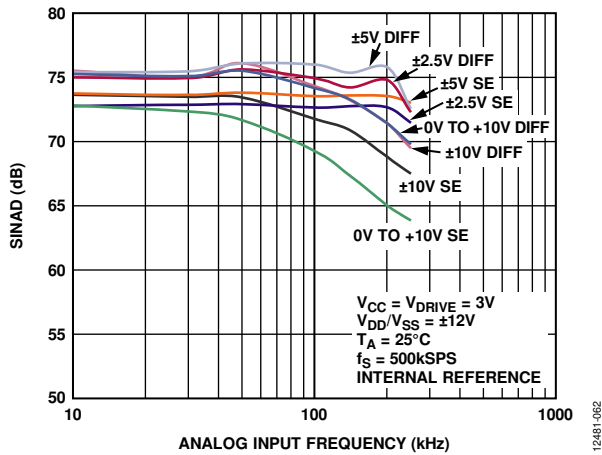


Figure 12. SINAD vs. Analog Input Frequency for Single-Ended (SE) and True Differential (Diff) Mode at 3 V  $V_{CC}$

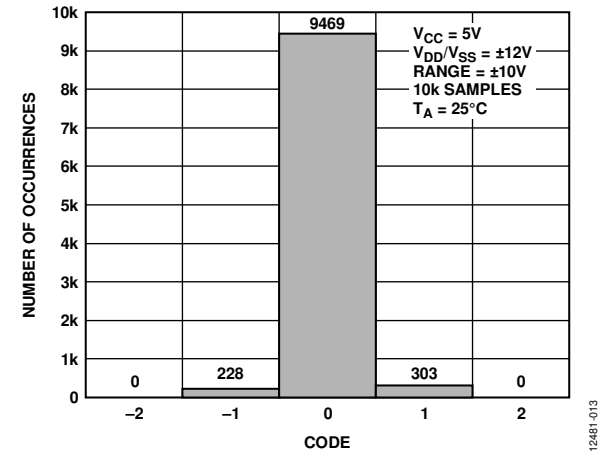


Figure 15. Histogram of Codes, True Differential Mode

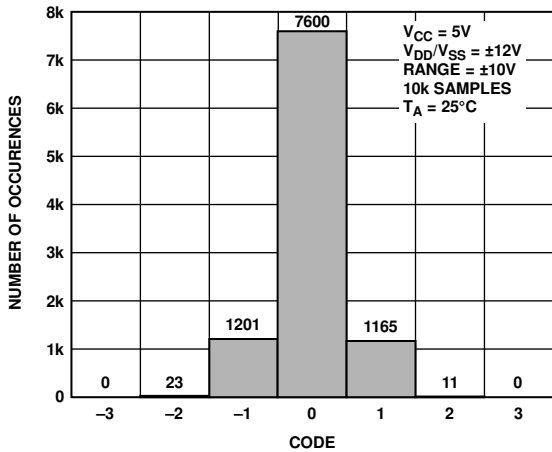


Figure 16. Histogram of Codes, Single-Ended Mode

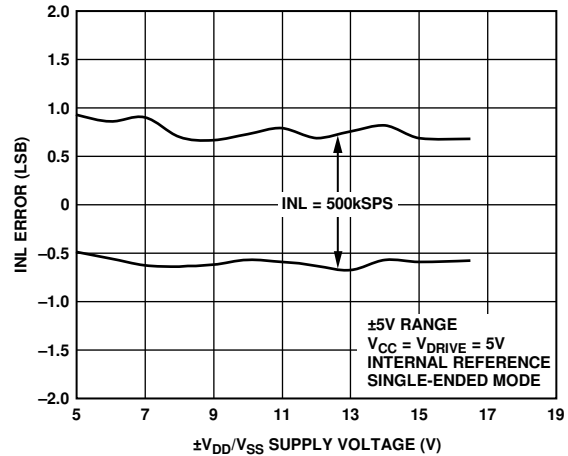


Figure 19. INL Error vs.  $\pm V_{DD}/V_{SS}$  Supply Voltage at 500 kSPS

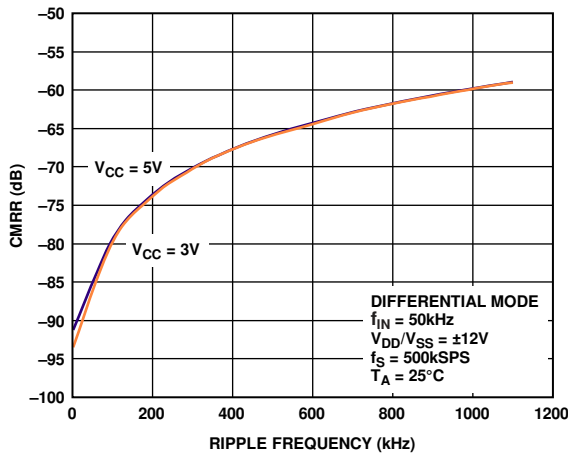


Figure 17. CMRR vs. Common-Mode Ripple Frequency

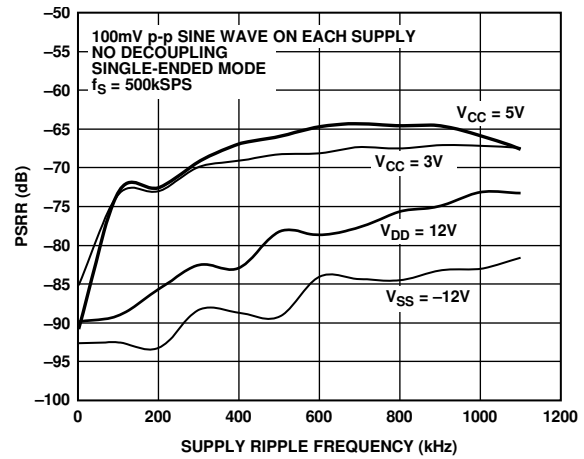


Figure 20. PSRR vs. Supply Ripple Frequency Without Supply Decoupling

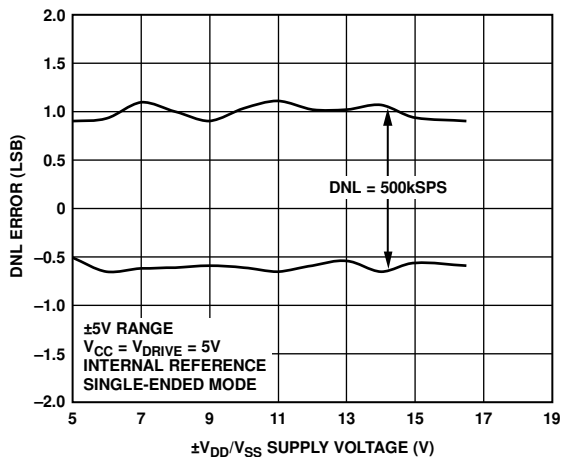


Figure 18. DNL Error vs.  $\pm V_{DD}/V_{SS}$  Supply Voltage at 500 kSPS

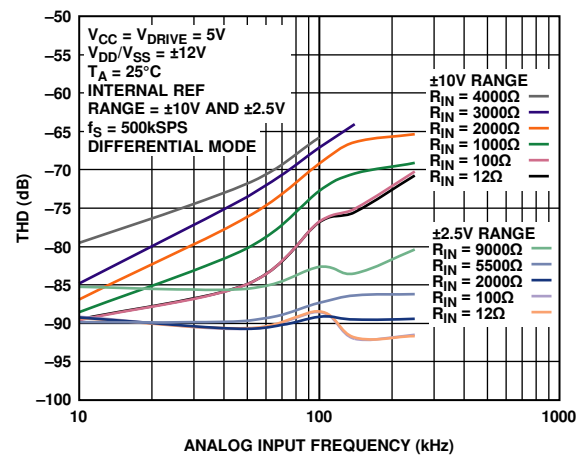


Figure 21. THD vs. Analog Input Frequency for Various Source Impedances, True Differential Mode

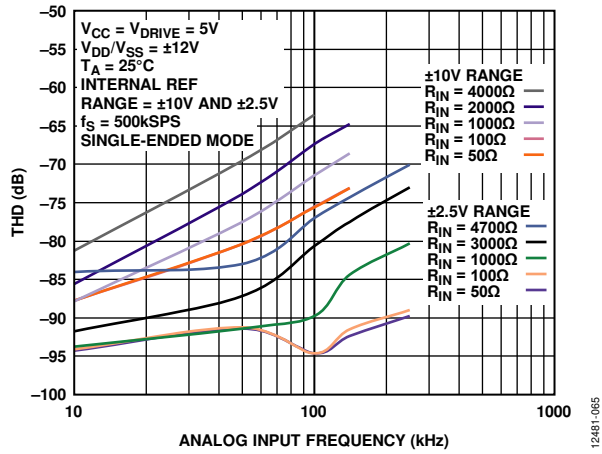
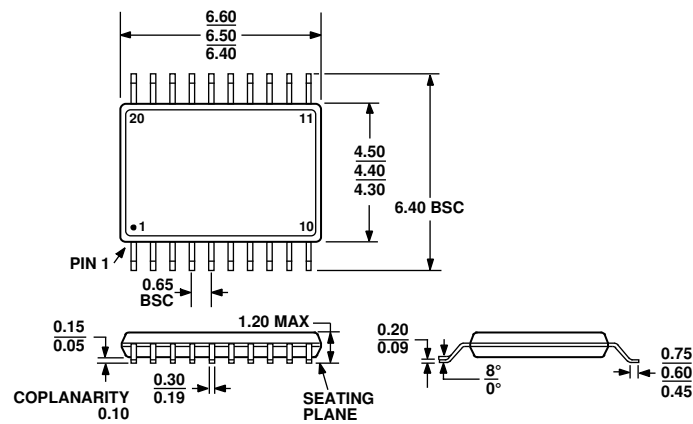


Figure 22. THD vs. Analog Input Frequency for Various Source Impedances, Single-Ended Mode

## OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-153-AC

Figure 23. 20-Lead Thin Shrink Small Outline Package [TSSOP]  
(RU-20)

Dimensions show in millimeters

## ORDERING GUIDE

| Model <sup>1</sup> | Temperature Range | Package Description                               | Package Option |
|--------------------|-------------------|---|----------------|
| AD7327TRU-EP       | -55°C to +125°C   | 20-Lead Thin Shrink Small Outline Package [TSSOP] | RU-20          |
| AD7327TRU-EP-RL7   | -55°C to +125°C   | 20-Lead Thin Shrink Small Outline Package [TSSOP] | RU-20          |
| AD7327TRUZ-EP      | -55°C to +125°C   | 20-Lead Thin Shrink Small Outline Package [TSSOP] | RU-20          |
| AD7327TRUZ-EP-RL7  | -55°C to +125°C   | 20-Lead Thin Shrink Small Outline Package [TSSOP] | RU-20          |

<sup>1</sup> Z = RoHS Compliant Part.