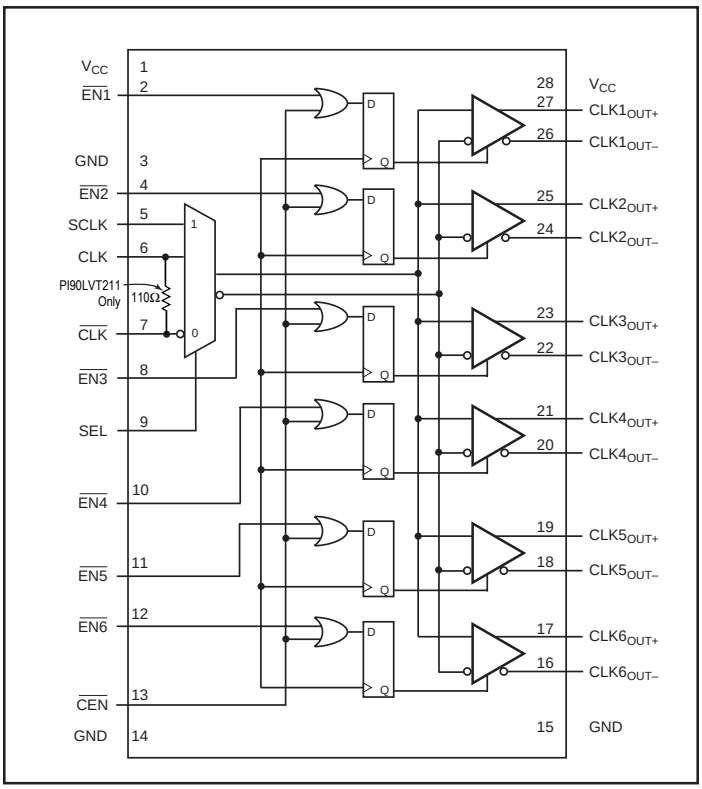
1:6 Differential Clock Distribution Chip

Features

- Meets or Exceeds Requirements of ANSI TIA/EIA-644-1995
- Designed for Clocking Rates up to 320MHz
- Operates from a single 3.3-V Supply
- Low-Voltage Differential Signaling (LVDS) with Output Voltages of ±350mV into a 100-ohm load
- Choice between LVDS or TTL clock input
- Synchronous Enable/Disable
- Multiplexed clock input
  – Internal 300 kohm pullup resistor on all control pins
  – CLK and $\overline{CLK}$ have 110-ohm termination (PI90LVT211)
- Common and individual Enable/Disable control
- 50ps Output-to-Output Skew
- ±24ps Period Jitter
- Bus Pins are High Impedance when disabled or with V_{CC} <1.5V
- TTL Inputs are 5V Tolerant
- Power Dissipation at 300 MHz
- P190LV211 is functionally compatible with Motorola's (PECL) MC10E211/MC100E211
- >12kV ESD Protection
- Packaging (Pb-free & Green available):
  - 28-pin TSSOP (L)
  - 28-pin QSOP (Q)

Block Diagram & Pin Configuration



Description

The PI90LV211 implements low voltage differential signaling (LVDS) to achieve clocking rates as high as 320 MHz with low skew. The PI90LV211 is a low skew 1:6 fanout device designed explicitly for low skew clock distribution applications. The device features a multiplexed clock input to allow for the distribution of a lower speed scan or test clock with the high-speed system clock. When LOW the SEL pin will select the differential clock input.

Both a common enable and individual output enables are provided. When asserted the positive output will go LOW on the next negative transition of the CLK (or SCLK) input. The enable function is synchronous so that the outputs will only be enabled/disabled when they are already in the LOW state. This avoids any chance of generating a runt clock pulse when the device is enabled/disabled as can happen with an asynchronous control. The internal flip flop is clocked on the falling edge of the input clock, therefore all associated specification limits are referenced to the negative edge of the clock input.

Individual synchronous enable controls and multiplexed clock inputs make this device ideal as the first level distribution unit in a distribution tree. The individual enables could be used to allow for the disabling of individual cards on a backplane in fault tolerant designs.

Function Table

CLK/$\overline{CLK}$	SCLK	SEL	$\overline{ENx}$	$\overline{CEN}$	CLK OUT (±)
H/L	X	L	L	L	CLK
X	H/L	H	L	L	SCLK
↓	↓	X	H	L	Z*
↓	↓	H	L	H	Z**

* $\overline{ENx}$ disables individual banks
** $\overline{CEN}$ disables all six banks
↓ = Negative transition of CLK or SCLK
Z = High Impedance

Electrical Characteristics over Recommended Operating Conditions (unless otherwise noted).

Symbol	Parameter	Test Conditions	Min.	Typ.(1)	Max.	Units
$\|V_{OD}\|$	Differential output voltage magnitude	R_L = 100Ω See Figures 1 and 2	247	340	454	mV
$\Delta\|V_{OD}\|$	Change in differential output voltage magnitude between logic states		–50		50	
$V_{OC(SS)}$	Steady-state common-mode output voltage	See Figure 3	1.125	1.30	1.60	V
$\Delta V_{OC(SS)}$	Change in steady-state common-mode output voltage between logic states		–50		50	mV
$V_{OC(PP)}$	Peak-to-peak common-mode output voltage			40	150	
I_{CC}	Supply Current	Enabled, R_L = 100Ω V_{IN} = V_{CC} or GND		27	35	mA
		Disabled, V_{IN} = V_{CC} or GND		3.0	3.9	
I_{IH}	High-level input current	V_{IH} = 2V		4.8	20	µA
I_{IL}	Low-level input current	V_{IL} = 0.8V		9	20	
I_{OS}	Short-circuit output current	V_{ODOUT+} or V_{ODOUT-} = 0V			±7	mA
		V_{OD} = 0V			±4.5	
I_{OZ}	High-impedance output current	V_O = 0V or V_{CC}			±1	µA
$I_{O(OFF)}$	Power-off output current	V_{CC} = 1.1V, V_O = 2.4V			±1	
C_{IN}	Input capacitance,	V_I = 0.4 sin (4E6πt) +0.5V		9		pF
C_O	Output capacitance	V_I = 0.4 sin (4E6πt) +0.5V, Disabled		10		
R_{TERM}	Termination Resistor	PI90LVT211	90	110	132	Ω

Switching Characteristics over Recommended Operating Conditions (unless otherwise noted)[8,9].

Characteristic	Symbol	Min.	Typ.	Max.	Units	Condition
Propagation Delay to Output CLK to CLKOUT ± SCLK to CLKOUT ± SEL to CLKOUT ±	 t_{PLH} t_{PHL}	 1.5 1.5 1.5	 2.7 2.7 2.7	 3.4 3.24 3.6	ns	
Disable Time CLK or SCLK to CLKOUT ±	 t_{PHZ} t_{PLZ} t_{PZH} t_{PZL}		 2.2 2.1 3.6 2.8	 2.8 2.8 4.8 4.8		2
Part-to-Part Skew CLK (Diff) to Q CLK (SE), SCLK to Q With Device Skew	t_{skew}			 TBD TBD TBD	ps	1
Cycle-to-Cycle Jitter	$t_{jit(cc)}$	–48		+48		Figure 6
Period Jitter	$t_{jit(per)}$	–24		+24		Figure 7
Setup Time $\overline{EN}$x to CLK $\overline{CEN}$ to CLK	t_s	 200 200	 –100 0			2
Hold Time CLK to $\overline{EN}$x, $\overline{CEN}$	t_h		600	760		2
Minimum Input Swing (CLK)	V_{PP}	0.20		0.800	V	3
Com. Mode Range (CLK)	V_{CMR}	0.125	1.5	V_{CC} - 0.2		4
Rise/Fall Times 20 – 80%	t_r, t_f	150	400	1200		
Duty Cycle Distortion Pulse Skew (t_{PLH} - t_{PHL}) SCLK to CLKOUT± CLK to CLKOUT±	 t_{SK1R} t_{SK1R}		 140 25	 180 60	ps	5
Channel-to-Channel Skew, same edge	t_{SK2R}		30	100		6
Maximum Operating Frequency			250		MHz	7

Notes:

1. Within-Device skew is defined for identical transitions on similar paths through a device.
2. Setup, Hold, and Disable times are all relative to a falling edge on CLK or SCLK.
3. Minimum input swing for which AC parameters are guaranteed. Full DC LVDS output swings will be generated with only 50mV input swings.
4. The range in which the high level of the input swing must fall while meeting the V_{PP} spec.
5. t_{SK1R} is the difference in receiver propagation delay (t_{PLH}-t_{PHL}) of one device, and is the duty cycle distortion of the output at any given temperature and V_{CC}. The propagation delay specification is a device-to-device worst case over process, voltage, and temperature.
6. t_{SK2R} is the difference in receiver propagation delay between channels in the same device of any outputs switching in the same direction. This parameter is guaranteed by design and characterization.
7. Generator input conditions: $t_r t_f$ < 1ns, 50% duty cycle, differential (1.10V to 1.35V peak-peak).
   Output Criteria: 60%/40% duty cycle, V_{OL} (max) 0-4V, V_{OH} (min) 2.7V, Load - 7pF (stray plus probes).
8. C_L includes probe and fixture capacitance.
9. Generator waveform for all tests unless otherwise specified: f = 25 MHz, Z_O = 50 ohms, t_r = 1ns, t_f = 1ns (35%-65%). To ensure fastest propagation delay and minimum skew, clock input edge rates should not be slower than 1ns/V; control signals not slower than 3ns/V.

Parameter Measurement Information

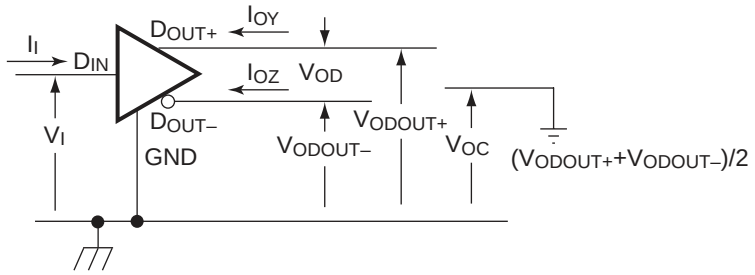


Figure 1. Voltage and Current Definitions

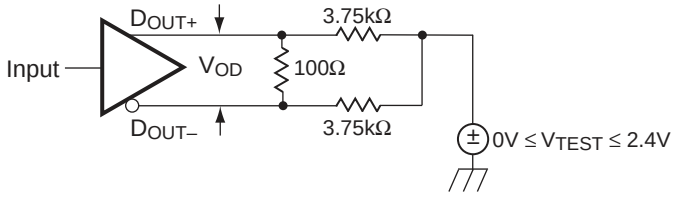


Figure 2. V_{OD} Test Circuit

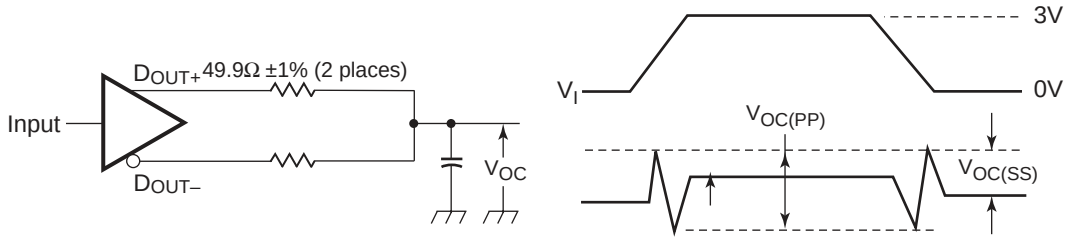


Figure 3. Test Circuit & Definitions for the Driver Common-Mode Output Voltage

Note:

1. All input pulses are supplied by a generator having the following characteristics: t_r or $t_f \le 1$ns, Pulse Repetition Rate (PRR) = 50 Mpps, Pulse width = 10 ±0.2ns. C_L includes instrumentation and fixture capacitance within 0.06m of the D.U.T. Themeasurement of VOC(PP) is made on test equipment with a –3dB bandwidth of at least 300MHz.

Parameter Measurement Information (continued)

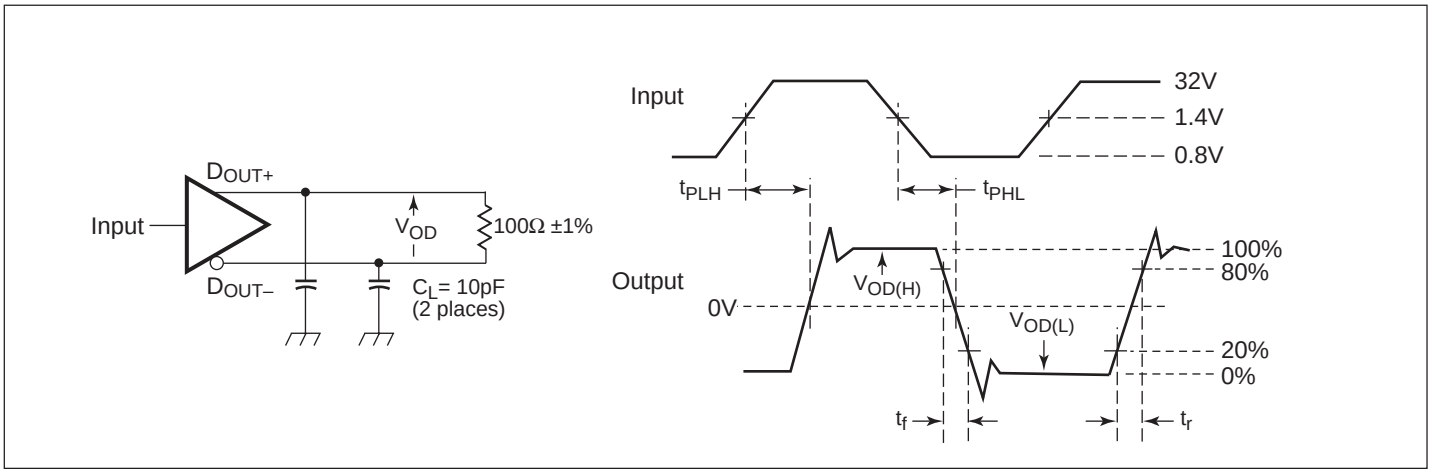


Figure 4. Test Circuit, Timing, & Voltage Definitions for the Differential Output Signal

Note:

1. All input pulses are supplied by a generator having the following characteristics: t_r or $t_f \leq 1$ns, Pulse Repetition Rate (PRR) = 15 Mpps, Pulse width = 10 ±0.2ns. C_L includes instrumentation and fixture capacitance within 0.06m of the D.U.T.

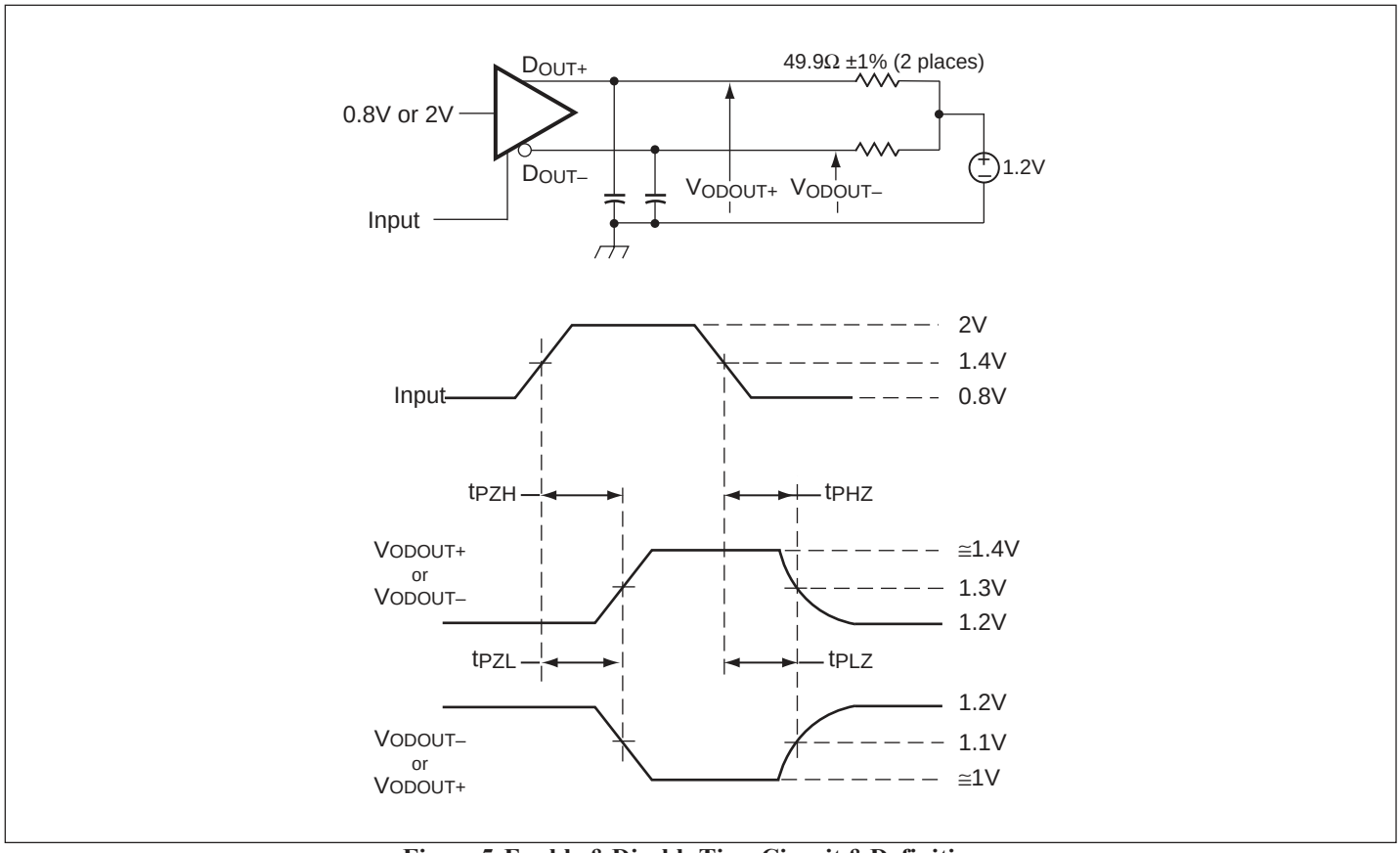


Figure 5. Enable & Disable Time Circuit & Definitions

Note:

1. All input pulses are supplied by a generator having the following characteristics: t_r or $t_f \leq 1$ns, Pulse Repetition Rate (PRR) = 0.5 Mpps, Pulse width = 500 ±10ns. C_L includes instrumentation and fixture capacitance within 0.06m of the D.U.T.

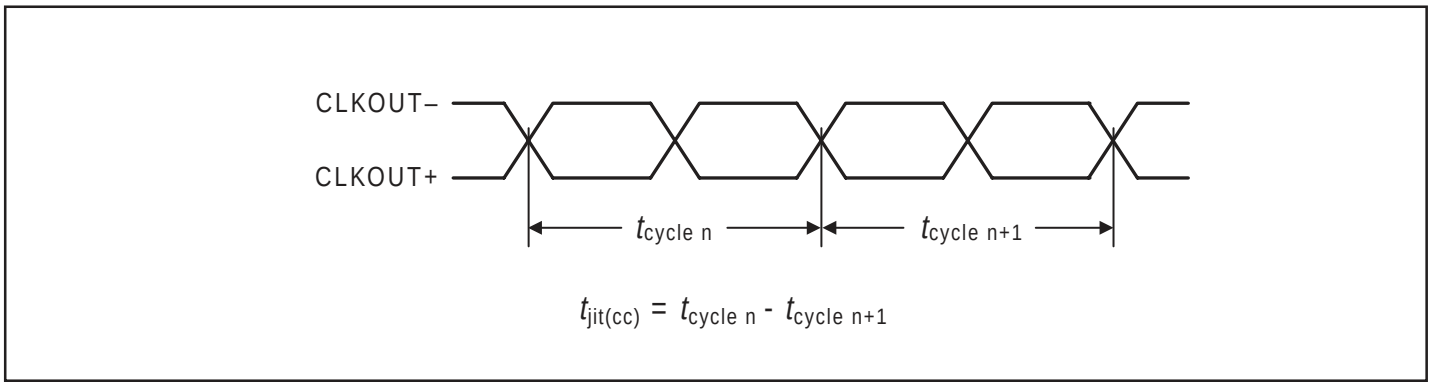


Figure 6. Cycle-to-Cycle Jitter

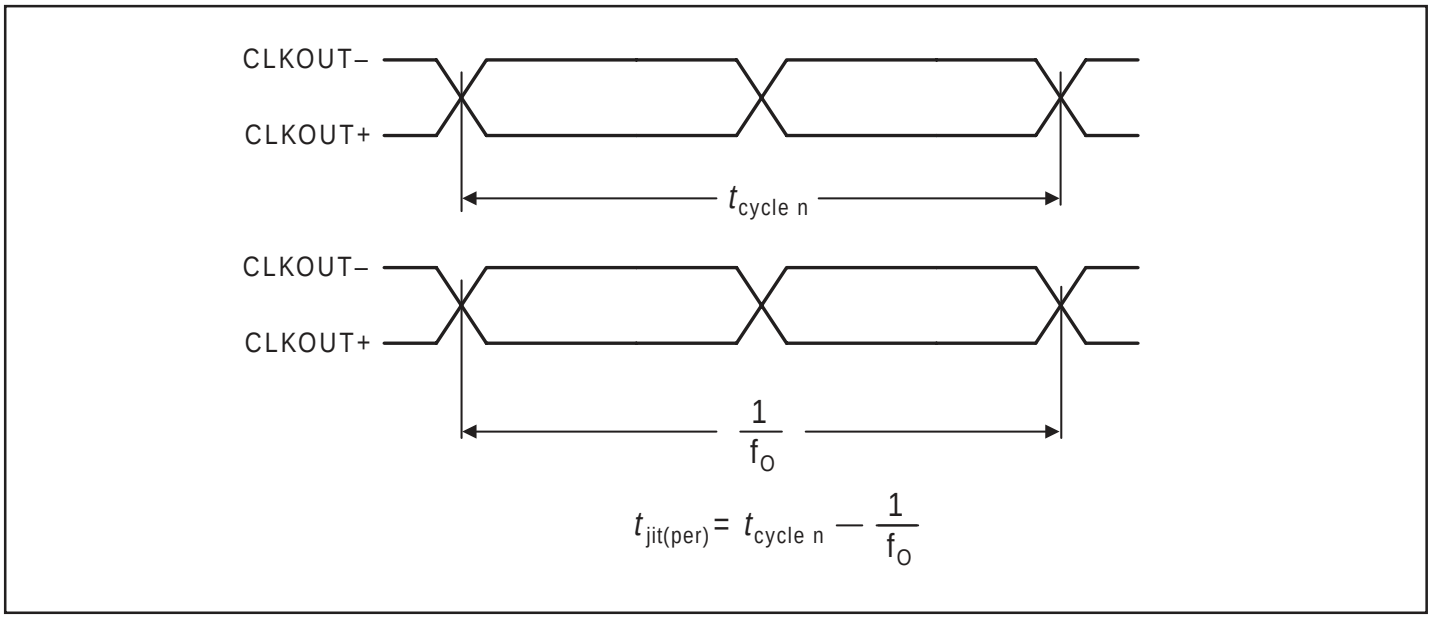


Figure 7. Period Jitter

General Desciption

The PI90LV211 is a 1:6 fanout tree designed explicitly for low-skew, high-speed clock distribution. The device was targeted to work in conjunction with the PI90LV14 device to provide another level of flexibility in the design and implementation of clock distribution trees. The individual synchronous enable controls and multiplexed clock inputs make the device ideal as the first level distribution unit in a distribution tree. The device provides the ability to distribute a lower speed scan or test clock along with the high-speed system clock to ease the design of system diagnostics and self test procedures. The individual enables could be used to allow for the disabling of individual cards on a backplane in fault tolerant designs.

Handling Open Inputs and Outputs

With the simultaneous switching characteristics and the tight skew specifications of the P90LV211, the handling of the unused outputs becomes critical. To minimize the noise generated on the die all outputs should be terminated in pairs, i.e. both the true and compliment outputs should be terminated even if only one of the outputs will be used in the system. With both complimentary pairs terminated, the current in the V_{CC} pins will remain essentially constant and thus inductance induced voltage glitches on V_{CC} will not occur. V_{CC} glitches will result in distorted output waveforms and degradations in the skew performance of the device.

The package parasitics of the 28-lead package cause the signals on a given pin to be influenced by signals on adjacent pins. PI90LV211 is characterized and tested with all of the outputs switching, therefore the numbers in the data book are guaranteed only for this situation. If all of the outputs of the PI90LV211 are not needed and there is a desire to save power, the unused output pairs can be left unterminated. Unterminated outputs can influence the propagation delay on adjacent pins by 15ps–20ps. Therefore, under these conditions, this 15ps–20ps needs to be added to the overall skew of the device. Pins which are separated by a package corner are not considered adjacent pins in the context of propagation delay influence. Therefore if all of the outputs on a single side of the package are terminated, the specification limits in the data sheet will apply.

Using the Enable Pins

Both the common enable ($\overline{CEN}$) and the individual enables ($\overline{EN}x$) are synchronous to the CLK or SCLK input depending on which is selected. The active low signals are clocked into the enable flip flops on the negative edges of the PI90LV211 clock inputs. In this way, the devices will only be disabled when the outputs are already in the LOW state. The internal propagation delays are such that the delay to the output through the distribution buffers is less than that through the enable flip flops. This will ensure that the disabling of the device will not slice any time off the clock pulse. On initial power up, the enable flip flops will randomly attain a stable state; therefore precautions should be taken on initial power up to ensure the PI90LV211 is in the desired state.

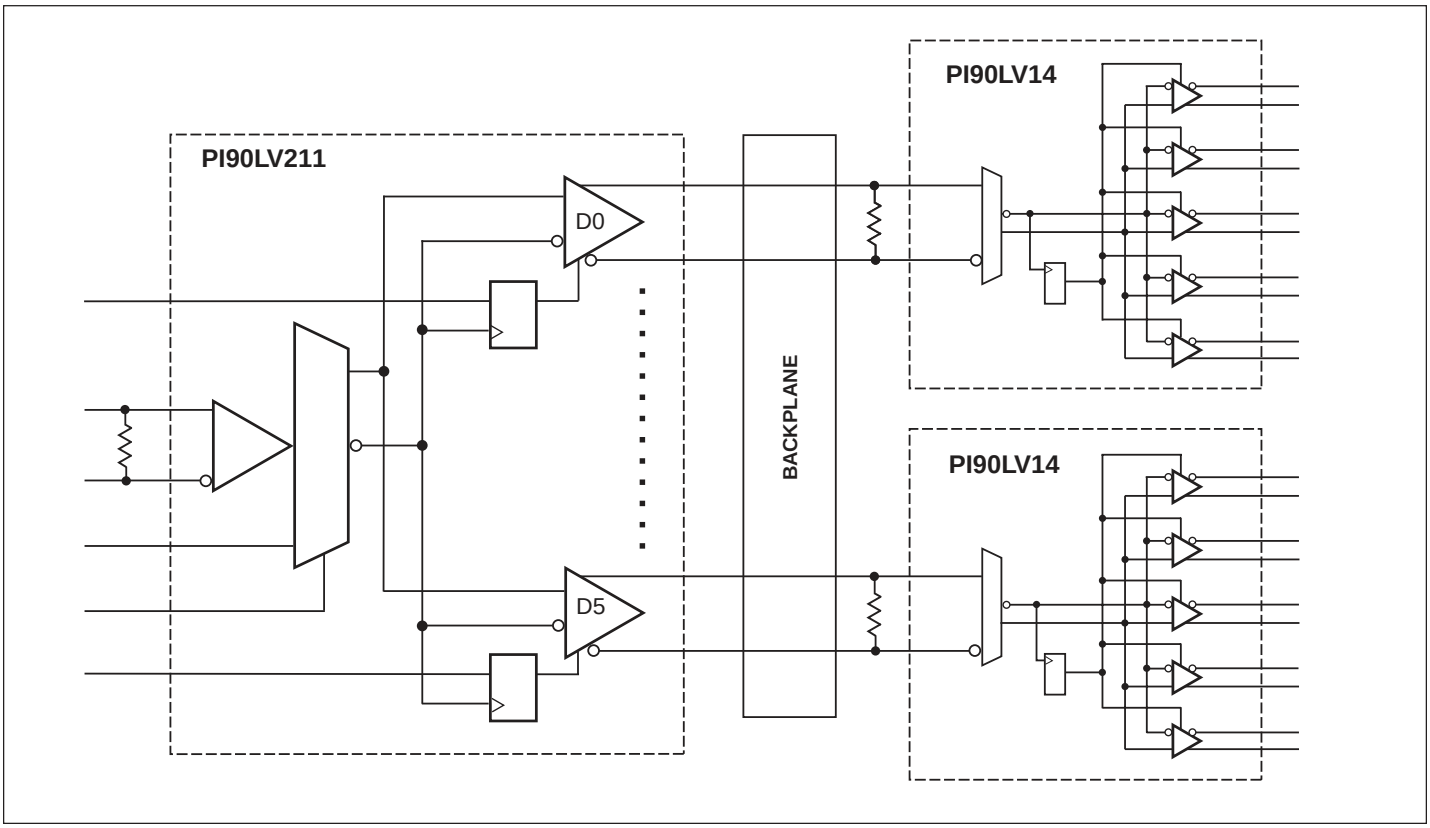
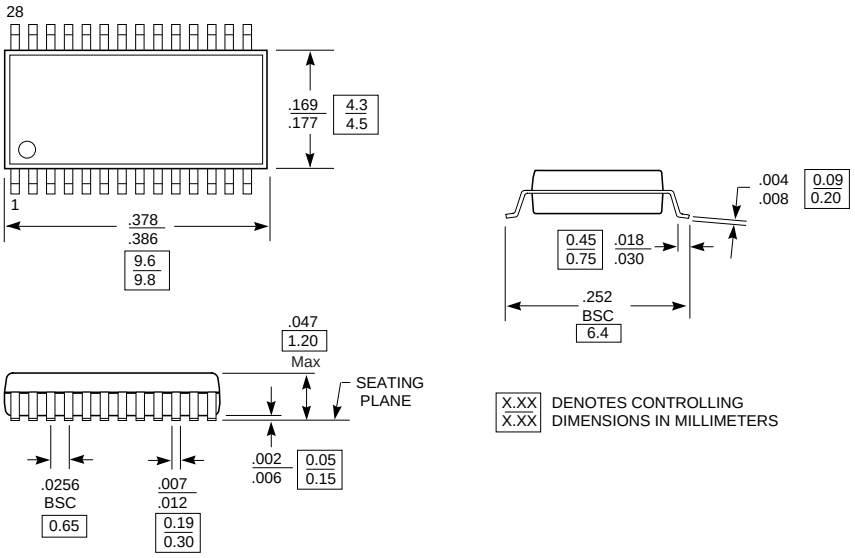
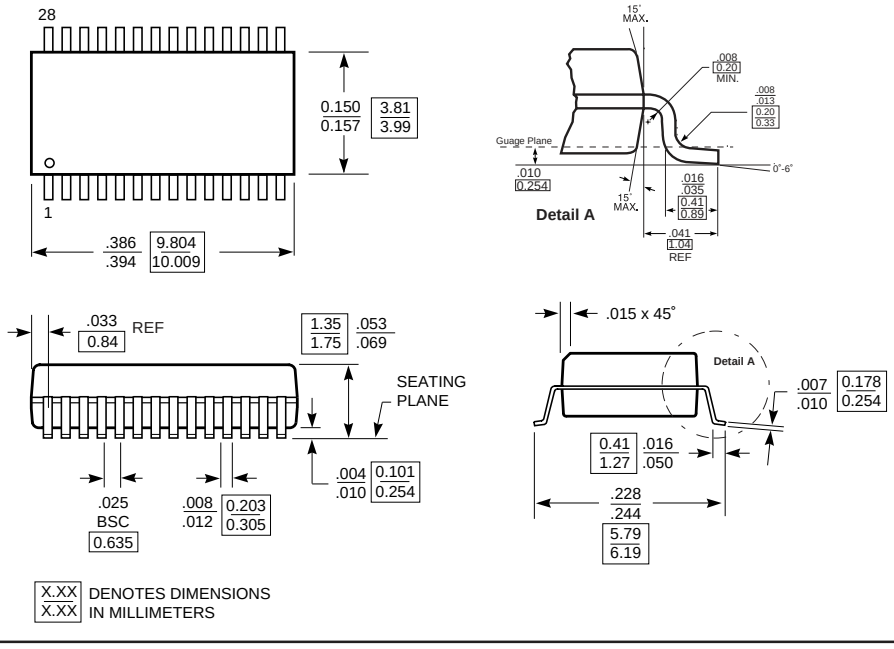


Figure 8. Standard PI90LV211 LVDS Application

Packaging Mechanical: 28-Pin TSSOP (L)



Packaging Mechanical: 28-Pin QSOP (Q)



Ordering Information

Ordering Code	Package Code	Package Type
PI90LV211L	L	28-pin 173-mil TSSOP
PI90LV211LE	L	Pb-free & Green, 28-pin 173-mil TSSOP
PI90LV211Q	Q	28-pin 150-mil QSOP
PI90LV211QE	Q	Pb-free & Green, 28-pin 150-mil QSOP
PI90LVT211L	L	28-pin 173-mil TSSOP
PI90LVT211LE	L	Pb-free & Green, 28-pin 173-mil TSSOP
PI90LVT211Q	Q	28-pin 150-mil QSOP
PI90LVT211QE	Q	Pb-free & Green, 28-pin 150-mil QSOP

Notes:
1. Thermal characteristics can be found on the company web site at www.pericom.com/packaging/