20 GHz to 54 GHz, GaAs, pHEMT, MMIC, 29 dBm (0.5 W) Power Amplifier

FEATURES

- Integrated power-supply capacitors and bias inductors
- Integrated AC coupling capacitors
- Gain: 17.5 dB typical at 20 GHz to 35 GHz
- Input return loss: 14 dB typical at 20 GHz to 35 GHz
- Output return loss: 15 dB typical at 20 GHz to 35 GHz
- OP1dB: 28 dBm typical at 20 GHz to 35 GHz
- P_{SAT}: 28.5 dBm typical at 20 GHz to 35 GHz
- OIP3: 34.5 dBm typical at 20 GHz to 35 GHz
- Noise figure: 7.5 dB typical at 20 GHz to 35 GHz
- 5 V supply voltage at 850 mA
- 50 Ω matched input and output
- 5.00 mm × 5.00 mm, 24-terminal chip array, small outline, no lead cavity [LGA_CAV] package

APPLICATIONS

- Military and space
- Test instrumentation

GENERAL DESCRIPTION

The ADPA7009-2 is a gallium arsenide (GaAs), pseudomorphic high-electron-mobility transistor (pHEMT), monolithic microwave integrated circuit (MMIC), 0.5 W power amplifier with an integrated temperature-compensated, on-chip power detector that operates between 20 GHz and 54 GHz. The amplifier provides a gain of 17.5 dB, an output power for 1 dB compression (OP1dB) of 28 dBm, and a typical output third-order intercept (OIP3) of 34.5 dBm at 20 GHz to 35 GHz. The ADPA7009-2 requires 850 mA from a 5 V supply voltage (VDDx). The RF input and outputs are internally matched and DC-blocked for ease of integration into higher level assemblies. Most of the typically required external passive components for operation (AC coupling capacitors and power supply decoupling capacitors) are integrated, which facilitates a small, compact printed circuit board (PCB) footprint. The ADPA7009-2 is available in a 5.00 mm × 5.00 mm, 24-terminal chip array, small outline, no lead cavity [LGA_CAV] package.

FUNCTIONAL BLOCK DIAGRAM

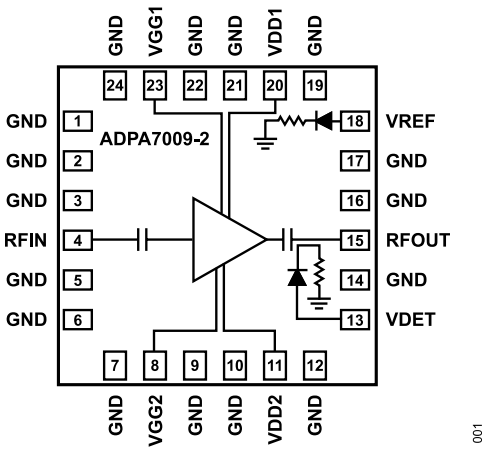

Figure 1. Functional Block Diagram

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REVISION HISTORY

8/2022—Revision 0: Initial Version

SPECIFICATIONS

20 GHz TO 35 GHz FREQUENCY RANGE

T_{CASE} = 25°C, supply voltage (V_{DD}) = 5 V, quiescent drain current (I_{DQ}) = 850 mA, and 50 Ω matched input and output, unless otherwise noted. Adjust the gate voltage (V_{GG}) from −1.5 V to 0 V to achieve I_{DQ} = 850 mA typical.

Table 1. 20 GHz to 35 GHz Frequency Range

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
FREQUENCY RANGE		20		35	GHz	
GAIN		15	17.5		dB	
Gain Flatness			±1.3		dB	
Gain Variation over Temperature			0.028		dB/°C	
NOISE FIGURE			7.5		dB	
RETURN LOSS						
Input			14		dB	
Output			15		dB	
OUTPUT						
Output Power for 1 dB Compression	OP1dB	25.5	28.0		dBm	
Saturated Output Power	P_{SAT}		28.5		dBm	
Output Third-Order Intercept	OIP3		34.5		dBm	Output power (P_{OUT}) per tone = 14 dBm with 1 MHz tone spacing
SUPPLY						
Quiescent Drain Current	I_{DQ}		850		mA	Adjust V_{GG} to achieve I_{DQ} = 850 mA typical
Voltage	V_{DD}	3	5		V	

35 GHz TO 43 GHz FREQUENCY RANGE

T_{CASE} = 25°C, V_{DD} = 5 V, I_{DQ} = 850 mA, and 50 Ω matched input and output, unless otherwise noted. Adjust V_{GG} from −1.5 V to 0 V to achieve I_{DQ} = 850 mA typical.

Table 2. 35 GHz to 43 GHz Frequency Range

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
FREQUENCY RANGE		35		43	GHz	
GAIN		14.5	17		dB	
Gain Flatness			±1.0		dB	
Gain Variation over Temperature			0.046		dB/°C	
NOISE FIGURE			7		dB	
RETURN LOSS						
Input			15		dB	
Output			13		dB	
OUTPUT						
Output Power for 1 dB Compression	OP1dB	24	26.5		dBm	
Saturated Output Power	P_{SAT}		27.5		dBm	
Output Third-Order Intercept	OIP3		34.5		dBm	P_{OUT} per tone = 14 dBm with 1 MHz tone spacing
SUPPLY						
Quiescent Drain Current	I_{DQ}		850		mA	Adjust V_{GG} to achieve I_{DQ} = 850 mA typical
Voltage	V_{DD}	3	5		V	

SPECIFICATIONS

43 GHz TO 54 GHz FREQUENCY RANGE

T_{CASE} = 25°C, V_{DD} = 5 V, I_{DQ} = 850 mA, and 50 Ω matched input and output, unless otherwise noted. Adjust V_{GG} from −1.5 V to 0 V to achieve I_{DQ} = 850 mA typical.

Table 3. 43 GHz to 54 GHz Frequency Range

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
FREQUENCY RANGE		43		54	GHz	
GAIN			16.5		dB	
Gain Flatness			±1.3		dB	
Gain Variation over Temperature			0.055		dB/°C	
NOISE FIGURE			7.0		dB	
RETURN LOSS						
Input			13		dB	
Output			12		dB	
OUTPUT						
Output Power for 1 dB Compression	OP1dB		24.0		dBm	
Saturated Output Power	P_{SAT}		25.0		dBm	
Output Third-Order Intercept	OIP3		34.0		dBm	P_{OUT} per tone = 14 dBm with 1 MHz tone spacing
SUPPLY						
Quiescent Drain Current	I_{DQ}		850		mA	Adjust V_{GG} to achieve I_{DQ} = 850 mA typical
Voltage	V_{DD}	3	5		V	

ABSOLUTE MAXIMUM RATINGS

Table 4. Absolute Maximum Ratings

Parameter	Rating
V_{DD}	6.0 V
V_{GG}	−1.6 V to 0 V
RF Input Power (RFIN)	20 dBm
Continuous Power Dissipation (P_{DISS}), T_{CASE} = 85°C (Derate 13.6 mW/°C above 85°C)	6.6 W
Temperature	
Maximum Channel	175°C
Quiescent Channel (T_{CASE} = 85°C, V_{DD} = 5 V) I_{DQ} = 850 mA, P_{IN} = Off	143°C
Storage Range	−65°C to +150°C
Operating Range	−40°C to +85°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to system design and operating environment. Careful attention to PCB thermal design is required.

θ_{JC} is the channel-to-case thermal resistance (channel to exposed metal ground pad on the underside of the device).

Table 5. Thermal Resistance

Package Type	θ_{JC}[1]	Unit
CE-24-2	13.6	°C/W

[1] θ_{JC} was determined by simulation under the following conditions: the heat transfer is due solely to thermal conduction from the channel, through the ground pad, to the PCB, and the ground pad is held constant at the operating temperature of 85°C.

ELECTROSTATIC DISCHARGE (ESD) RATINGS

The following ESD information is provided for handling of ESD-sensitive devices in an ESD-protected area only.

Human Body Model (HBM) per ANSI/ESDA/JEDEC JS-001.

ESD Ratings for ADPA7009-2

Table 6. ADPA7009-2, 24-Terminal LGA_CAV

ESD Model	Withstand Threshold (V)	Class
HBM	±500	1B

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

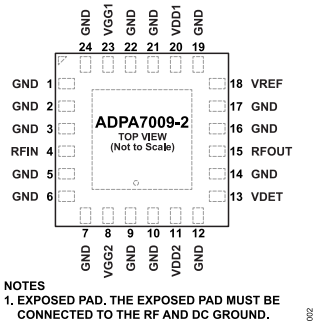

Figure 2. Pin Configuration

Table 7. Pin Function Descriptions

Pin No.	Mnemonic	Description
1, 2, 3, 5, 6, 7, 9, 10, 12, 14, 16, 17, 19, 21, 22, 24	GND	Ground. Connect to a ground plane that has low electrical and thermal impedance. See Figure 3 for the interface schematic.
4	RFIN	RF Signal Input. The RFIN pin is AC-coupled and matched to 50 Ω. See Figure 4 for the interface schematic.
8, 23	VGG1, VGG2	Negative Gate Bias Control. The gate voltage must be applied to VGGx. Adjust the negative voltage on the VGGx pin to set the I_{DQ} to the desired level. See Figure 5 for the interface schematic.
11, 20	VDD1, VDD2	Drain Biases for the Amplifier. See Figure 6 for the interface schematic.
13	VDET	Detector Diode Used for Measuring the RF Output Power. Detection by the VDET pin requires the application of a DC bias voltage through an external series resistor. Used in combination with VREF, the difference detector voltage, $V_{REF} - V_{DET}$, is a temperature-compensated DC voltage proportional to the RF output power. See Figure 7 for the interface schematic.
15	RFOUT	RF Signal Output. The RFOUT pin is AC-coupled and matched to 50 Ω. See Figure 9 for the interface schematic.
18	VREF	Reference Diode Voltage. Use the VREF pin for temperature compensation of the VDET RF output power measurements. Used in combination with VDET, this voltage provides temperature compensation to the VDET RF output power measurements. See Figure 8 for the interface schematic.
	EPAD	Exposed Pad. The exposed pad must be connected to the RF and dc ground.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

INTERFACE SCHEMATICS

Figure 3. GND Interface Schematic

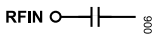

Figure 4. RFIN Interface Schematic

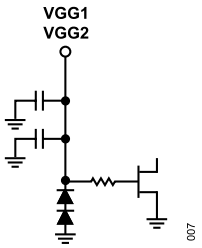

Figure 5. VGG1 and VGG2 Interface Schematic

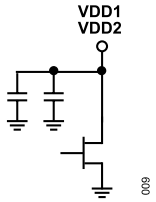

Figure 6. VDD1 and VDD2 Interface Schematic

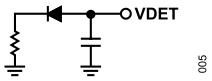

Figure 7. VDET Interface Schematic

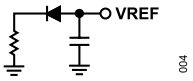

Figure 8. VREF Interface Schematic

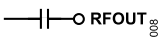

Figure 9. RFOUT Interface Schematic

TYPICAL PERFORMANCE CHARACTERISTICS

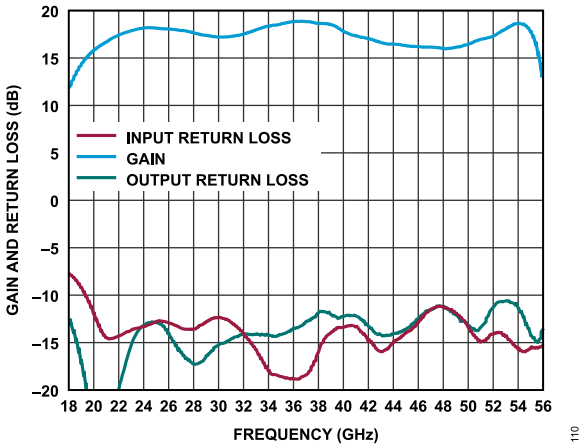

Figure 10. Gain and Return Loss vs. Frequency, V_{DD} = 5 V, I_{DQ} = 850 mA

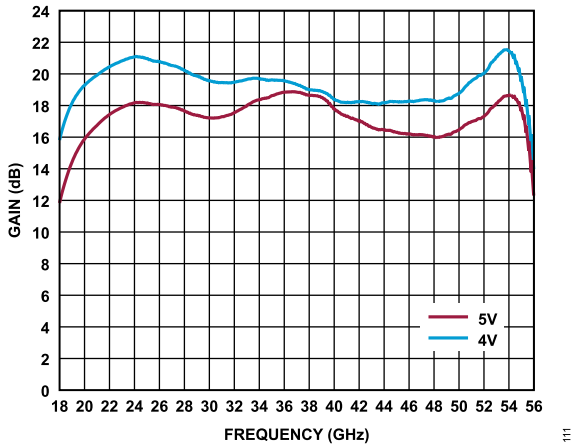

Figure 11. Gain vs. Frequency for Various V_{DD} Values, I_{DQ} = 850 mA

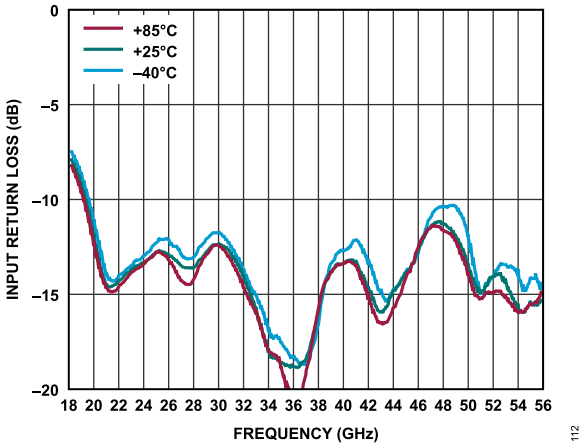

Figure 12. Input Return Loss vs. Frequency for Various Temperatures, V_{DD} = 5 V, I_{DQ} = 850 mA

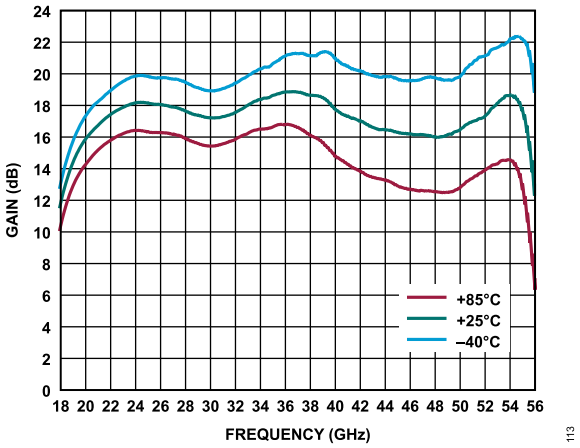

Figure 13. Gain vs. Frequency for Various Temperatures, V_{DD} = 5 V, I_{DQ} = 850 mA

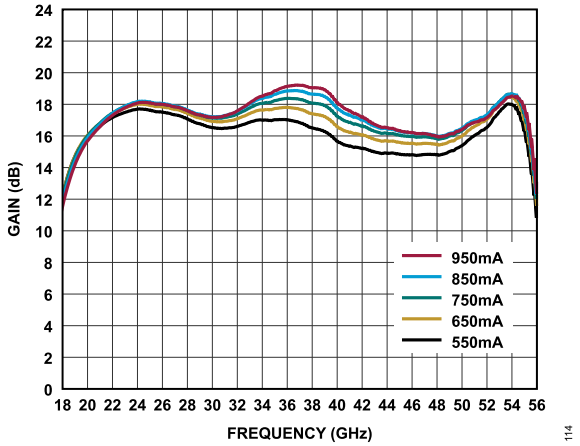

Figure 14. Gain vs. Frequency for Various I_{DQ} Values, V_{DD} = 5 V

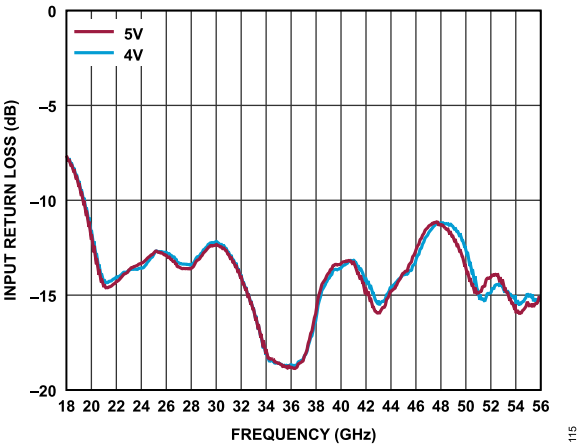

Figure 15. Input Return Loss vs. Frequency for Various V_{DD} Values, I_{DQ} = 850 mA

TYPICAL PERFORMANCE CHARACTERISTICS

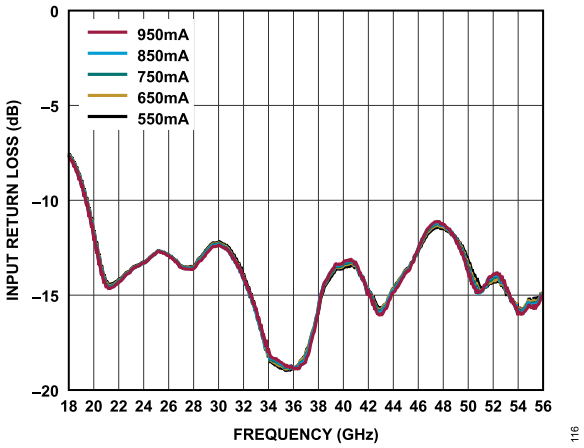

Figure 16. Input Return Loss vs. Frequency for Various I_{DQ} Values, V_{DD} = 5 V

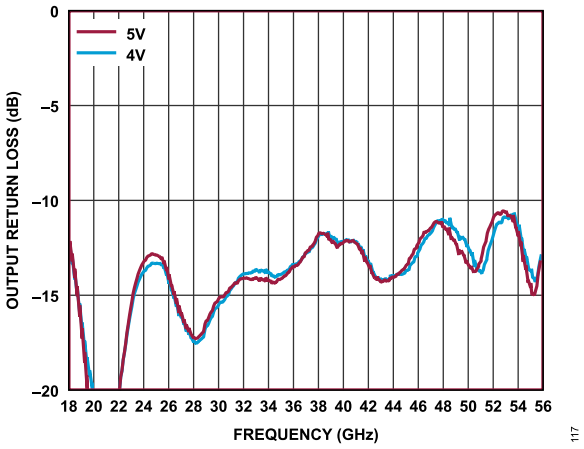

Figure 17. Output Return Loss vs. Frequency for Various V_{DD} Values, I_{DQ} = 850 mA

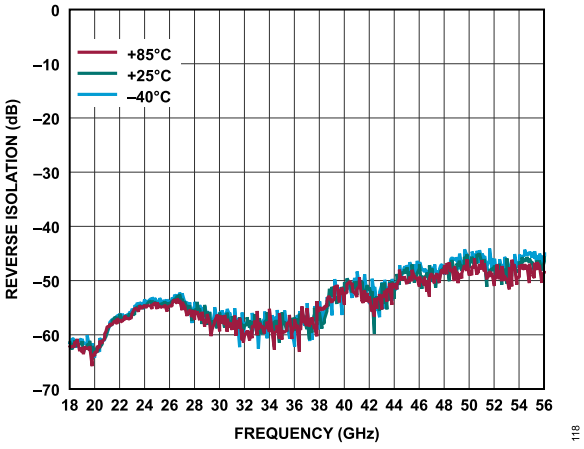

Figure 18. Reverse Isolation vs. Frequency for Various Temperatures, V_{DD} = 5 V, I_{DQ} = 850 mA

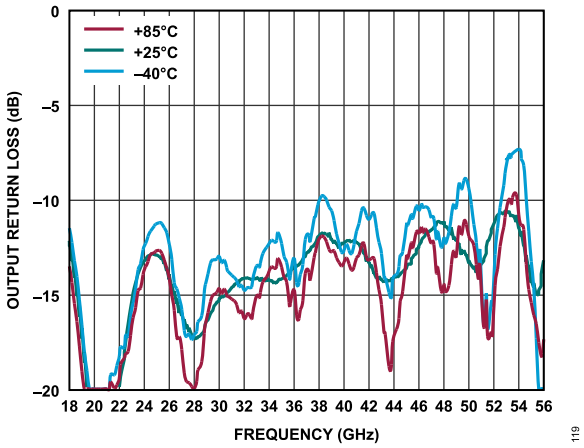

Figure 19. Output Return Loss vs. Frequency for Various Temperatures, V_{DD} = 5 V, I_{DQ} = 850 mA

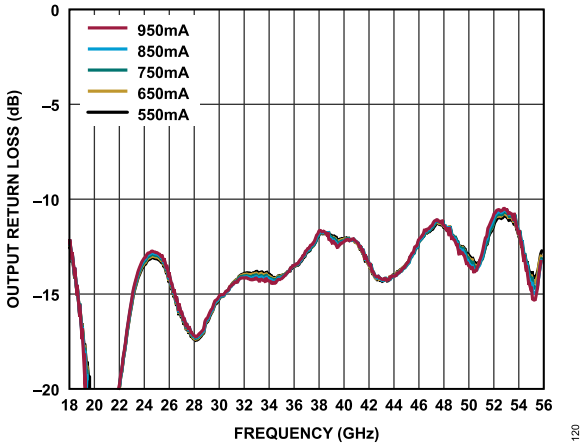

Figure 20. Output Return Loss vs. Frequency for Various I_{DQ} Values, V_{DD} = 5 V

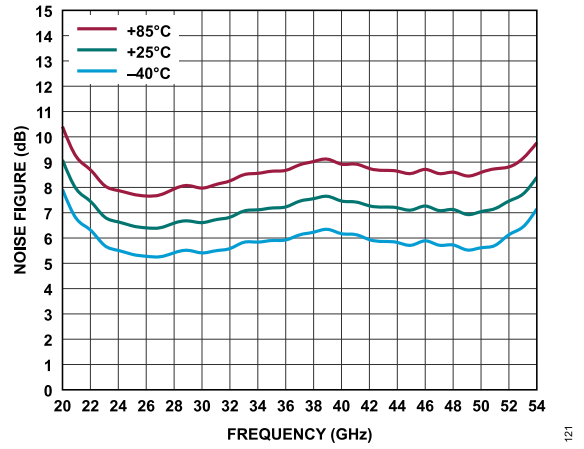

Figure 21. Noise Figure vs. Frequency for Various Temperatures, V_{DD} = 5 V, I_{DQ} = 850 mA

TYPICAL PERFORMANCE CHARACTERISTICS

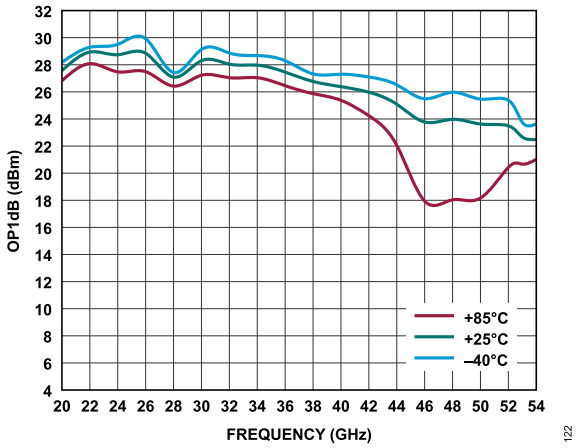

Figure 22. OP1dB vs. Frequency for Various Temperatures, V_{DD} = 5 V, I_{DQ} = 850 mA

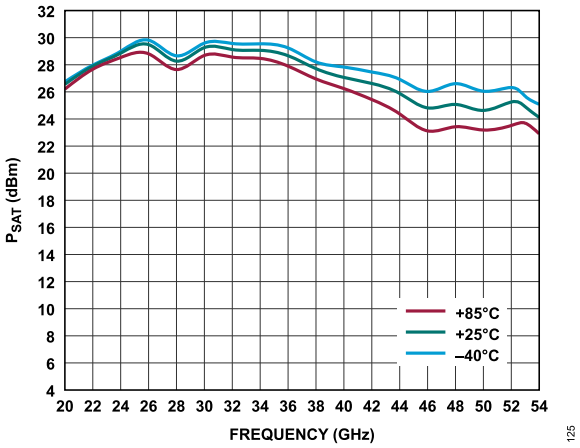

Figure 25. P_{SAT} vs. Frequency for Various Temperatures, V_{DD} = 5 V, I_{DQ} = 850 mA

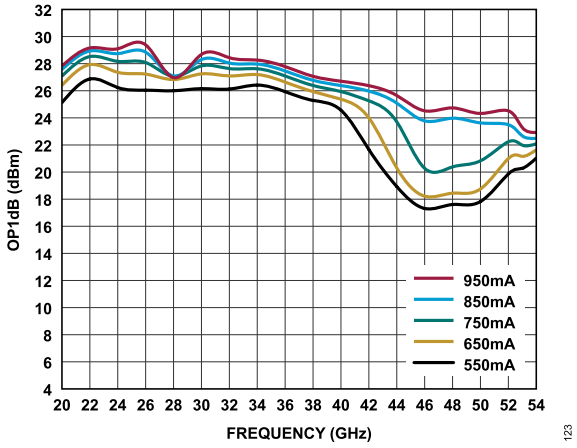

Figure 23. OP1dB vs. Frequency for Various I_{DQ} Values, V_{DD} = 5 V

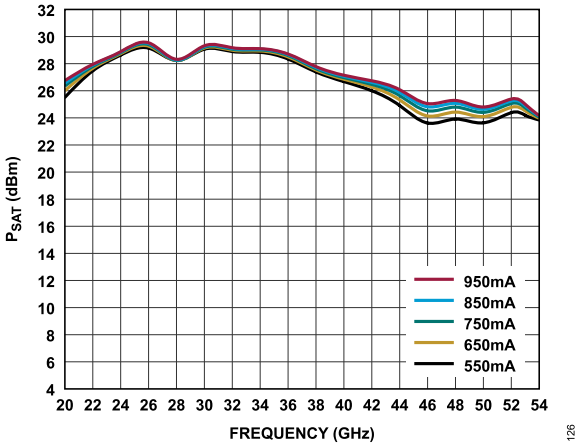

Figure 26. P_{SAT} vs. Frequency for Various I_{DQ} Values, V_{DD} = 5 V

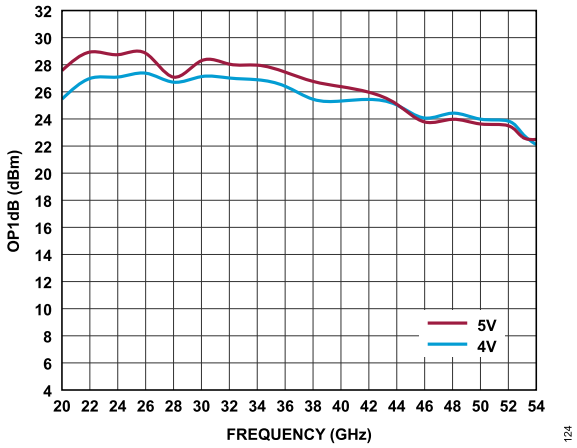

Figure 24. OP1dB vs. Frequency for Various V_{DD} Values, I_{DQ} = 850 mA

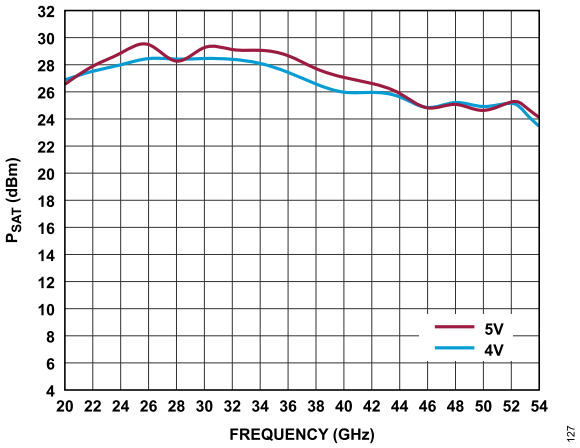

Figure 27. P_{SAT} vs. Frequency for Various, V_{DD} Values, I_{DQ} = 850 mA

TYPICAL PERFORMANCE CHARACTERISTICS

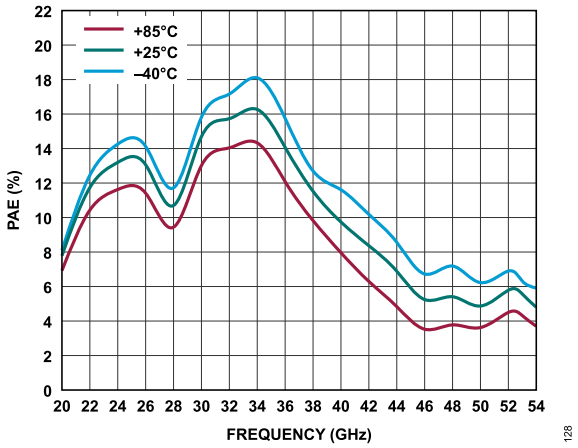

Figure 28. Power-Added Efficiency (PAE) vs. Frequency for Various Temperatures, V_{DD} = 5 V, I_{DQ} = 850 mA, PAE at P_{SAT}

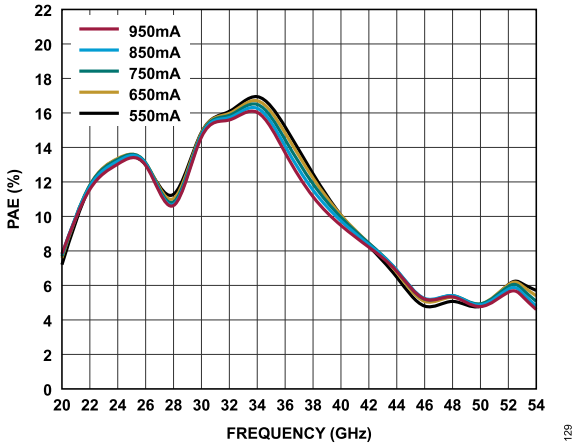

Figure 29. PAE vs. Frequency for Various I_{DQ} Values, V_{DD} = 5 V, PAE at P_{SAT}

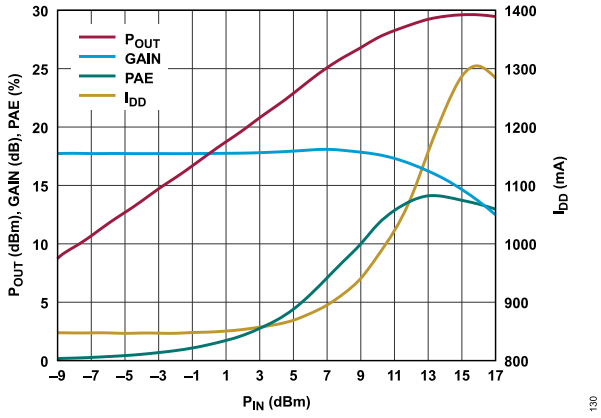

Figure 30. P_{OUT}, Gain, PAE, and Drain Current with RF Applied (I_{DD}) vs. P_{IN}, 26 GHz, V_{DD} = 5 V, I_{DQ} = 850 mA

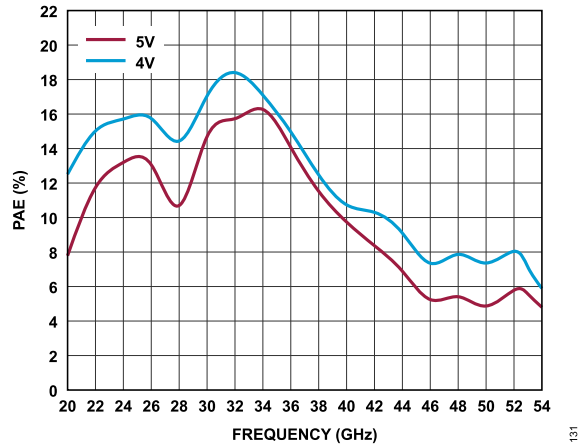

Figure 31. PAE vs. Frequency for Various V_{DD} Values, I_{DQ} = 850 mA, PAE at P_{SAT}

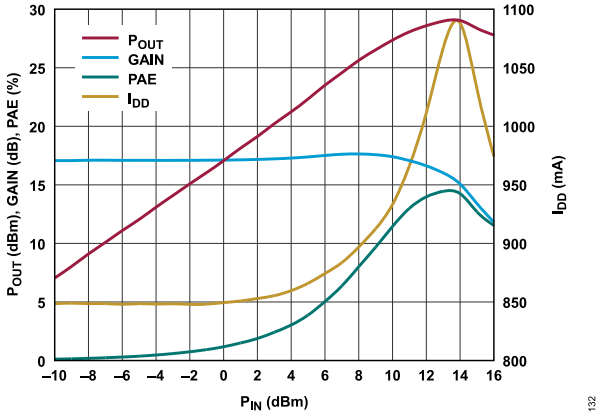

Figure 32. P_{OUT}, Gain, PAE, and I_{DD} vs. P_{IN}, 22 GHz, V_{DD} = 5 V, I_{DQ} = 850 mA

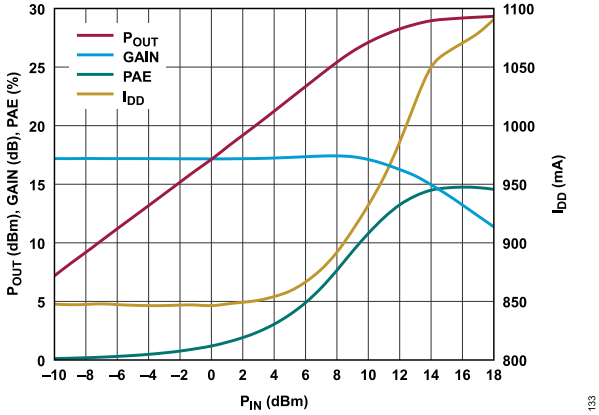

Figure 33. P_{OUT}, Gain, PAE, and I_{DD} vs. P_{IN}, 30 GHz, V_{DD} = 5 V, I_{DQ} = 850 mA

TYPICAL PERFORMANCE CHARACTERISTICS

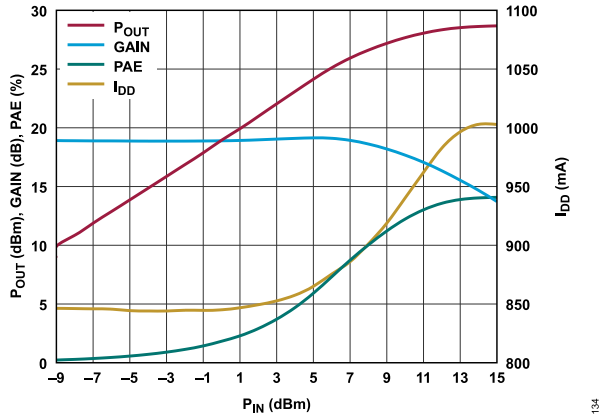

Figure 34. P_{OUT}, Gain, PAE, and I_{DD} vs. P_{IN}, 36 GHz, V_{DD} = 5 V, I_{DQ} = 850 mA

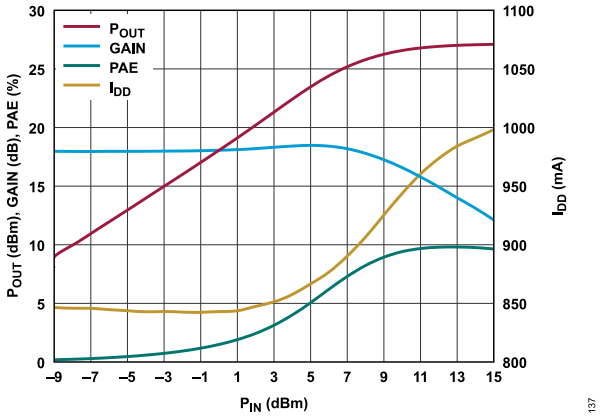

Figure 37. P_{OUT}, Gain, PAE, and I_{DD} vs. P_{IN}, 40 GHz, V_{DD} = 5 V, I_{DQ} = 850 mA

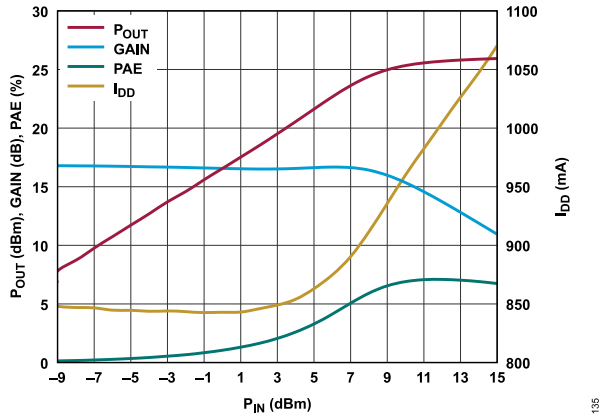

Figure 35. P_{OUT}, Gain, PAE, and I_{DD} vs. P_{IN}, 44 GHz, V_{DD} = 5 V, I_{DQ} = 850 mA

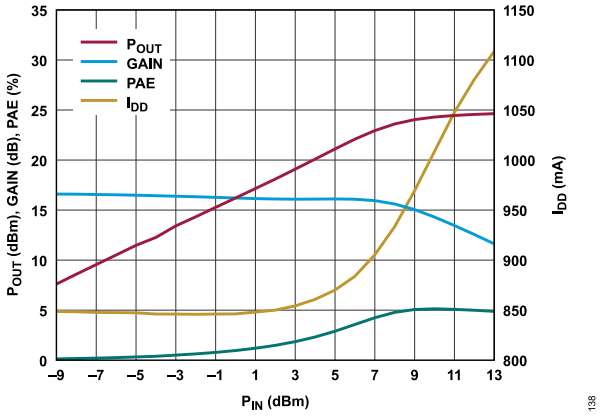

Figure 38. P_{OUT}, Gain, PAE, and I_{DD} vs. P_{IN}, 50 GHz, V_{DD} = 5 V, I_{DQ} = 850 mA

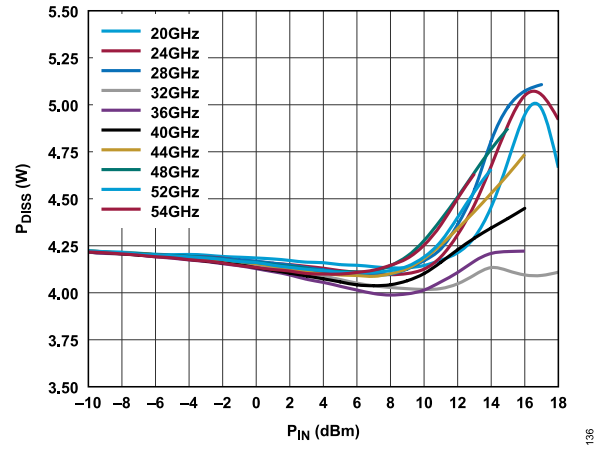

Figure 36. P_{DISS} vs. P_{IN} for Various Frequencies, T_{CASE} = 85°C, V_{DD} = 5 V, I_{DQ} = 850 mA

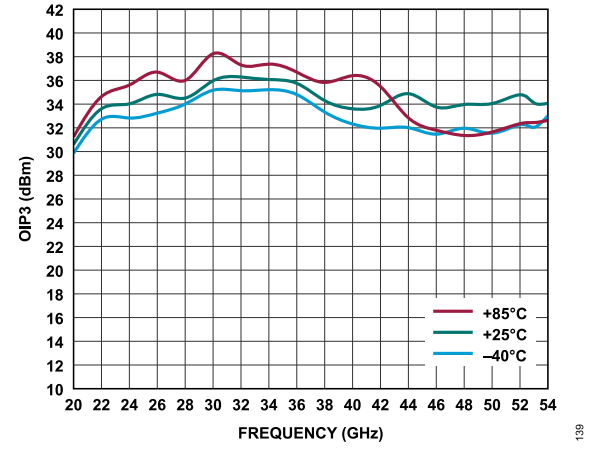

Figure 39. OIP3 vs. Frequency for Various Temperatures, P_{OUT} per Tone = 14 dBm, V_{DD} = 5 V, I_{DQ} = 850 mA

TYPICAL PERFORMANCE CHARACTERISTICS

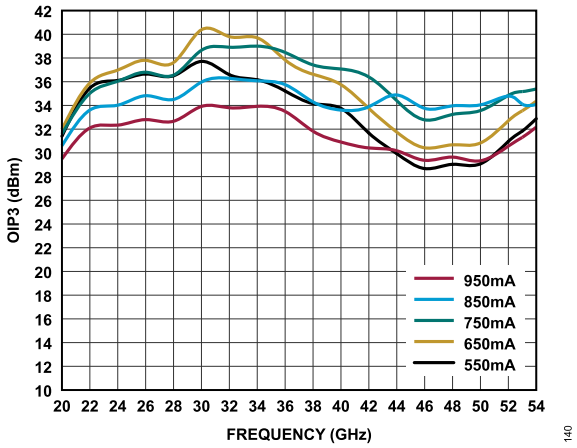

Figure 40. OIP3 vs. Frequency for Various I_{DQ} Values, P_{OUT} per Tone = 14 dBm, V_{DD} = 5 V

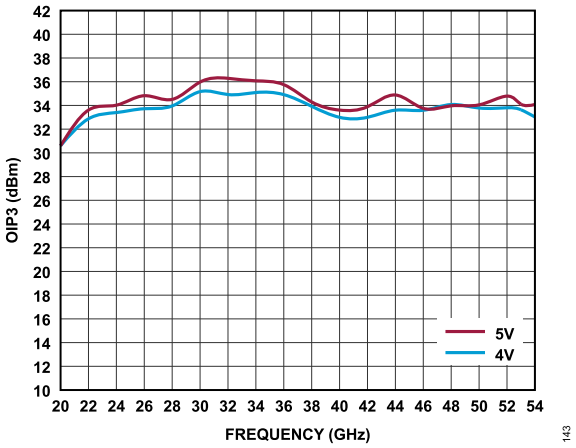

Figure 43. OIP3 vs. Frequency for Various V_{DD} Values, P_{OUT} per Tone = 14 dBm, I_{DQ} = 850 mA

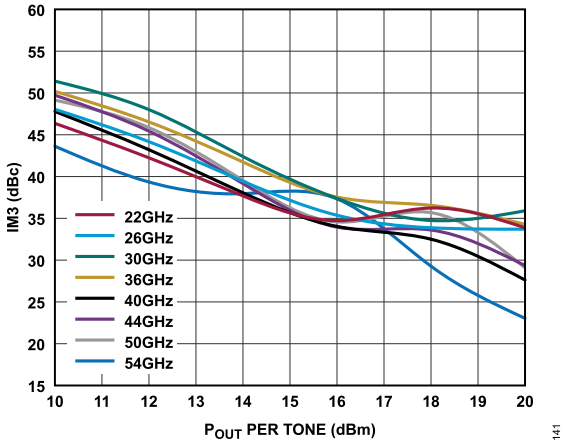

Figure 41. Third-Order Intermodulation Distortion (IM3) vs. P_{OUT} per Tone for Various Frequencies, V_{DD} = 4 V, I_{DQ} = 850 mA

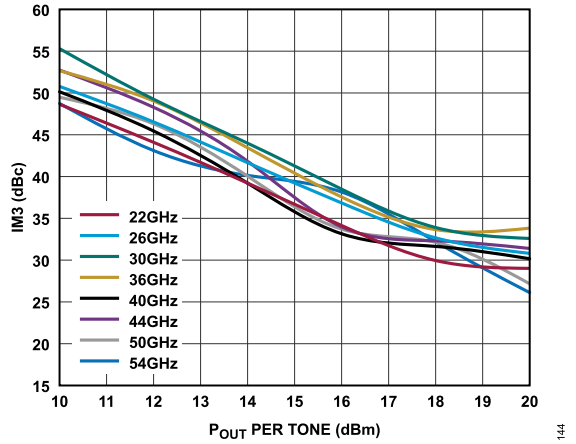

Figure 44. IM3 vs. P_{OUT} per Tone for Various Frequencies, V_{DD} = 5 V, I_{DQ} = 850 mA

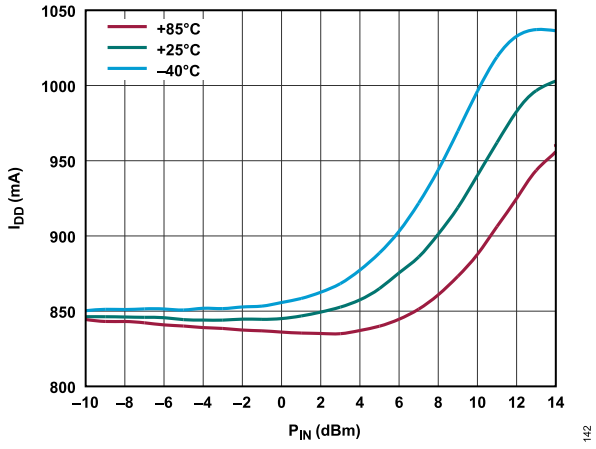

Figure 42. I_{DD} vs. P_{IN} for Various Temperatures, 36 GHz, V_{DD} = 5 V, I_{DQ} = 850 mA

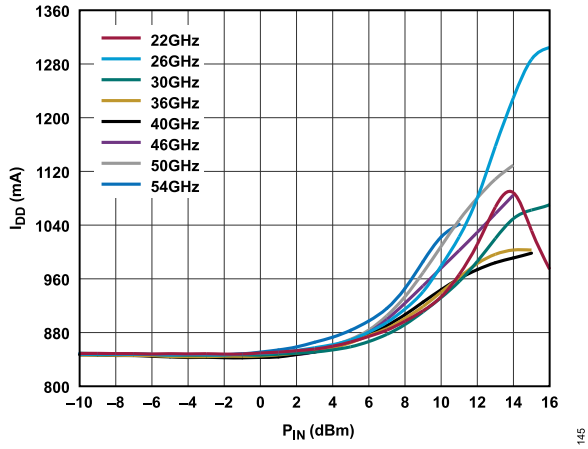

Figure 45. I_{DD} vs. P_{IN} for Various Frequencies, V_{DD} = 5 V, I_{DQ} = 850 mA

TYPICAL PERFORMANCE CHARACTERISTICS

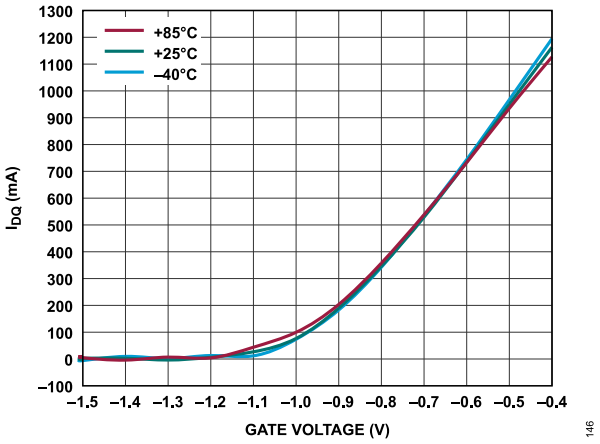

Figure 46. I_{DQ} vs. Gate Voltage for Various Temperatures, V_{DD} = 5 V

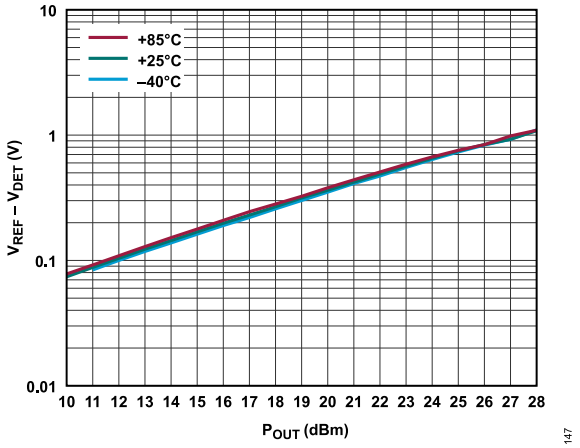

Figure 47. Detector Voltage ($V_{REF} – V_{DET}$) vs. P_{OUT} for Various Temperatures, 36 GHz, V_{DD} = 5 V, I_{DQ} = 850 mA

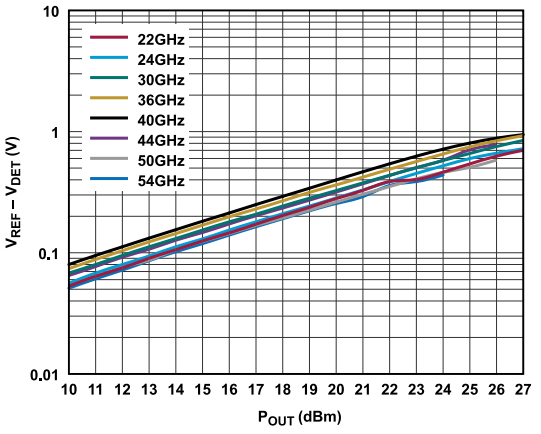

Figure 48. $V_{REF} – V_{DET}$ vs. P_{OUT} for Various Frequencies, V_{DD} = 5 V, I_{DQ} = 850 mA

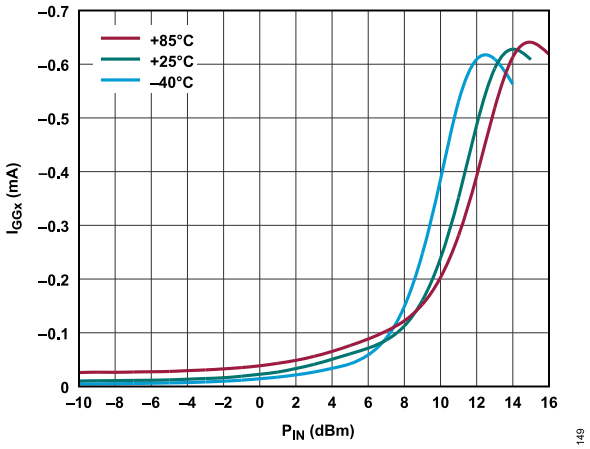

Figure 49. VGG_X Current (I_{GGX}) vs. P_{IN} for Various Temperatures, 36 GHz, V_{DD} = 5 V, I_{DQ} = 850 mA

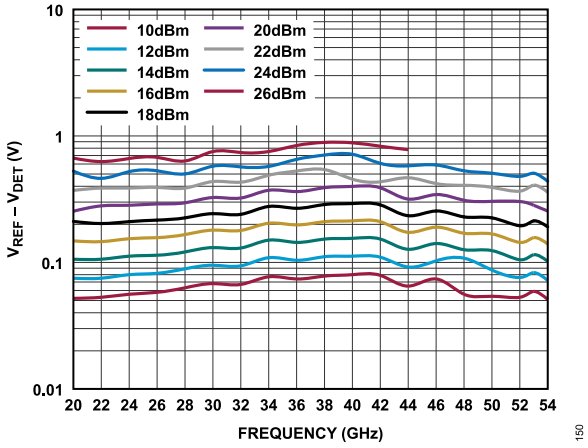

Figure 50. $V_{REF} – V_{DET}$ vs. Frequency for Various P_{OUT} Values, V_{DD} = 5 V, I_{DQ} = 850 mA

TYPICAL PERFORMANCE CHARACTERISTICS

LOWER BIAS OPERATION

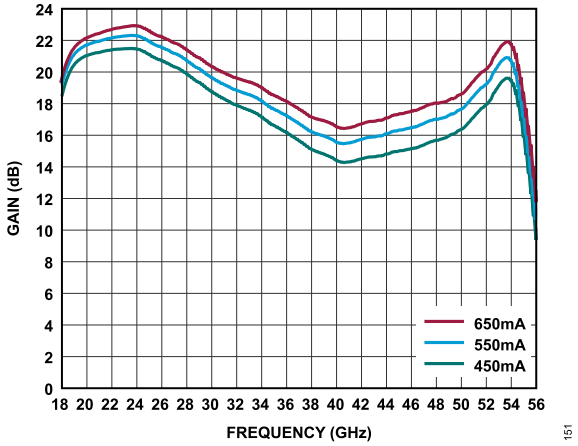

Figure 51. Gain vs. Frequency for Various I_{DQ} Values, V_{DD} = 3 V

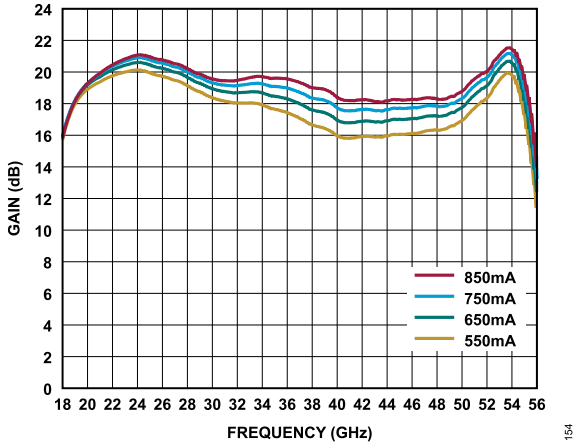

Figure 54. Gain vs. Frequency for Various I_{DQ} Values, V_{DD} = 4 V

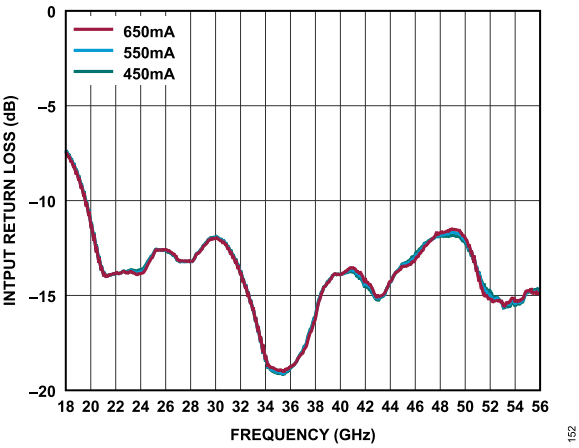

Figure 52. Input Return Loss vs. Frequency for Various I_{DQ} Values, V_{DD} = 3 V

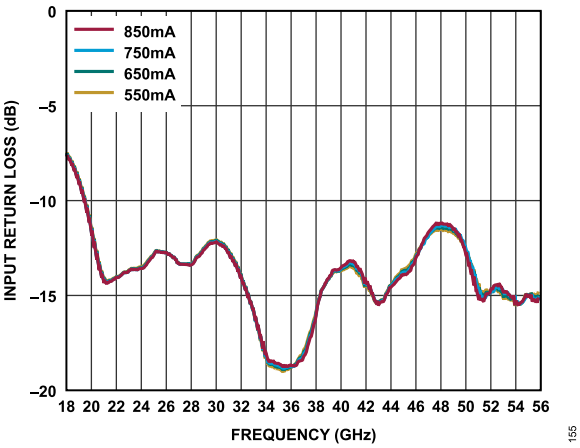

Figure 55. Input Return Loss vs. Frequency for Various I_{DQ} Values, V_{DD} = 4 V

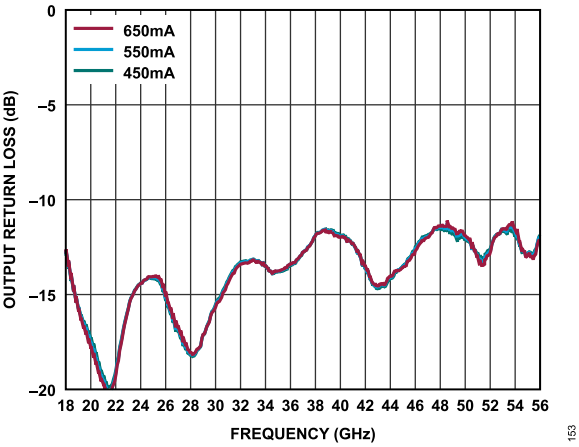

Figure 53. Output Return Loss vs. Frequency for Various I_{DQ} Values, V_{DD} = 3 V

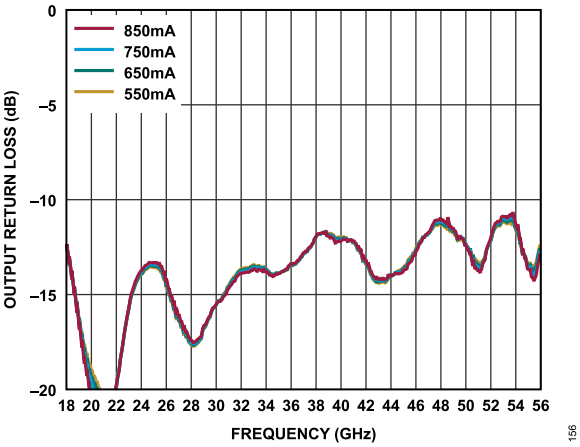

Figure 56. Output Return Loss vs. Frequency for Various I_{DQ} Values, V_{DD} = 4 V

TYPICAL PERFORMANCE CHARACTERISTICS

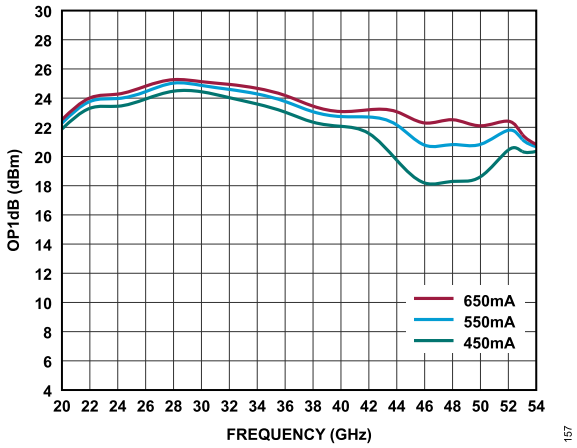

Figure 57. OP1dB vs. Frequency for Various I_{DQ} Values, V_{DD} = 3 V

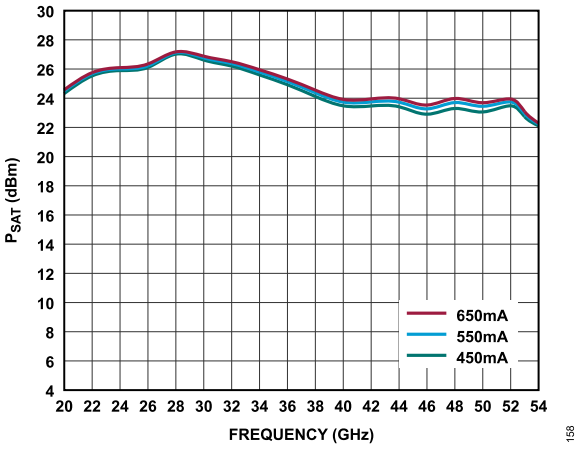

Figure 58. P_{SAT} vs. Frequency for Various I_{DQ} Values, V_{DD} = 3 V

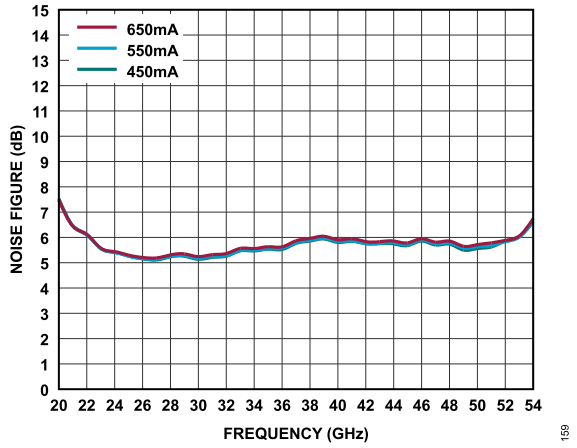

Figure 59. Noise Figure vs. Frequency for Various I_{DQ} Values, V_{DD} = 3 V

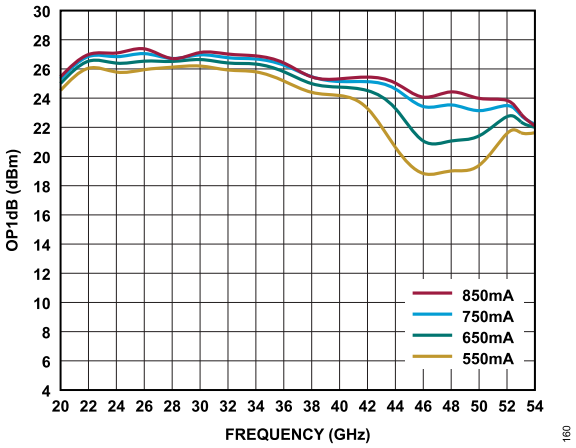

Figure 60. OP1dB vs. Frequency for Various I_{DQ} Values, V_{DD} = 4 V

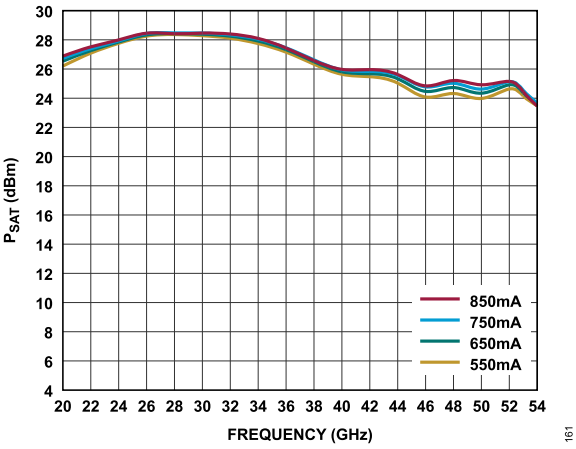

Figure 61. P_{SAT} vs. Frequency for Various I_{DQ} Values, V_{DD} = 4 V

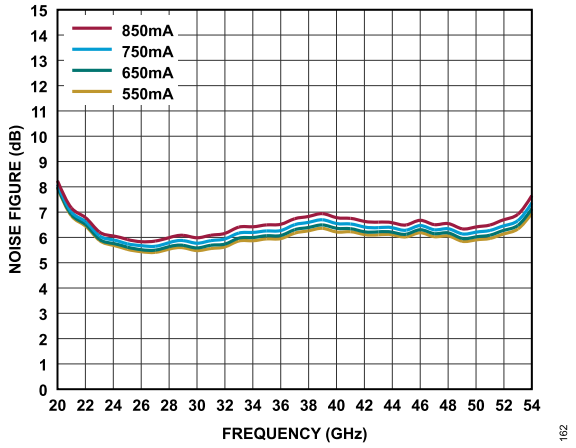

Figure 62. Noise Figure vs. Frequency for Various I_{DQ} Values, V_{DD} = 4 V

TYPICAL PERFORMANCE CHARACTERISTICS

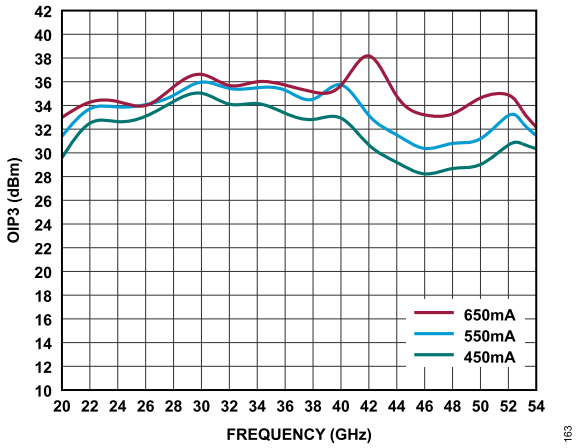

Figure 63. OIP3 vs. Frequency for Various I_{DQ} Values, P_{OUT} per Tone = 14 dBm, V_{DD} = 3 V

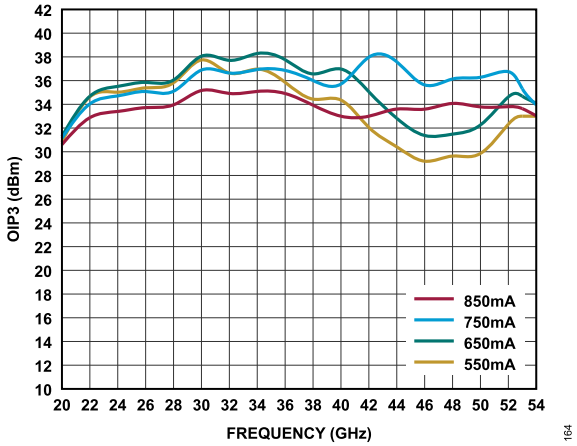

Figure 64. OIP3 vs. Frequency for Various I_{DQ} Values, P_{OUT} per Tone = 14 dBm, V_{DD} = 4 V

THEORY OF OPERATION

The ADPA7009-2 is a GaAs, pHEMT, medium power amplifier with integrated decoupling components. Figure 65 shows a simplified block diagram. The drain current is set by the negative voltage applied to the VGG1 pin. The drain bias voltage is applied through the VDD1 pin. The gate and drain can alternatively be biased through the VGG2 and VDD2 pins. Bias inductors and 0.1 µF and 100 pF decoupling capacitors are integrated. The ADPA7009-2 uses a cascaded, 4-stage amplifier operating in quadrature between two 90° hybrids.

The input signal is divided evenly in two. Each path is amplified through four independent gain stages. The amplified signals are then combined at the output. This balanced amplifier approach forms an amplifier with a combined gain of 17.5 dB and a P_{SAT} value of 28.5 dBm. The gate pins are internally connected and can be biased from either north or south of the circuit.

A portion of the RF output signal is directionally coupled to a diode for detection of the RF output power. When the diode is DC biased, the diode rectifies the RF power and makes the RF power available for measurement as a DC voltage at VDET. To allow temperature compensation of VDET, an identical and symmetrically located circuit, minus the coupled RF power, is available through VREF. Taking the difference of $V_{REF} - V_{DET}$ provides a temperature-compensated signal that is proportional to the RF output (see Figure 65).

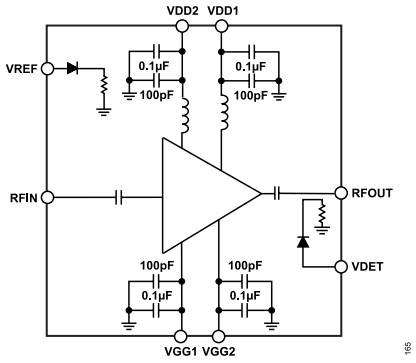

Figure 65. ADPA7009-2 Architecture

APPLICATIONS INFORMATION

The ADPA7009-2 can be biased though VGG1 and VDD1 (north side) or VGG2 and VDD2 (south side). Figure 66 shows the primary application circuit with north-side biasing. Figure 67 shows south-side biasing. The RFIN and RFOUT pins are internally AC-coupled.

Because VDD1, VDD2, VGG1, and VGG2 are internally decoupled, minimal external decoupling components are required on these pins.

VGG1 and VGG2 are the gate bias pins for the amplifier. VDD1 and VDD2 are the drain bias pins for the amplifier.

All measurements for this device were taken using the primary application circuit (see Figure 66).

See the ADPA7009-2-EVALZ user guide for information on using the evaluation board.

To avoid damaging the device, set VGG1 to −1.5 V before turning on VDD1. VGG1 can then be adjusted upwards until the desired I_{DQ} is achieved. Then, apply the RF input signal. If the desired gate voltage is known, VGG1 can be set to that voltage value directly without taking it to the pinch off voltage (−1.5 V).

To turn off the device, turn off the RF input signal, turn off VDD1, and then turn off VGG1.

The V_{DD} = 5 V and I_{DQ} = 850 mA bias conditions are recommended to optimize overall performance. Unless otherwise noted, the data shown was taken using the recommended bias conditions.

Operation of the ADPA7009-2 at different bias conditions may provide performance that differs from what is shown in Table 1 to Table 3. Biasing the ADPA7009-2 for higher drain current typically results in higher OP1dB and gain at the expense of increased power consumption (see Table 8).

Data for Table 8 was taken at the following nominal bias conditions: V_{DD} = 5 V, T_{CASE} = 25°C, and frequency = 36 GHz.

Table 8. Power Selection

I_{DQ} (mA)[1]	Gain (dB)	OP1dB (dBm)	OIP3 (dBm)	P_{DISS} (W) at P_{SAT}
650	18.5	26.5	38.0	3.80
750	19.0	27.0	37.0	4.08
850	19.5	27.5	34.5	4.30
950	19.7	27.8	32.5	4.49

[1] Adjust V_{GGx} from −1.5 V to 0 V to achieve the desired drain current.

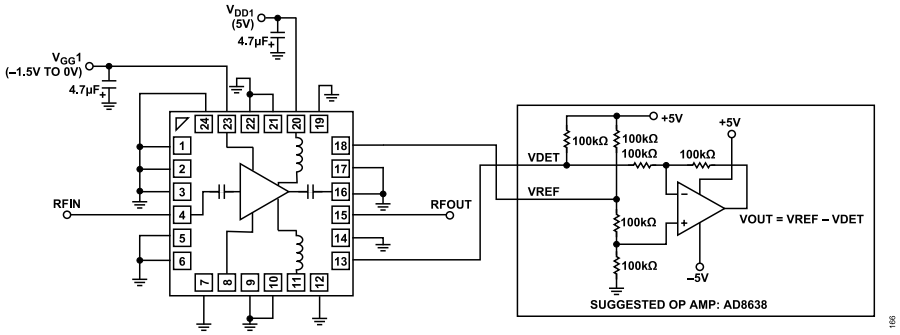

Figure 66. Primary Application Circuit (North-Side Biasing)

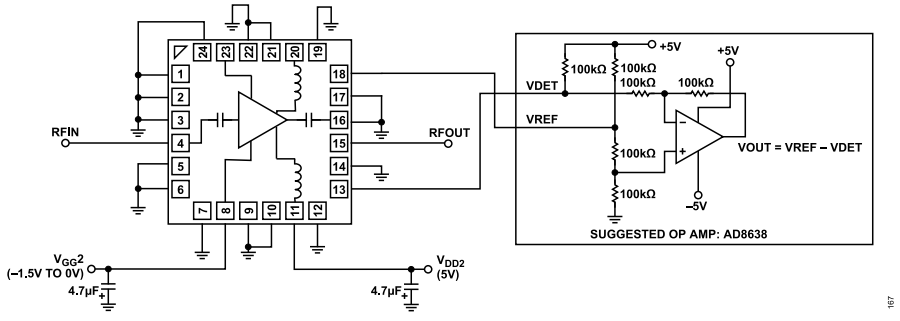

Figure 67. Alternate Application Circuit (South-Side Biasing)

BIASING THE ADPA7009-2 WITH THE HMC980LP4E

The HMC980LP4E is an active bias controller that is designed to meet the bias requirements for enhancement mode and depletion mode amplifiers such as the ADPA7009-2. The controller provides constant drain current biasing over temperature and device to device variation, and properly sequences gate and drain voltages to ensure the safe operation of the amplifier. The HMC980LP4E also offers self-protection in the event of a short circuit, an internal charge pump that generates the negative voltage needed on the gate of the ADPA7009-2, and the option to use an external negative voltage source. The HMC980LP4E is also available in die form as the HMC980-Die.

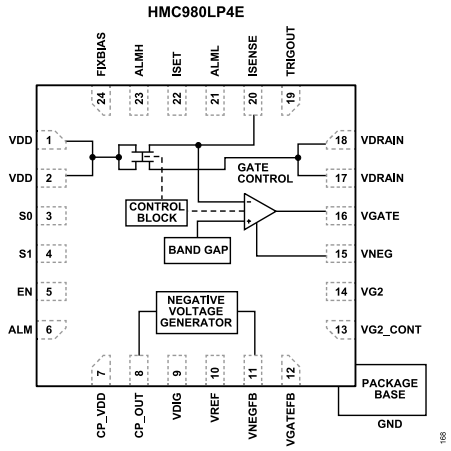

Figure 68. HMC980LP4E Active Bias Control

APPLICATION CIRCUIT SETUP

Figure 69 shows an application circuit using the HMC980LP4E to control the ADPA7009-2. When using an external negative supply for VNEG, see the application circuit shown in Figure 70.

In the application circuit shown in Figure 69, the ADPA7009-2 drain voltage (V_{DRAIN}) and drain current (I_{DRAIN}) are set by the following equations:

$$V_{DD} = V_{DRAIN} + (I_{DRAIN} \times 0.85\ \Omega)$$

$$V_{DD} = 5\ V + (0.95\ A \times 0.85\ \Omega) = 5.81\ V$$

where:
V_{DD} and V_{DRAIN} are in volts.
I_{DRAIN} is in amperes.

$$R10 = (150\ \Omega \times A) \div (I_{DRAIN})$$

$$R10 = (150\ \Omega \times A) \div (0.95\ A) = 158\ \Omega$$

where:
R10 is in ohms.
I_{DRAIN} is in amperes.

LIMITING VGATE FOR THE ADPA7009-2 VGGx ABSOLUTE MAXIMUM RATING REQUIREMENT

When using the HMC980LP4E to control the ADPA7009-2, the minimum voltages for VNEG and VGATE must be −1.5 V to keep the voltages within the absolute maximum rating limit for the VGGx pin of the ADPA7009-2. To set the minimum voltages, set R15 and R16 to the values shown in Figure 69 and Figure 70. Refer to the AN-1363 Application Note *Meeting Biasing Requirements of Externally Biased RF/Microwave Amplifiers with Active Bias Controllers* for more information and calculations for R15 and R16.

The HMC980LP4E application circuits for biasing figures in the AN-1363 Application Note are two examples of how the HMC980LP4E is used as an active bias controller. Both application circuits within the AN-1363 Application Note show the R5 and R7 resistors, which are analogous to the R15 and R16 resistors shown in Figure 69 and Figure 70.

BIASING THE ADPA7009-2 WITH THE HMC980LP4E

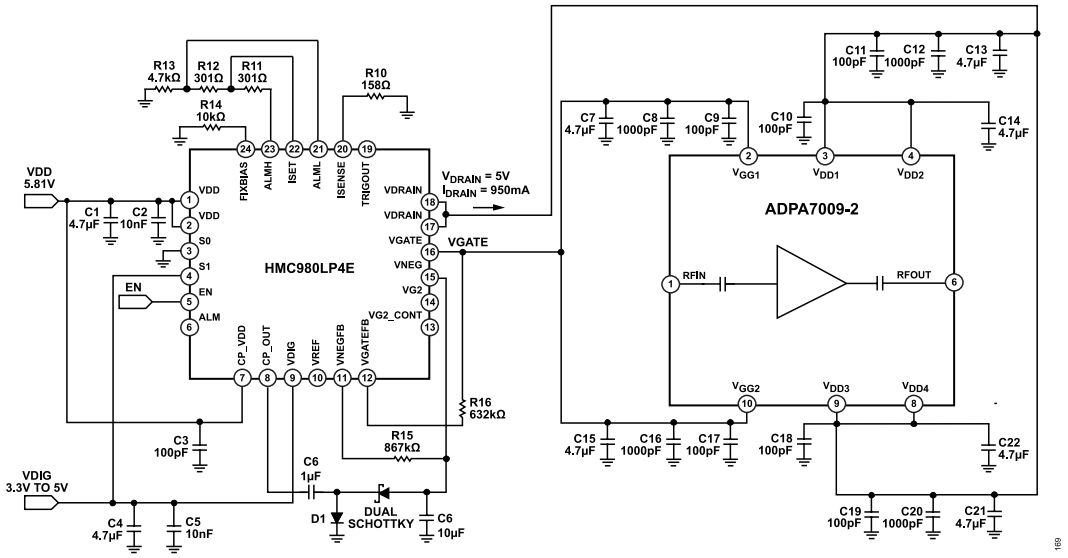

Figure 69. Application Circuit Using the HMC980LP4E with the ADPA7009-2 (Internal Negative Voltage Source)

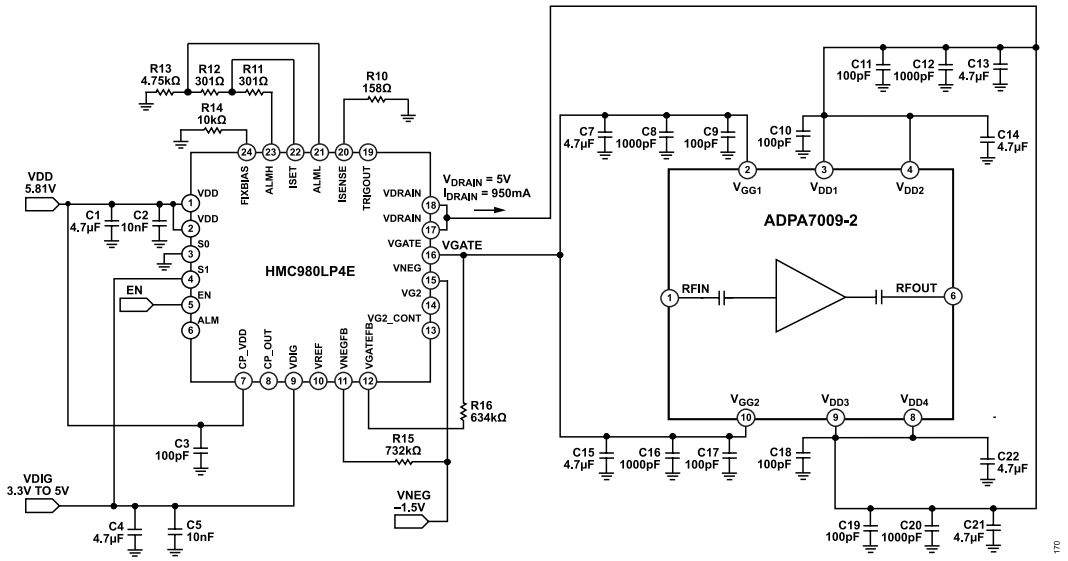

Figure 70. Application Circuit Using the HMC980LP4E with the ADPA7009-2 (External Negative Voltage Source)

HMC980LP4E BIAS SEQUENCE

The DC supply sequence described in this section is required to prevent damage to the HMC980LP4E when using the device to control the ADPA7009-2.

Power-Up Sequence

The power-up sequence for the HMC980LP4E is as follows:

1. Set VDIG = 3.3 V.
2. Set S0 = 3.3 V.
3. Set VDD = 5.81 V.
4. Set VNEG = −1.5 V (this step is unnecessary if using an internally generated voltage).
5. Set EN = 3.3 V (the transition from 0 V to 3.3 V turns on VGATE and VDRAIN).

Power-Down Sequence

The power-down sequence for the HMC980LP4E is as follows:

1. Set EN = 0 V (the transition from 3.3 V to 0 V turns off VDRAIN and VGATE).
2. Set VNEG = 0 V (this step is unnecessary if using and internally generated voltage).
3. Set VDD = 0 V.
4. Set S0 = 0 V.
5. Set VDIG = 0 V.

BIASING THE ADPA7009-2 WITH THE HMC980LP4E

After the HMC980LP4E bias control circuit is set up, toggle the bias to the ADPA7009-2 on or off by applying 3.3 V or 0 V, respectively, to the EN pin. At EN = +3.3 V, VGATE drops to −1.5 V, and VDRAIN turns on at +5 V. VGATE then rises until I_{DRAIN} = 950 mA, and the closed control loop regulates I_{DRAIN} at 950 mA. When EN = 0 V, VGATE is set to −1.5 V, and VDRAIN is set to 0 V.

CONSTANT DRAIN CURRENT BIASING VS. CONSTANT GATE VOLTAGE BIASING

The HMC980LP4E uses closed-loop feedback to continuously adjust VGATE to maintain a constant drain current bias over DC supply variation, temperature, and device-to-device variation. In addition, constant drain current bias is the optimum method for reducing time in calibration procedures and for maintaining consistent performance over time. Comparing the constant drain current bias with a constant gate voltage bias where the current is driven to increase when RF power is applied, a slightly lower OP1dB is seen with a constant drain current bias. This OP1dB is shown in Figure 78, where the RF performance is slightly lower than the constant gate voltage bias operation due to a lower drain current at the high input powers as the device reaches 1 dB compression.

To increase the OP1dB performance for the constant drain current bias toward the constant gate voltage bias performance, increase the setpoint current, bringing it closer to the maximum I_{DD} current, as shown in Figure 78. The limit of increasing I_{DQ} under the constant drain current operation is set by the thermal limitations found in Table 4 with the maximum power-dissipation specification. As the I_{DD} increase continues, the actual OP1dB does not continue to increase indefinitely, and the power dissipation increases. Therefore, when using constant drain current biasing, take the trade-off between the power dissipation and the output P1dB performance into consideration.

CONSTANT I_{DD} OPERATION

T_{CASE} = 25°C, V_{DD} = 5 V, and I_{DD} = 950 mA for nominal operation, unless otherwise noted. Figure 71 to Figure 78 are biased with the HMC980LP4E active bias controller. See the Biasing the ADPA7009-2 with the HMC980LP4E section for biasing details.

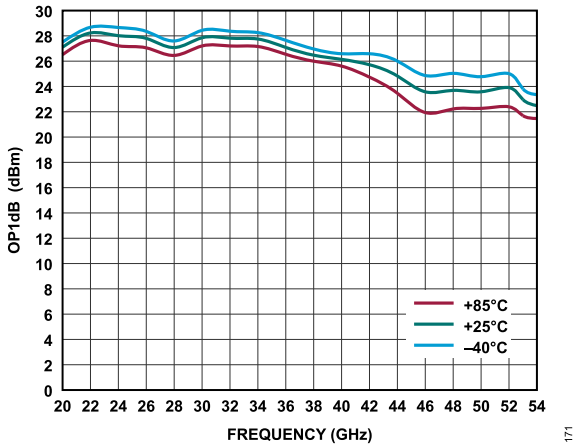

Figure 71. OP1dB vs. Frequency for Various Temperatures, V_{DD} = 5 V, Data Measured with Constant I_{DD} = 950 mA

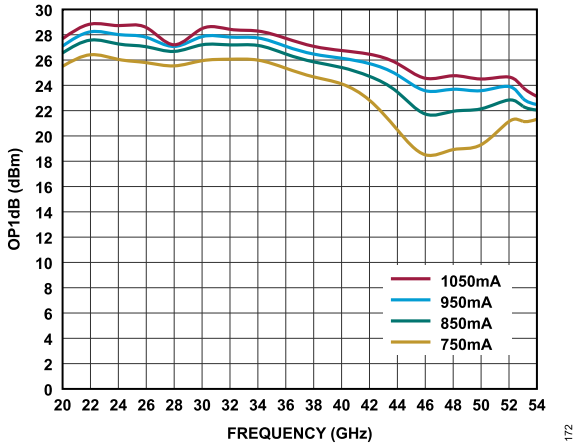

Figure 72. OP1dB vs. Frequency for Various I_{DQ} Values, V_{DD} = 5 V, Data Measured with Constant I_{DD} = 950 mA

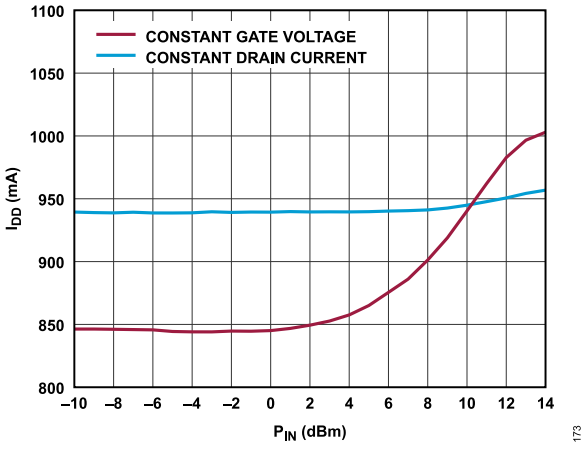

Figure 73. I_{DD} vs. P_{IN}, V_{DD} = 5 V, Frequency = 36 GHz, Constant Drain Current (I_{DRAIN} Setpoint = 950 mA) and Constant Gate Voltage (I_{DQ} = 850 mA)

BIASING THE ADPA7009-2 WITH THE HMC980LP4E

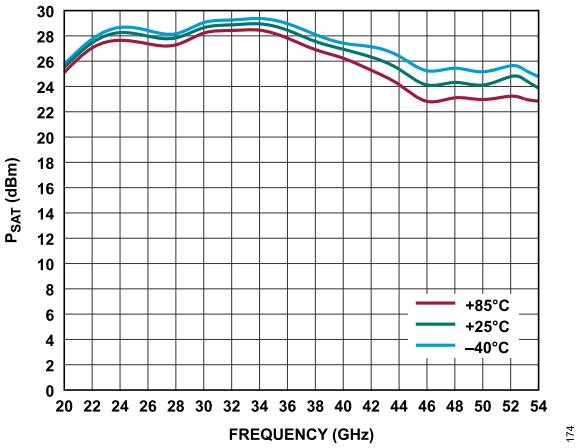

Figure 74. P_{SAT} vs. Frequency for Various Temperatures, V_{DD} = 5 V, Data Measured with Constant I_{DD} = 950 mA

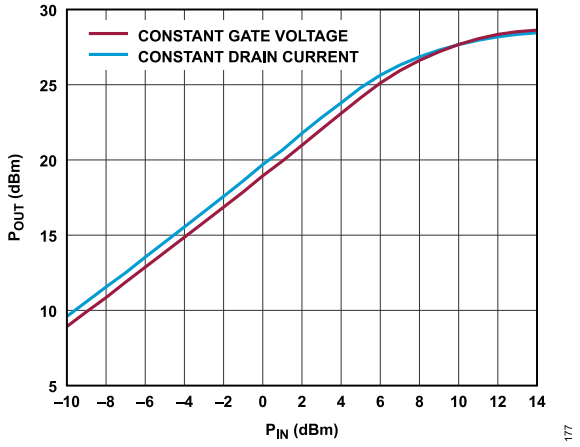

Figure 77. P_{OUT} vs. P_{IN}, V_{DD} = 5 V, Frequency = 36 GHz, Constant Drain Current (I_{DRAIN} Setpoint = 950 mA) and Constant Gate Voltage (I_{DQ} = 850 mA)

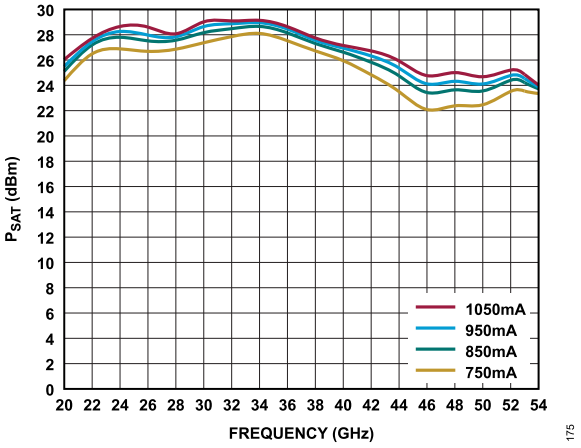

Figure 75. P_{SAT} vs. Frequency for Various I_{DQ} Values, V_{DD} = 5 V, Data Measured with Constant I_{DD}

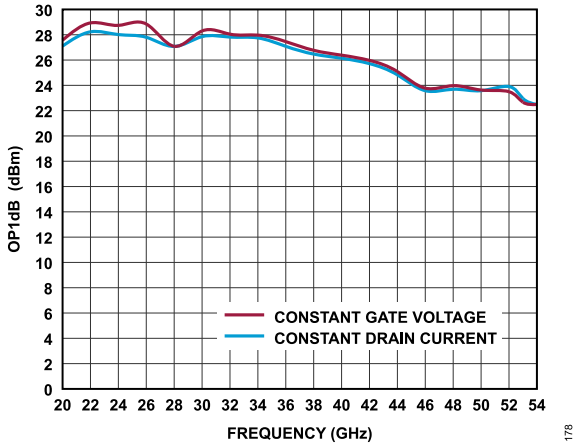

Figure 78. OP1dB vs. Frequency, V_{DD} = 5 V, Constant Drain Current (I_{DRAIN} Setpoint = 950 mA) and Constant Gate Voltage (I_{DQ} = 850 mA)

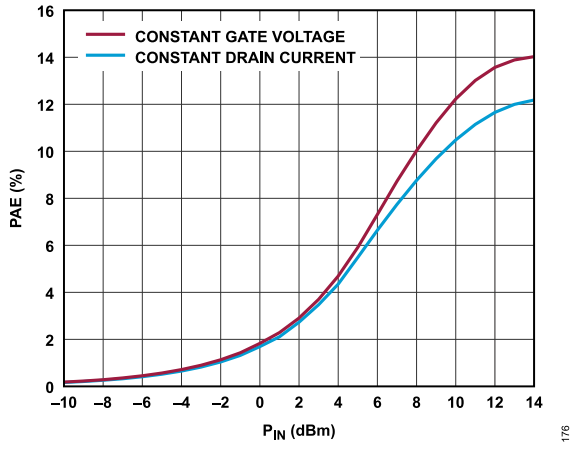

Figure 76. PAE vs. P_{IN}, V_{DD} = 5 V, Frequency = 36 GHz, Constant Drain Current (I_{DRAIN} Setpoint = 950 mA) and Constant Gate Voltage (I_{DQ} = 850 mA)

OUTLINE DIMENSIONS

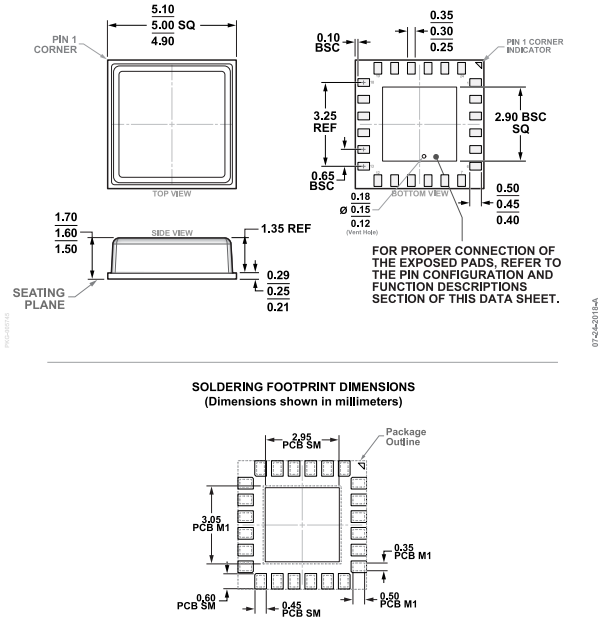

Figure 79. 24-Terminal Chip Array Small Outline No Lead Cavity [LGA_CAV]
5.00 mm × 5.00 mm Body and 1.60 mm Package Height
(CE-24-2)
Dimensions shown in millimeters

Updated: August 09, 2022

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Packing Quantity	Package Option
ADPA7009-2ACEZ	−40°C to +85°C	24-Terminal Chip Array Small Outline No Lead Cavity [LGA_CAV]	Tray, 1	CE-24-2
ADPA7009-2ACEZ-R7	−40°C to +85°C	24-Terminal Chip Array Small Outline No Lead Cavity [LGA_CAV]	Reel, 500	CE-24-2

[1] Z = RoHS-Compliant Part.

EVALUATION BOARDS

Model[1]	Description
ADPA7009-2-EVALZ	Evaluation Board

[1] Z = RoHS-Compliant Part.