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Single 3-Input OR Gate

NL17SZ332

The NL17SZ332 is a single 3-input OR Gate in tiny footprint packages.

Features

- Designed for 1.65 V to 5.5 V V_{CC} Operation
- 2.4 ns t_{PD} at $V_{CC} = 5 V (Typ)$
- Inputs/Outputs Overvoltage Tolerant up to 5.5 V
- IOFF Supports Partial Power Down Protection
- Source/Sink 24 mA at 3.0 V
- Chip Complexity < 100 FETs
- This Device is Pb-Free, Halogen Free/BFR Free and is RoHS Compliant



Figure 1. Logic Symbol



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MARKING DIAGRAMS



SC-74 CASE 318F-05



XM



UDFN6 1.45 x 1.0 CASE 517AQ



Μ

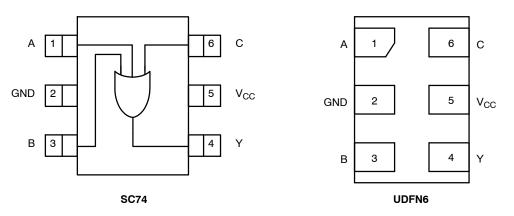
UDFN6 1.0 x 1.0 CASE 517BX



X, XX = Specific Device Code = Date Code = Pb-Free Package

ORDERING INFORMATION

See detailed ordering, marking and shipping information in the package dimensions section on page 6 of this data sheet.





PIN ASSIGNMENT

Pin	Function
1	A
2	GND
3	В
4	Y
5	V _{CC}
6	С

FUNCTION TABLE (Y = A + B + C)

	Input				
Α	В	С	Y		
Н	Х	Х	Н		
Х	Н	Х	Н		
Х	Х	Н	Н		
L	L	L	L		

H = HIGH Logic Level L = LOW Logic Level X = Either LOW or HIGH Logic Level

MAXIMUM RATINGS

Symbol	Characteristics		Value	Unit
V _{CC}	DC Supply Voltage		–0.5 to +6.5	V
V _{IN}	DC Input Voltage		-0.5 to +6.5	V
V _{OUT}		tive-Mode (High or Low State) Tri-State Mode (Note 1) ower-Down Mode (V _{CC} = 0 V)	-0.5 to V _{CC} + 0.5 -0.5 to +6.5 -0.5 to +6.5	V
I _{IK}	DC Input Diode Current	V _{IN} < GND	-50	mA
I _{OK}	DC Output Diode Current	V _{OUT} < GND	-50	mA
IOUT	DC Output Source/Sink Current		±50	mA
I _{CC} or I _{GND}	DC Supply Current per Supply Pin or Ground Pin		±100	mA
T _{STG}	Storage Temperature Range		-65 to +150	°C
ΤL	Lead Temperature, 1 mm from Case for 10 secs		260	°C
TJ	Junction Temperature Under Bias		+150	°C
θ_{JA}	Thermal Resistance (Note 2)	SC-74 UDFN6	320 154	°C/W
P _D	Power Dissipation in Still Air	SC-74 UDFN6	390 812	mW
MSL	Moisture Sensitivity		Level 1	-
F _R	Flammability Rating	Oxygen Index: 28 to 34	UL 94 V-0 @ 0.125 in	-
V _{ESD}	ESD Withstand Voltage (Note 3)	Human Body Model Charged Device Model	2000 1000	V
I _{Latchup}	Latchup Performance (Note 4)		±100	mA

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

Applicable to devices with outputs that may be tri-stated.
Measured with minimum pad spacing on an FR4 board, using 10mm-by-1inch, 2 ounce copper trace no air flow per JESD51-7.
HBM tested to ANSI/ESDA/JEDEC JS-001-2017. CDM tested to EIA/JESD22-C101-F. JEDEC recommends that ESD qualification to EIA/JESD22-A115-A (Machine Model) be discontinued per JEDEC/JEP172A.

4. Tested to EIA/JESD78 Class II.

RECOMMENDED OPERATING CONDITIONS

Symbol	Chara	acteristics	Min	Max	Unit
V _{CC}	Positive DC Supply Voltage		1.65	5.5	V
V _{IN}	DC Input Voltage		0	5.5	V
V _{OUT}	DC Output Voltage	Active-Mode (High or Low State) Tri-State Mode (Note 1) Power-Down Mode (V _{CC} = 0 V)	0 0 0	V _{CC} 5.5 5.5	
T _A	Operating Temperature Range		-55	+125	°C
t _r , t _f	Input Rise and Fall Time	$\begin{array}{l} V_{CC} = 1.65 \; V \; \text{to} \; 1.95 \; V \\ V_{CC} = 2.3 \; V \; \text{to} \; 2.7 \; V \\ V_{CC} = 3.0 \; V \; \text{to} \; 3.6 \; V \\ V_{CC} = 4.5 \; V \; \text{to} \; 5.5 \; V \end{array}$	0 0 0	20 20 10 5	ns/V

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

			V _{CC}	Т	م = 25°0	C	–55°C ≤ T _A ≤ 125°C		
Symbol	Parameter	Condition	(V)	Min	Тур	Max	Min	Max	Units
VIH	High-Level Input		1.65 to 1.95	0.65 V _{CC}	-	-	0.65 V _{CC}	_	V
	Voltage		2.3 to 5.5	0.70 V _{CC}	-	-	0.70 V _{CC}	-	
VIL	Low-Level Input		1.65 to 1.95	-	-	0.35 V _{CC}	-	0.35 V _{CC}	V
	Voltage		2.3 to 5.5	_	-	0.30 V _{CC}	-	0.30 V _{CC}	
V _{OH}	High-Level Output Voltage		1.65 to 5.5 1.65 2.3 3.0 3.0 4.5	V _{CC} - 0.1 1.29 1.9 2.4 2.3 3.8	V _{CC} 1.4 2.1 2.7 2.5 4.0	- - - - -	V _{CC} - 0.1 1.29 1.9 2.4 2.3 3.8	- - - - -	V
V _{OL}	Low-Level Output Voltage		1.65 to 5.5 1.65 2.3 3.0 3.0 4.5	- - - - -	- 0.08 0.2 0.28 0.38 0.42	0.1 0.24 0.3 0.4 0.55 0.55		0.1 0.24 0.3 0.4 0.55 0.55	V
I _{IN}	Input Leakage Current	V_{IN} = 5.5 V or GND	1.65 to 5.5	-	-	±0.1	-	±1.0	μA
I _{OFF}	Power Off Leakage Current	V_{IN} = 5.5 V or V_{OUT} = 5.5 V	0	-	_	1.0	_	10	μΑ
I _{CC}	Quiescent Supply Current	$V_{IN} = V_{CC}$ or GND	5.5	-	-	1.0	_	10	μΑ

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

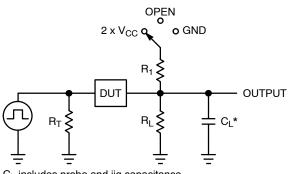
AC ELECTRICAL CHARACTERISTICS

			V _{CC} T _A = 25°C		С	–55°C ≤ T			
Symbol	Parameter	Condition	(V)	Min	Тур	Max	Min	Max	Units
t _{PLH} , Propagation Delay, A to Y	R_L = 1 M Ω , C_L = 15 pF	1.65 to 1.95	I	6.5	18.5	-	19.0	ns	
t _{PHL}	(Figures 3 and 4)	R_L = 1 M Ω , C_L = 15 pF	2.3 to 2.7	I	3.0	11.0	-	11.5	
		R_L = 1 MΩ, C_L = 15 pF	3.0 to 3.6	-	2.4	7.5	-	8.0	
		$R_L = 500 \ \Omega$, $C_L = 50 \ pF$		-	1.9	5.5	-	6.0	
		$R_L = 1 M\Omega$, $C_L = 15 pF$	4.5 to 5.5	-	3.0	8.5	_	9.0	
		$R_L = 500 \ \Omega$, $C_L = 50 \ pF$		-	2.4	7.0	-	7.5	

CAPACITIVE CHARACTERISTICS

Symbol	Parameter	Condition	Typical	Units
C _{IN}	Input Capacitance	V_{CC} = 5.5 V, V_{IN} = 0 V or V_{CC}	2.5	pF
C _{OUT}	Output Capacitance	V_{CC} = 5.5 V, V_{IN} = 0 V or V_{CC}	2.5	pF
C _{PD}	Power Dissipation Capacitance (Note 5)	10 MHz, V _{CC} = 3.3 V, V _{IN} = 0 V or V _{CC} 10 MHz, V _{CC} = 5.5 V, V _{IN} = 0 V or V _{CC}	9 11	pF

5. C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: $I_{CC(OPR)} = C_{PD} \bullet V_{CC} \bullet f_{in} + I_{CC}$. C_{PD} is used to determine the no-load dynamic power consumption; $P_D = C_{PD} \bullet V_{CC}^2 \bullet f_{in} + I_{CC} \bullet V_{CC}$.

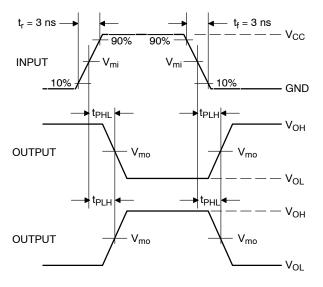


Switch Position	C _L , pF	R_{L}, Ω	R ₁ , Ω		
Open	See AC Characteristics Table				
$2 \times V_{CC}$	50	500	500		
GND	50	500	500		
	Position Open 2 x V _{CC}	Position Entropy Open See AC Character 2 x V _{CC} 50	Position End Open See AC Characteristics Tall 2 x V _{CC} 50		

X = Don't Care

 C_L includes probe and jig capacitance R_T is Z_{OUT} of pulse generator (typically 50 $\Omega)$ f = 1 MHz

Figure 3. Test Circuit



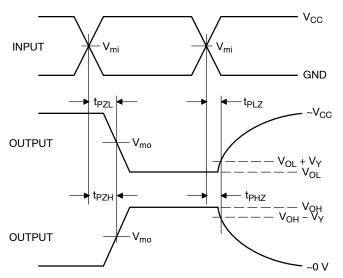


Figure 4. Switching Waveforms

		v		
V _{CC} , V	V _{mi} , V	t _{PLH} , t _{PHL}	t _{PZL} , t _{PLZ} , t _{PZH} , t _{PHZ}	V _Y , V
1.65 to 1.95	V _{CC} / 2	V _{CC} / 2	V _{CC} / 2	0.15
2.3 to 2.7	V _{CC} / 2	V _{CC} / 2	V _{CC} / 2	0.15
3.0 to 3.6	V _{CC} / 2	V _{CC} / 2	V _{CC} / 2	0.3
4.5 to 5.5	V _{CC} / 2	V _{CC} / 2	V _{CC} / 2	0.3

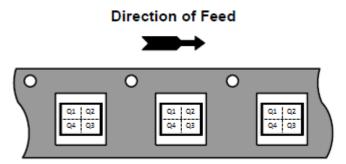
DEVICE ORDERING INFORMATION

Device	Packages	Specific Device Code	Pin 1 Orientation (See below)	Shipping [†]
NL17SZ332DBVT1G	SC-74	AE	Q4	3000 / Tape & Reel
NL17SZ332MU1TCG (In Development)	UDFN6, 1.45x1.0, 0.5P	6	Q4	3000 / Tape & Reel
NL17SZ332MU3TCG (In Development)	UDFN6, 1.0x1.0, 0.35P	6	Q4	3000 / Tape & Reel

+For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

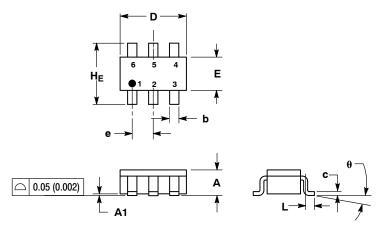
*NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable.

Pin 1 Orientation in Tape and Reel



PACKAGE DIMENSIONS

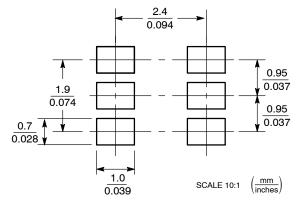
SC-74 CASE 318F-05 **ISSUE N**



- NOTES: 1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982. 2. CONTROLLING DIMENSION: INCH. 3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL. 4. 318F-01, -02, -03, -04 OBSOLETE. NEW STANDARD 318F-05.

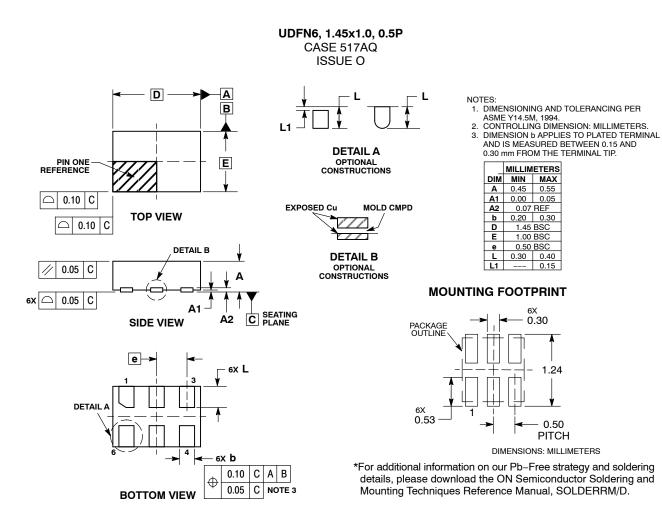
	М	ILLIMETE	RS	INCHES			
DIM	MIN	NOM	MAX	MIN	NOM	MAX	
Α	0.90	1.00	1.10	0.035	0.039	0.043	
A1	0.01	0.06	0.10	0.001	0.002	0.004	
b	0.25	0.37	0.50	0.010	0.015	0.020	
С	0.10	0.18	0.26	0.004	0.007	0.010	
D	2.90	3.00	3.10	0.114	0.118	0.122	
Е	1.30	1.50	1.70	0.051	0.059	0.067	
е	0.85	0.95	1.05	0.034	0.037	0.041	
L	0.20	0.40	0.60	0.008	0.016	0.024	
HE	2.50	2.75	3.00	0.099	0.108	0.118	
θ	0°	-	10°	0°	-	10°	

SOLDERING FOOTPRINT*

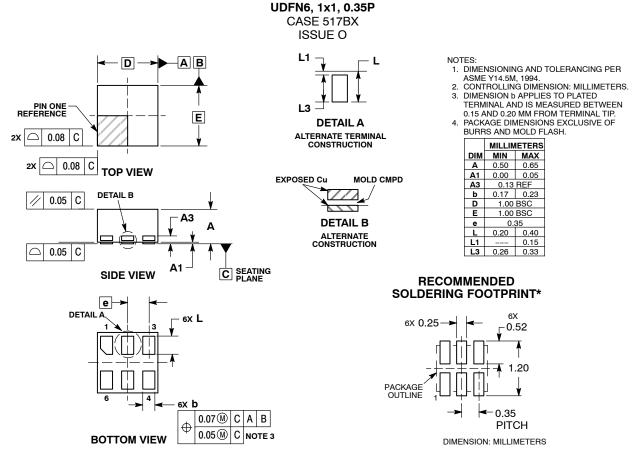


*For additional information on our Pb–Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PACKAGE DIMENSIONS



PACKAGE DIMENSIONS



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