



# Industrial PCIe U.2 SSD Specification

## (HIX Series, 3D TLC)

**Version 1.6**

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# 1. GENERAL DESCRIPTION



## 1.1. Introduction

FLEXXON’s HIX U.2 PCIe SSD has PCIe Gen3x4 interface, and is fully compliant with NVMe 1.3 industrial standard. It supports ultimate performance, high density and great reliability, suitable for enterprise application.

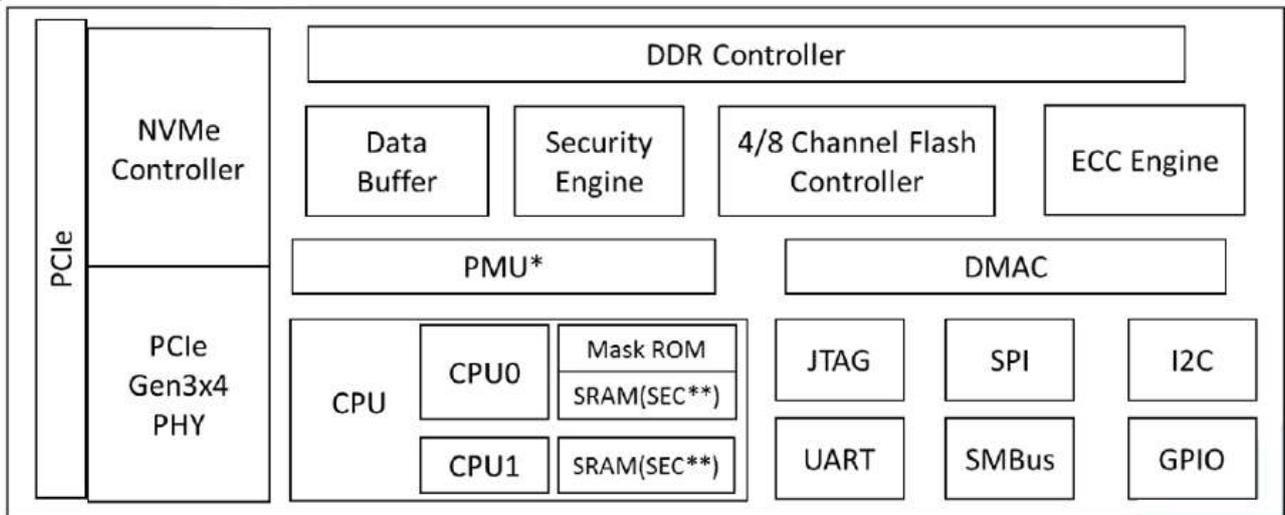


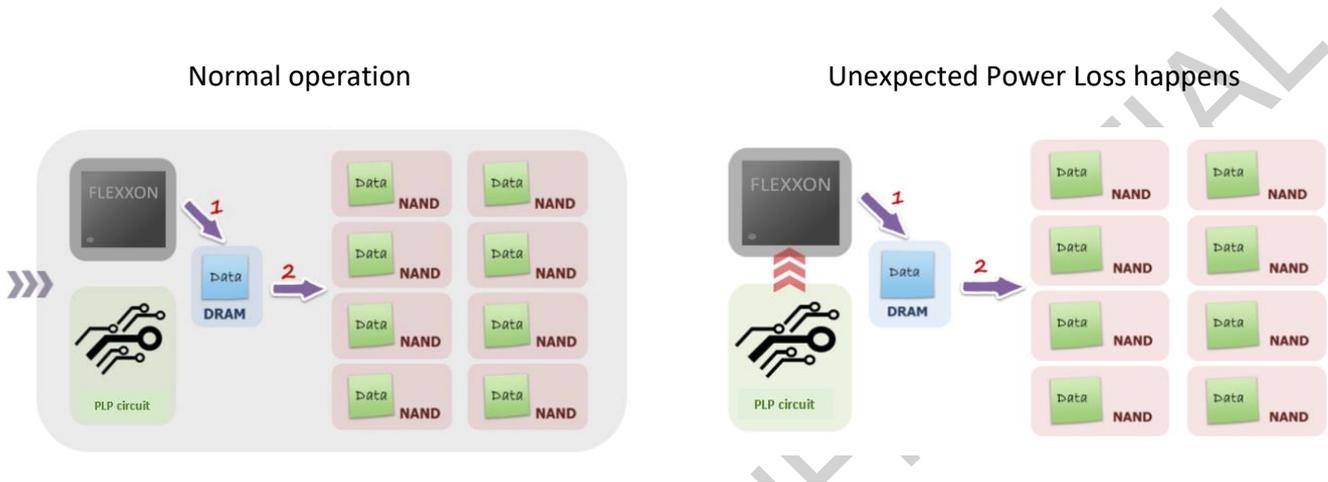
Figure 1-1 HIX U.2 PCIe SSD Controller Block Diagram

## 1.2. Product Overview

- ❖ **Flash**
  - 3D TLC
- ❖ **Capacity**
  - 240GB ~ 7680GB
- ❖ **PCIe Interface**
  - Compliant with NVMe 1.3
  - Compatible with PCIe I/II/III x4 interface
  - Support power management
- ❖ **ECC Scheme**
  - LDPC (Low Density Parity Check) of ECC algorithm
- ❖ **GPIO**
- ❖ **UART**
- ❖ **Dynamic and Static Wear Leveling**
- ❖ **Support SMART and TRIM commands**
- ❖ **Power Loss Protection Algorithm**
- ❖ **Support AES256/TCG OPAL**
- ❖ **Support PYRITE (Optional)**
- ❖ **Secure Erase**
- ❖ **Temperature Range**
  - Operation (Silver) : 0°C ~ 70°C
  - Operation (Diamond) : -40°C ~ 85°C
  - Storage: -40°C ~ 85°C
- ❖ **RoHS Compliant**
- ❖ **Conformal Coating (Optional)**

### 1.3. Power Loss Protection (Optional)

FLEXON designs SSD device with a hardware power loss protection mechanism. It has a voltage drop detector, so when the SSD device detects the host power dropping, the SSD's power loss protection circuit will be triggered and begin providing power to the SSD. The SSD then will start to flush cached data from DRAM memory to NAND flash memory in order to preserve data integrity and prevent data loss.



The SSD is powered by the host power, and the power loss protection circuit is charged by the host power.

When the SSD detects the host power dropping, the power loss protection circuit starts to provide power to the SSD while it flushes cached data from DRAM to NAND.

Figure 1-2 power loss protection mechanism

## 2. PRODUCT SPECIFICATIONS



### 2.1. Performance

Table 2-1 Performance of HIX U.2 PCIe SSD

Capacity	Sequential		Random	
	Read (MB/s)	Write (MB/s)	Read (IOPS)	Write (IOPS)
240GB	3,000	340	100K	13K
480GB	3,000	520	200K	20K
960GB	3,200	1,000	360K	25K
1920GB	3,200	1,000	360K	28K
3840GB	2,900	970	400K	30K
7680GB	2,900	970	400K	30K

**NOTES:**

1. Performance may differ according to flash configuration and platform.

### 2.2. Power

Table 2-2 Supply Voltage of HIX U.2 PCIe SSD

Parameter	Rating
Operating Voltage	12V

### 2.3. TBW (Terabytes Written)

Capacity	TBW
240GB	380
480GB	804
960GB	1625
1920GB	3100
3840GB	6050
7680GB	12100

## 2.4. MTBF

MTBF, an acronym for Mean Time Between Failures, is a measure of a device's reliability. Its value represents the average time between a repair and the next failure. The predicted result of FLEXON's HIX PCIe U.2 SSD is more than 2 million hours.

## 2.5. Data Retention

- 10 years if > 90% life remaining (@25C)
- 1 year if < 10% life remaining (@25C)

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### 3. ENVIRONMENTAL SPECIFICATIONS



Test Items	Test Conditions
Storage Temperature	-40°C ~ 85°C
Operating Temperature	Silver Grade: 0°C ~ 70°C Diamond Grade: -40°C ~ 85°C
Storage Humidity	40°C, 93% RH
Operating Humidity	40°C, 90% RH
Shock	1500G, Half Sin Pulse Duration 0.5ms
Vibration	80Hz ~ 2000Hz/20G, 20Hz ~ 80Hz/1.52mm, 3 axis/60min
Drop	80cm free fall, 6 face of each unit
Bending	≥ 20N, Hold 1 min/5 times
ESD	24°C, 49% RH, +/-4KV

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## 4. SUPPORTED COMMANDS



**Table 4-1 Admin Commands**

Identifier	Command Description
00h	Delete I/O Submission Queue
01h	Create I/O Submission Queue
02h	Get Log Page
04h	Delete I/O Completion Queue
05h	Create I/O Completion Queue
06h	Identify
08h	Abort
09h	Set Feature
0Ah	Get Feature
0Ch	Asynchronous Event Request
10h	Firmware Commit
11h	Firmware Image Download
14h	Device Self-test
80h	Format NVM
81h	Security Send
82h	Security Receive
84h	Sanitize

**Table 4-2 I/O Commands**

Identifier	Command Description
00h	Flush
01h	Write
02h	Read
04h	Write Uncorrectable
05h	Compare
08h	Write Zeroes
09h	Dataset Management

**Table 4-3 Set Feature Commands**

Identifier	Command Description
00h	Reserved
01h	Arbitration
02h	Power Management
03h	LBA Range Type
04h	Temperature Threshold
05h	Error Recovery
06h	Volatile Write Cache
07h	Number of Queues
08h	Interrupt Coalescing
09h	Interrupt Vector Configuration
0Ah	Write Atomicity Normal
0Bh	Asynchronous Event Configuration
0Ch	Autonomous Power State Transition
0Dh	Host Memory Buffer
0Eh	Timestamp
10h	Host Controlled Thermal Management
11h	Non-Operational Power State Config
0Eh-7Dh	Reserved
80h	Software Progress Marker

**Table 4-4 Get Log Page Commands**

Identifier	Command Description
00h	Reserved
01h	Error Information
02h	SMART / Health Information
03h	Firmware Slot Information
04h	Changed Namespace List
06h	Device Self-test
09h-07h	Reserved
81h	Sanitize Status
82h-FFh	Reserved

## 5. PIN ASSIGNMENT

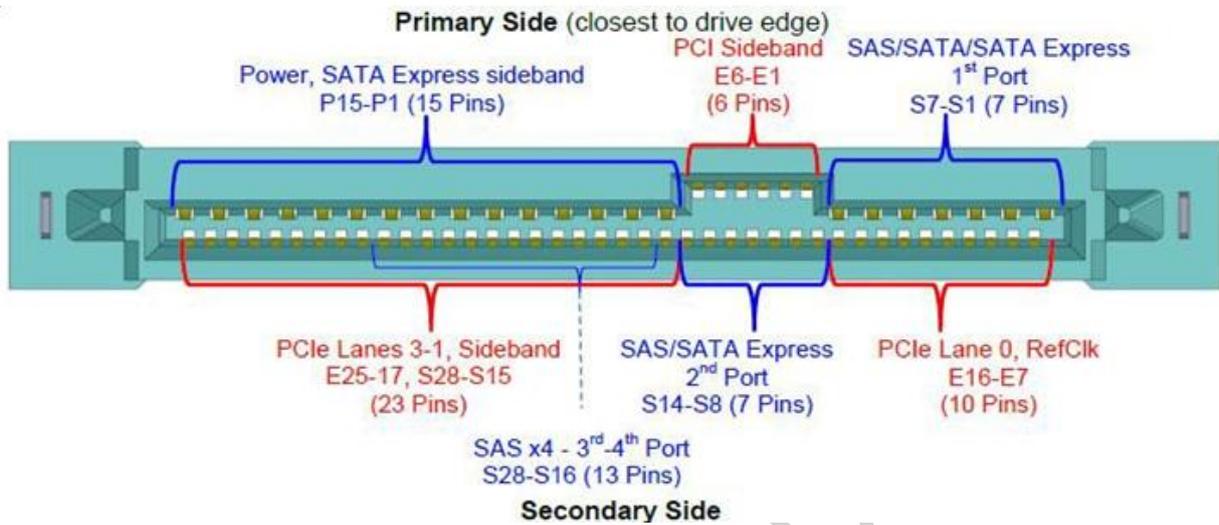


Figure 5-1 HIX U.2 PCIe SSD Pin Locations

Table 5-1 U.2 PCIe SSD SFF-8639 Connector Pin Assignment and Descriptions

Pin Number	Name	Type	Description
P1	WAKE#	Input	Signal for Link reactivation
P2	-	-	Outside scope of this specification
P3	CLKREQ#	Bi-Dir	Clock request
P4	IfDet#	Input	Interface Type Detect
P5	Ground	Ground	Ground
P6	Ground	Ground	Ground
P7	-	-	Outside scope of this specification
P8	-	-	Outside scope of this specification
P9	-	-	Outside scope of this specification
P10	PRSNT#	Input	Presence detect
P11	Activity	Input	
P12	Ground	Ground	Ground
P13	+12V Precharge	Power	+12V Precharge power for SFF-8639 module
P14	+12V	Power	+12V power for SFF-8639 module
P15	+12V	Power	+12V power for SFF-8639 module
S1	Ground	Ground	Ground
S2	-	-	Outside scope of this specification
S3	-	-	Outside scope of this specification
S4	Ground	Ground	Ground

Pin Number	Name	Type	Description
S5	-	-	Outside scope of this specification
S6	-	-	Outside scope of this specification
S7	Ground	Ground	Ground
S8	Ground	Ground	Ground
S9	-	-	Outside scope of this specification
S10	-	-	Outside scope of this specification
S11	Ground	Ground	Ground
S12	-	-	Outside scope of this specification
S13	-	-	Outside scope of this specification
S14	Ground	Ground	Ground
S15	Reserved	-	Reserved
S16	Ground	Ground	Ground
S17	PETp1	Diff-Pair	Transmitter differential pair, Lane 1
S18	PETn1	Diff-Pair	Transmitter differential pair, Lane 1
S19	Ground	Ground	Ground
S20	PERn1	Diff-Pair	Receiver differential pair, Lane 1
S21	PERp1	Diff-Pair	Receiver differential pair, Lane 1
S22	Ground	Ground	Ground
S23	PETp2	Diff-Pair	Transmitter differential pair, Lane 2
S24	PETn2	Diff-Pair	Transmitter differential pair, Lane 2
S25	Ground	Ground	Ground
S26	PERn2	Diff-Pair	Receiver differential pair, Lane 2
S27	PERp2	Diff-Pair	Receiver differential pair, Lane 2
S28	Ground	Ground	Ground
E1	REFCLKB+	Diff-Pair	Reference clock (differential pair) for second X2 port
E2	REFCLKB-	Diff-Pair	Reference clock (differential pair) for second X2 port
E3	+3.3 Vaux	Power	3.3 V auxiliary power
E4	PERSTB#	Output	Fundamental reset for second X2 port
E5	PERST#	Output	Fundamental reset (if dual-port enabled, first X2 port)
E6	Reserved	-	Reserved
E7	REFCLK+	Diff-Pair	Reference clock (if dual-port enabled, first X2 port)
E8	REFCLK-	Diff-Pair	Reference clock (if dual-port enabled, first X2 port)
E9	Ground	Ground	Ground
E10	PETp0	Diff-Pair	Transmitter differential pair, Lane 0
E11	PETn0	Diff-Pair	Transmitter differential pair, Lane 0

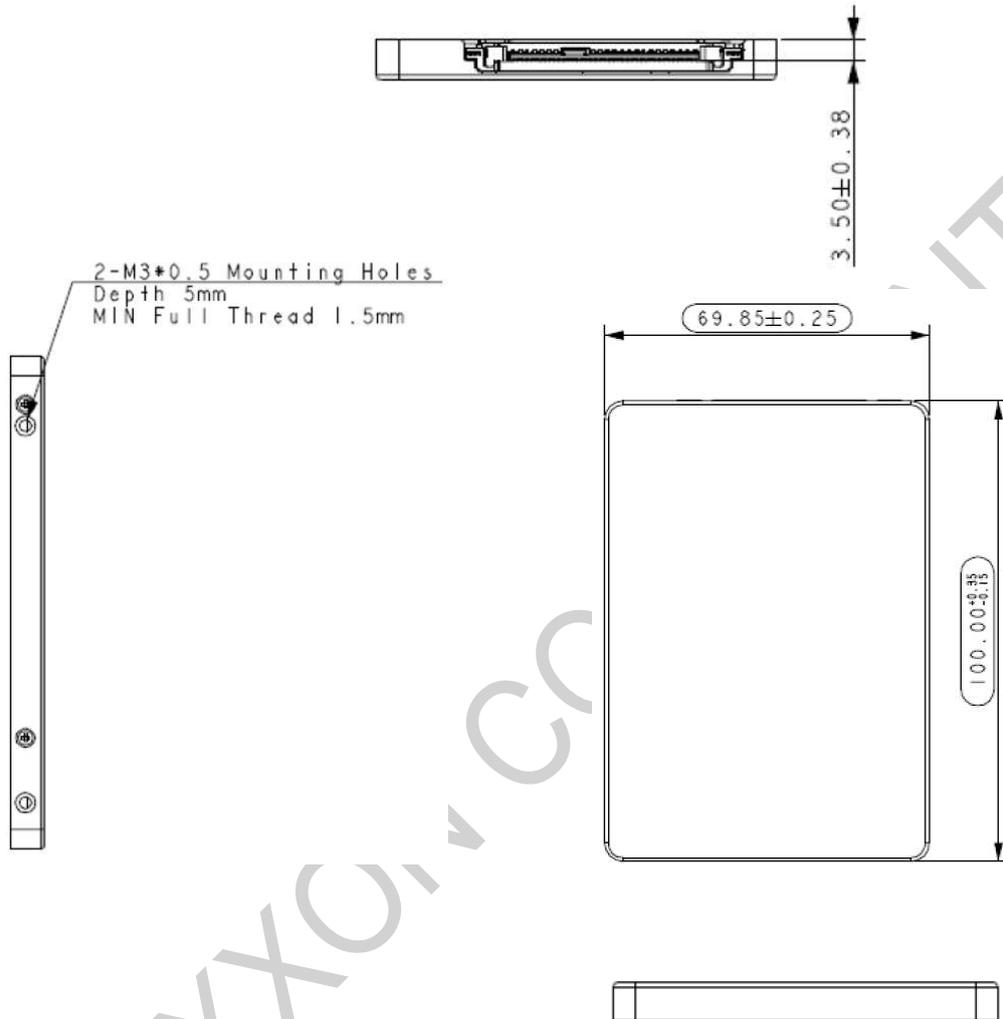
Pin Number	Name	Type	Description
E12	Ground	Ground	Ground
E13	PERn0	Diff-Pair	Receiver differential pair, Lane 0
E14	PERp0	Diff-Pair	Receiver differential pair, Lane 0
E15	Ground	Ground	Ground
E16	Reserved	-	Reserved
E17	PETp3	Diff-Pair	Transmitter differential pair, Lane 3
E18	PETn3	Diff-Pair	Transmitter differential pair, Lane 3
E19	Ground	Ground	Ground
E20	PERn3	Diff-Pair	Receiver differential pair, Lane 3
E21	PERp3	Diff-Pair	Receiver differential pair, Lane 3
E22	Ground	Ground	Ground
E23	SMCLK	Bi-Dir	SMBus (System Management Bus) clock
E24	SMDAT	Bi-Dir	SMBus (System Management Bus) data
E25	DualPortEn#	Output	Dual-port Enable

## 6. PHYSICAL DIMENSION

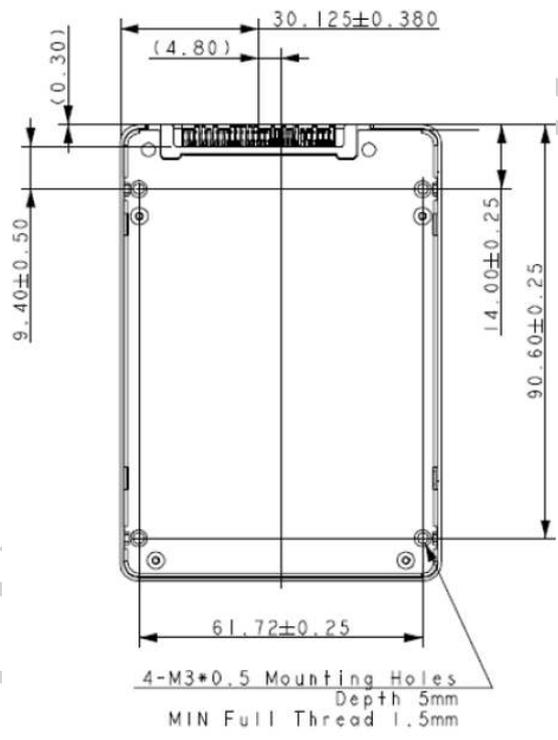
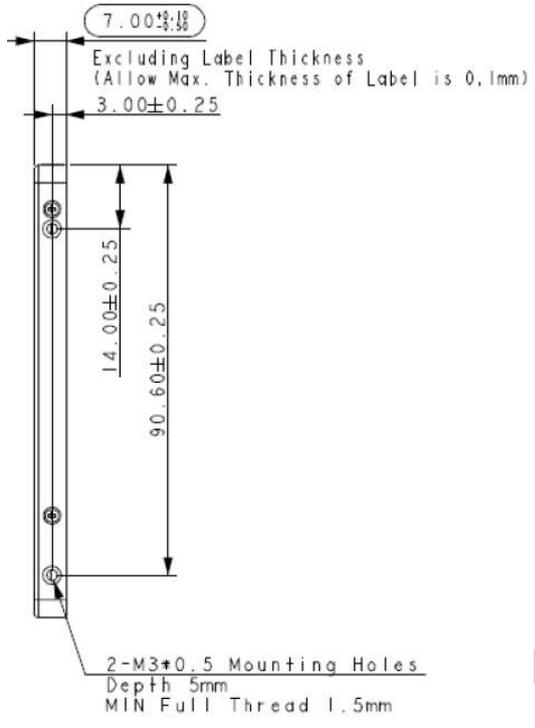


Dimension: 100.00mm(L) x 69.85mm(W) x 7.00mm(H)

Top View



Bottom / Side View



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## 7. ORDERING INFORMATION



### AES 256/TCG OPAL

Capacity	MPN (Silver)	MPN (Diamond)
240GB	FCCB240GBS-EC0S	FCCB240GBE-EC0S
480GB	FCCB480GBS-EC0S	FCCB480GBE-EC0S
960GB	FCCB960GBS-EC0S	FCCB960GBE-EC0S
1920GB	FCCB1920BS-EC0S	FCCB1920BE-EC0S
3480GB	FCCB3840BS-EC0S	FCCB3840BE-EC0S
7680GB	FCCB7680BS-EC0S	FCCB7680BE-EC0S *

### AES 256/TCG OPAL with conformal coating

Capacity	MPN (Silver)	MPN (Diamond)
240GB	FCCB240GBS-EC0V	FCCB240GBE-EC0V
480GB	FCCB480GBS-EC0V	FCCB480GBE-EC0V
960GB	FCCB960GBS-EC0V	FCCB960GBE-EC0V
1920GB	FCCB1920BS-EC0V	FCCB1920BE-EC0V
3480GB	FCCB3840BS-EC0V	FCCB3840BE-EC0V
7680GB	FCCB7680BS-EC0V	FCCB7680BE-EC0V*

### Power Loss Protection with AES 256/TCG OPAL

Capacity	MPN (Silver)	MPN (Diamond)
240GB	FCCB240GBS-EC0X	FCCB240GBE-EC0X
480GB	FCCB480GBS-EC0X	FCCB480GBE-EC0X
960GB	FCCB960GBS-EC0X	FCCB960GBE-EC0X
1920GB	FCCB1920BS-EC0X	FCCB1920BE-EC0X
3480GB	FCCB3840BS-EC0X	FCCB3840BE-EC0X
7680GB	FCCB7680BS-EC0X	FCCB7680BE-EC0X *

### AES 256/TCG OPAL, NSA-130 and Conformal coating

Capacity	MPN (Silver)	MPN (Diamond)
240GB	FCCB240GBS-EC0Z	FCCB240GBE-EC0Z
480GB	FCCB480GBS-EC0Z	FCCB480GBE-EC0Z
960GB	FCCB960GBS-EC0Z	FCCB960GBE-EC0Z
1920GB	FCCB1920BS-EC0Z	FCCB1920BE-EC0Z
3480GB	FCCB3840BS-EC0Z	FCCB3840BE-EC0Z
7680GB	FCCB7680BS-EC0Z	FCCB7680BE-EC0Z *

\* Please check with FLEXXON

## Revision History

Revision	Date	Description
1.0	2019/04	Preliminary release
1.1	2019/05	Update ordering number
1.2	2019/06	Update capacity
1.3	2019/10	Update ordering information
1.4	2020/03	Update performance
1.5	2020/05	Update ordering information
1.6	2020/06	Update performance

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