The Future of Analog IC Technology®

MPQ4425M

High Efficiency 1.5A, 36V, 2.2MHz Synchronous Step-Down LED Driver AEC-Q100 Qualified

DESCRIPTION

The MPQ4425M is a high-frequency, synchronous, rectified, step-down, switch-mode white LED driver with built-in power MOSFETs. It offers a very compact solution to achieve a 1.5A continuous output current with excellent load and line regulation over a wide input supply range. The MPQ4425M has synchronous mode operation to get high efficiency.

Current-mode operation provides fast transient response and eases loop stabilization.

Full protection features include over-current protection (OCP) and thermal shut down (TSD).

The MPQ4425M requires a minimal number of readily-available standard external components, and is available in a space-saving QFN-13 (2.5mmx3mm) package.

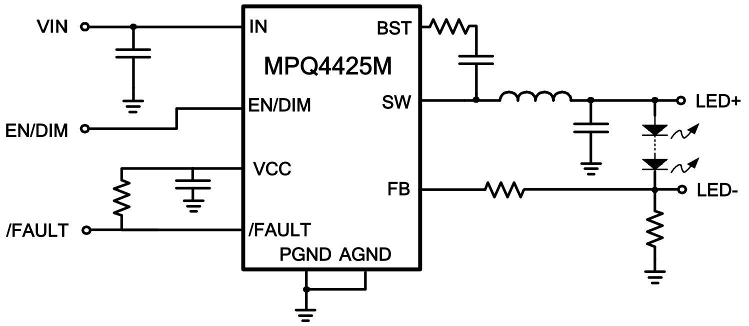
FEATURES

- EMI Reduction Technique
- Wide 4V-to-36V Operating Input Range
- 85mΩ/50mΩ Low $R_{DS(ON)}$ Internal Power MOSFETs
- High-Efficiency Synchronous Mode Operation
- Default 2.2MHz Switching Frequency
- PWM Dimming (Min 100Hz Dimming Frequency)
- Forced CCM Mode
- 0.2V Reference Voltage
- Internal Soft-Start
- Fault Indication for LED Short, Open and Thermal Shutdown
- Over-Current Protection (OCP) with Valley-Current Detection
- Thermal Shutdown
- Available in a QFN-13 (2.5mmx3mm) Package
- CISPR25 Class 5 Compliant
- Available in a Wettable Flank Package
- Available in AEC-Q100 Grade-1

APPLICATIONS

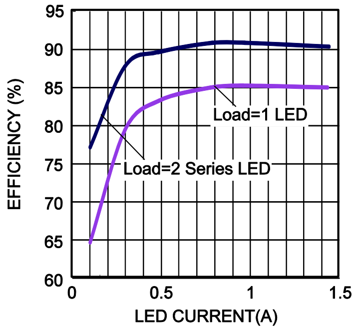
- Automotive LED Lighting

TYPICAL APPLICATION



Efficiency vs. LED Current

V_{IN}=12V



ORDERING INFORMATION

Part Number*	Package	Top Marking
MPQ4425MGQB	QFN-13 (2.5mmx3mm)	*See Below*
MPQ4425MGQB-AEC1		
MPQ4425MGQBE-AEC1**		*See Below*

* For Tape & Reel, add suffix –Z (e.g. MPQ4425MGQB–Z)

** Wettable Flank

TOP MARKING (MPQ4425MGQB & MPQ4425MGQB-AEC1)

ANP
YWW
LLL

ANP: product code;
Y: year code;
WW: week code:
LLL: lot number;

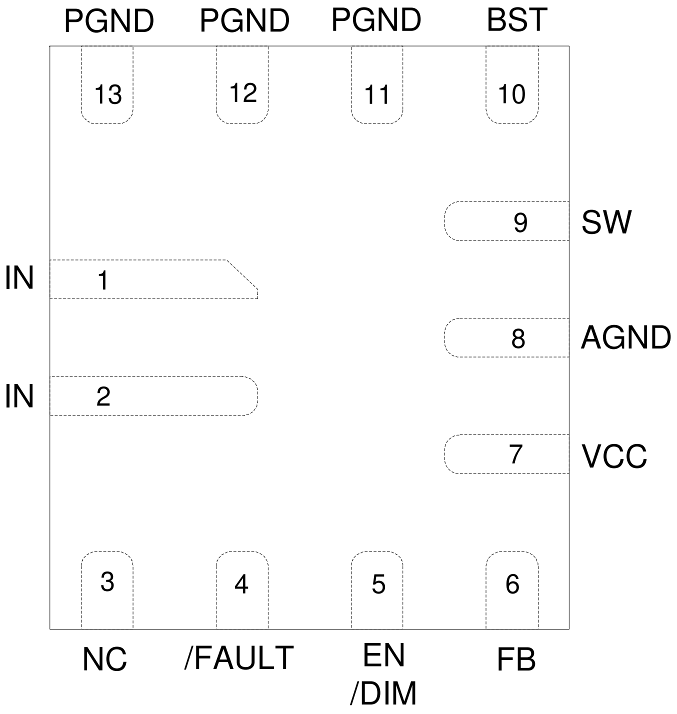
TOP MARKING (MPQ4425MGQBE-AEC1)

AXT
YWW
LLL

AXT: product code;
Y: year code;
WW: week code:
LLL: lot number;

PACKAGE REFERENCE

TOP VIEW



QFN-13 (2.5mmx3mm)

ABSOLUTE MAXIMUM RATINGS [1]

Supply voltage (V_{IN})	-0.3V to 40V
Switch voltage (V_{SW})	-0.3V to V_{IN} + 0.3V
BST voltage (V_{BST})	V_{SW}+6V
All other pins	-0.3V to 6V [2]
Continuous power dissipation (T_A = +25°C) [3]	
QFN-13 (2.5mmx3mm)	2.08W
Junction temperature	150°C
Lead temperature	260°C
Storage temperature	-65°C to 150°C

Recommended Operating Conditions

Supply voltage (V_{IN})	4V to 36V
LED current (I_{LED})	Up to 1.5A
Operating junction temp. (T_J)	-40°C to +125°C

Thermal Resistance [4]	θ_{JA}	θ_{JC}	
QFN-13 (2.5mmx3mm)	60	13	°C/W

Notes:

1) Absolute maximum ratings are rated under room temperature unless otherwise noted. Exceeding these ratings may damage the device.
2) About the details of EN/DIM pin's ABS MAX rating, please refer to page 14, Enable control section.
3) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX)-T_A)/θ_{JA}. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
4) Measured on JESD51-7, 4-layer PCB.

ELECTRICAL CHARACTERISTICS

V_{IN} = 12V, V_{EN} = 2V, T_J=-40°C to +125°C, unless otherwise noted, typical values are at T_J=+25°C

Parameter	Symbol	Condition	Min	Typ	Max	Units
Supply current (shutdown)	I_{IN}	V_{EN} = 0V		12		μA
Supply current (quiescent)	I_Q	V_{EN} = 2V, V_{FB} = 1V, no switching		0.6	0.8	mA
HS switch-on resistance	HS_{RDS-ON}	V_{BST-SW}=5V		85	150	mΩ
LS switch-on resistance	LS_{RDS-ON}	V_{CC} =5V		50	105	mΩ
Switch leakage	SW_{LKG}	V_{EN} = 0V, V_{SW} =12V			1	μA
Current limit (5)	I_{LIMIT}	Under 40% Duty Cycle	2.5	4	5.5	A
Reverse current limit				1.2		A
Oscillator frequency	f_{SW}	V_{FB}=100mV	1800	2200	2600	kHz
Maximum duty cycle	D_{MAX}	V_{FB}=100mV	80	87		%
Minimum on time(5)	τ_{ON_MIN}			46		ns
Feedback voltage	V_{FB}	T_J=+25°C	192	200	208	mV
		T_J=-40°C to +125°C	184	200	216	
Feedback current	I_{FB}	V_{FB}=250mV		30	100	nA
EN rising threshold	V_{EN_RISING}		1.1	1.45	1.8	V
EN falling threshold	$V_{EN\_FALLING}$		0.7	1	1.3	V
EN threshold hysteresis	V_{EN_HYS}			450		mV
EN input current	I_{EN}	V_{EN}=2V		5	10	μA
		V_{EN}=0		0	0.2	μA
EN turn-off delay	EN_{td-off}		10	25	50	ms
VIN under-voltage lockout threshold-rising	$INUV_{Vth}$		3.2	3.5	3.8	V
VIN under-voltage lockout threshold-falling			2.8	3.1	3.5	V
VIN under-voltage lockout threshold-hysteresis	$INUV_{HYS}$			400		mV
Over voltage detection (/FAULT pulled low)	FT_{Vth-Hi}			140%		V_{FB}
Over voltage detection hysteresis				20%		V_{FB}
/FAULT delay	FT_{Td}			10		μs
/FAULT sink current capability	V_{FT}	Sink 4mA			0.4	V
/FAULT leakage current	$I_{FT-LEAK}$				100	nA
VCC regulator	V_{CC}	I_{CC}=0mA	4.6	4.9	5.2	V
VCC load regulation		I_{CC}=5mA		1.5	4	%
Soft-start time(5)	t_{SS}	I_{LED}=1.5A, L=2.2uH, load=2 series LED, I_{LED} from 10% to 90%		0.9		ms
Thermal shutdown(5)			150	170		°C
Thermal hysteresis(5)				30		°C

Note:

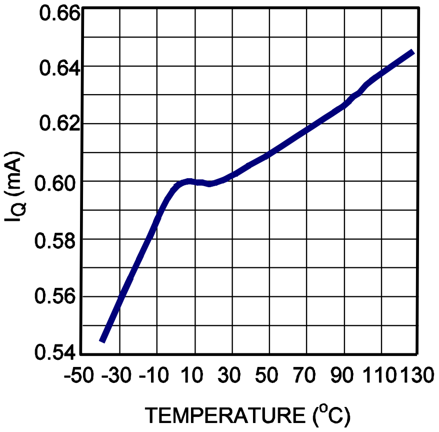
5) Derived from bench characterization. Not tested in production

PIN FUNCTIONS

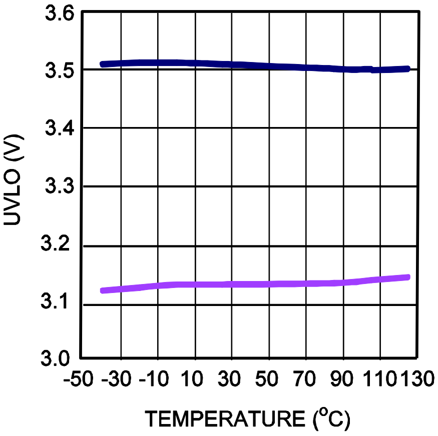
Package Pin #	Name	Description
1, 2	IN	**Supply Voltage.** The MPQ4425M operates from a 4V to 36V input rail. Requires C_{IN} to decouple the input rail. Connect using a wide PCB trace.
3	NC	**Do not connect.**
4	/FAULT	**Fault indicator.** Open Drain output, pulled to low when LED short, open or thermal shutdown happening.
5	EN/DIM	**Enable/Dimming Control.** Pull EN high to enable the MPQ4425M. Apply a 100Hz to 2kHz external clock to the EN/DIM pin for the PWM dimming.
6	FB	**LED Current Feedback Input.**
7	VCC	**Internal bias Supply.** Decouple VCC with a 0.1µF-to-0.22µF capacitor. The capacitance should be no more than 0.22µF.
8	AGND	**Analog ground.** Reference ground of the logic circuit. AGND is connected to PGND internally. There is no need to add external connections to PGND.
9	SW	**Switch Output.** Connect using a wide PCB trace.
10	BST	**Bootstrap.** Requires a capacitor connected between SW and BST pins to form a floating supply across the high-side switch driver. A 20Ω resistor placed between SW and BST cap is strongly recommended to reduce SW spike voltage.
11, 12, 13	PGND	**Power Ground.** PGND is the reference ground of the power device and requires careful consideration during PCB layout. For best results, connect PGND with copper pours and vias.

TYPICAL CHARACTERISTICS

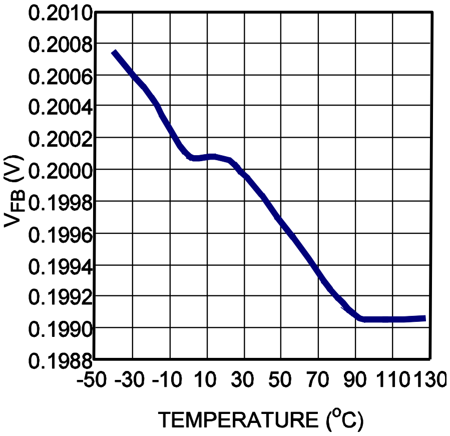
I_Q vs. Temperature



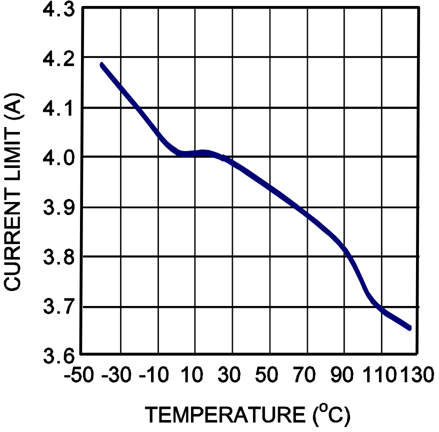
V_{IN} UVLO vs.Temperature



V_{FB} vs. Temperature



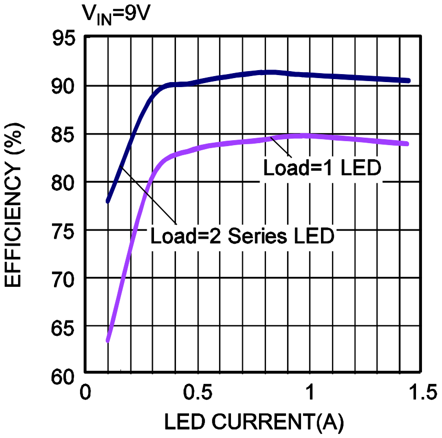
Current Limit vs. Temperature



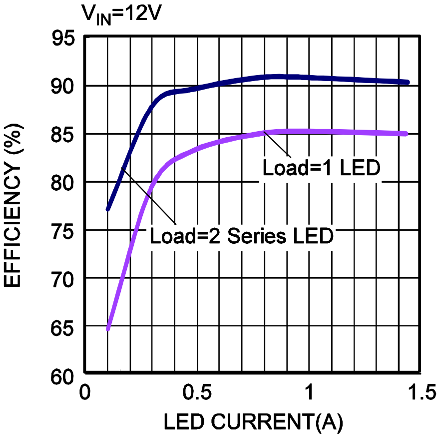
TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 12V, LOAD=2 series LED, L=2.2µH, F_{SW}=2.2MHz, T_A = +25°C, unless otherwise noted.

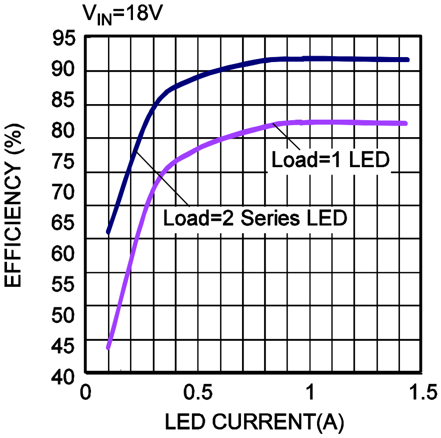
Efficiency vs. LED Current



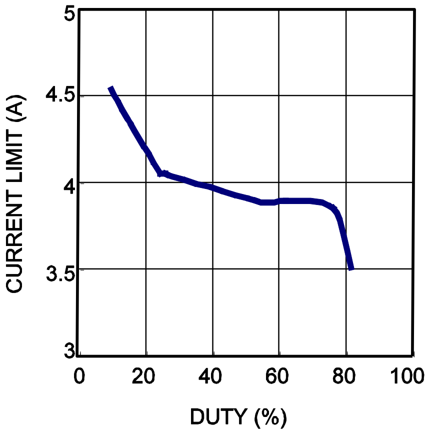
Efficiency vs. LED Current



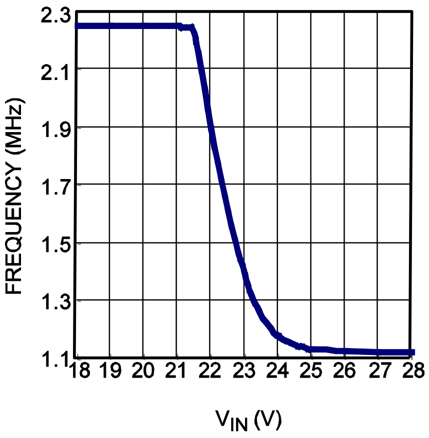
Efficiency vs. LED Current



Current Limit vs.Duty



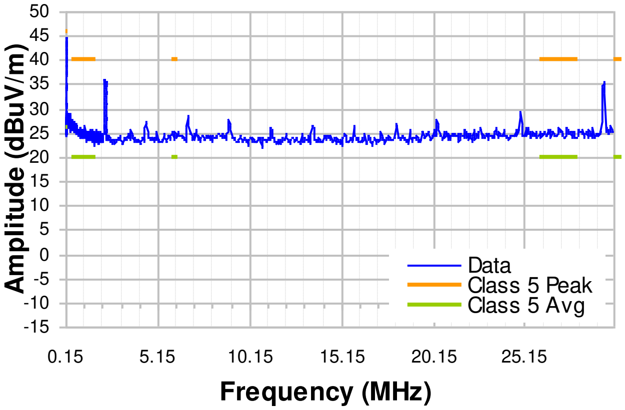
Frequency vs. V_{IN}



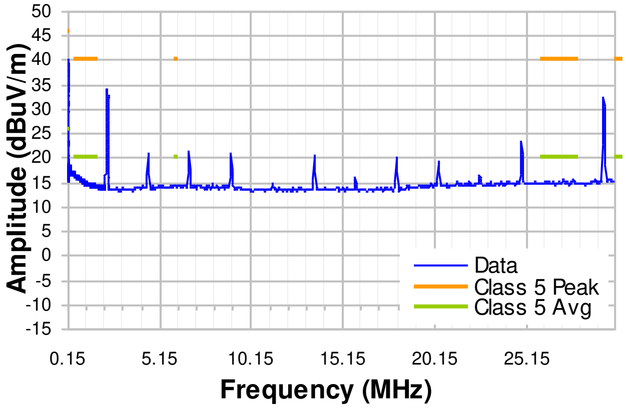
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, LOAD=2 series LED, I_{LED}=1.5A, L=2.2µH, F_{SW}=2.2MHz, with EMI filters, T_A = +25°C, unless otherwise noted. [(6)]

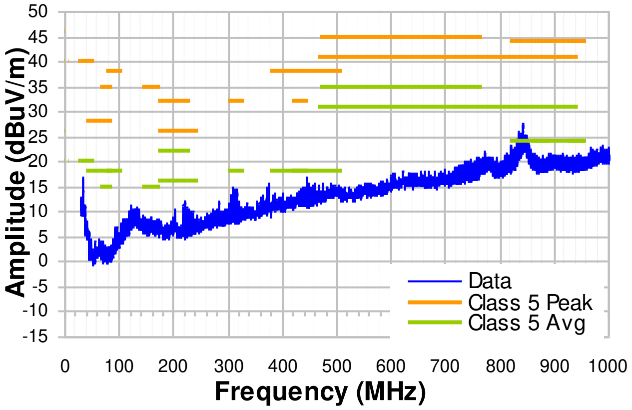
CISPR25 Class 5 Peak Radiated Emissions (150kHz-30MHz)



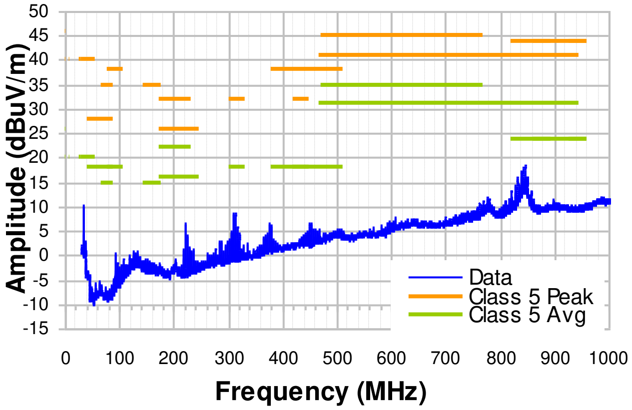
CISPR25 Class 5 Average Radiated Emissions (150kHz-30MHz)



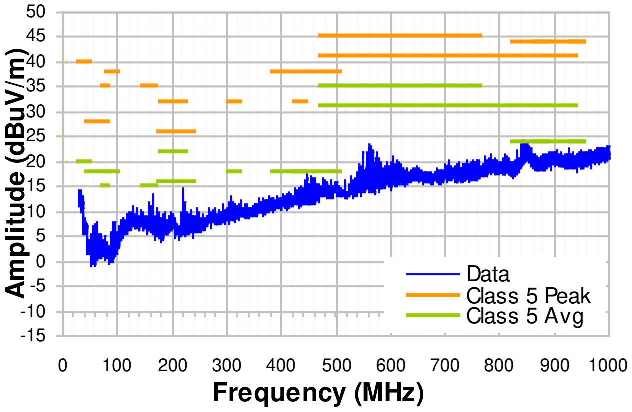
CISPR25 Class 5 Peak Radiated Emissions (Vertical, 30MHz-1GHz)



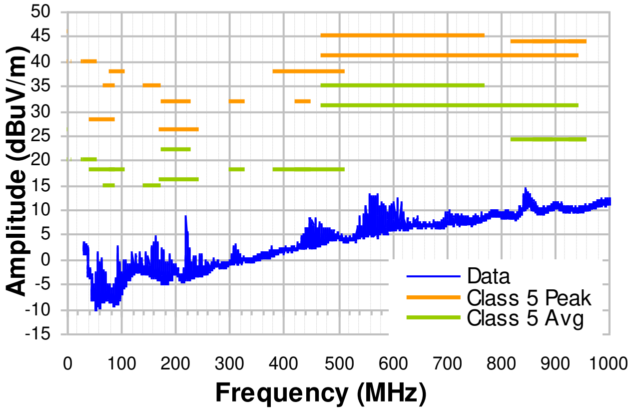
CISPR25 Class 5 Average Radiated Emissions (Vertical, 30MHz-1GHz)



CISPR25 Class 5 Peak Radiated Emissions (Horizontal, 30MHz-1GHz)



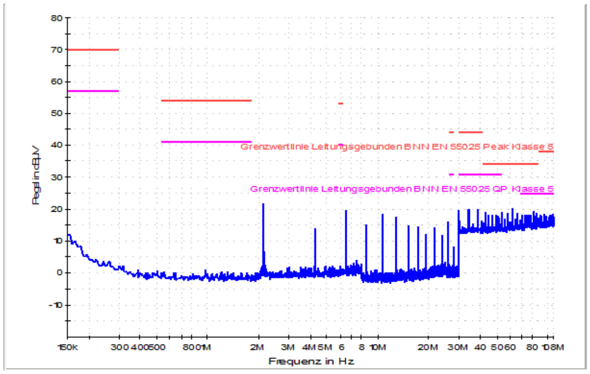
CISPR25 Class 5 Average Radiated Emissions (Horizontal, 30MHz-1GHz)



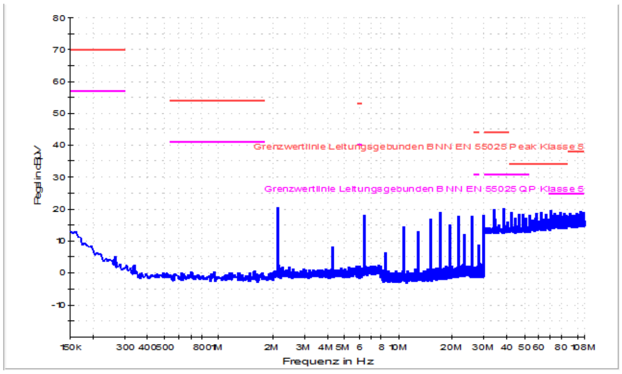
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, LOAD=2 series LED, I_{LED}=1.5A, L=2.2µH, F_{SW}=2.2MHz, with EMI filters, T_A = +25°C, unless otherwise noted. (6)

CISPR25 Class5 Peak Conducted Emissions (150kHz-108MHz)



CISPR25 Class5 Average Conducted Emissions (150kHz-108MHz)



Note:

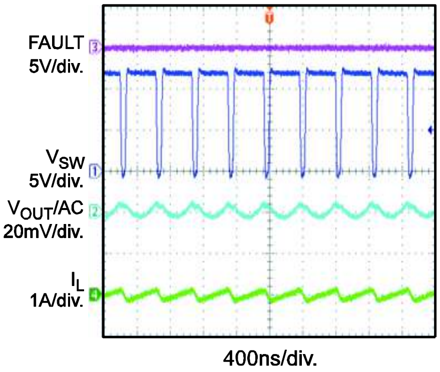
6) The EMC test results are based on application circuit with EMI filters as shown in Figure 9.

TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, LOAD=2 series LED, L=2.2µH, F_{SW}=2.2MHz, T_A = +25°C, unless otherwise noted.

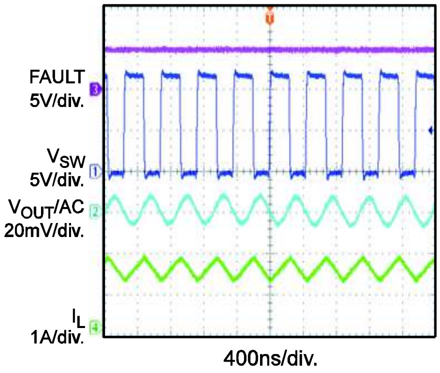
Steady State

I_{LED} = 0A



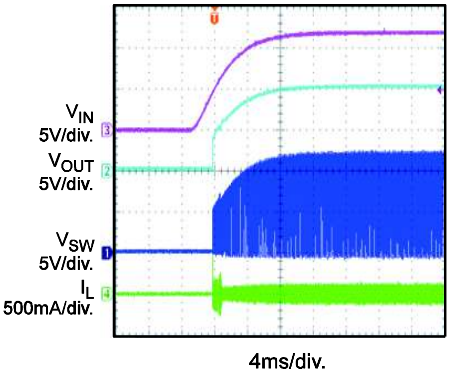
Steady State

I_{LED} = 1.5A



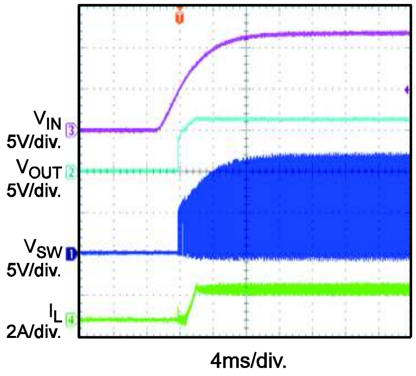
Start-Up through V_{IN}

I_{LED} = 0A



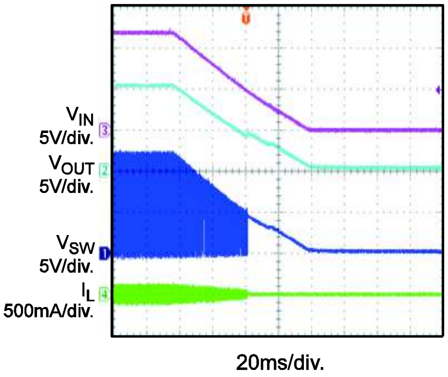
Start-Up through V_{IN}

I_{LED} = 1.5A



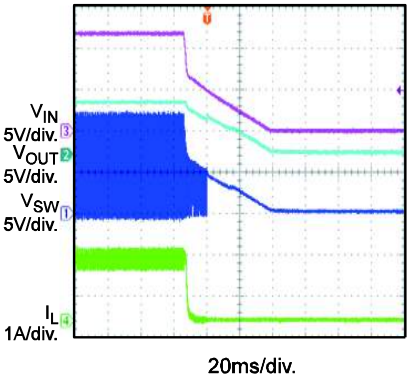
Shutdown through V_{IN}

I_{LED} = 0A



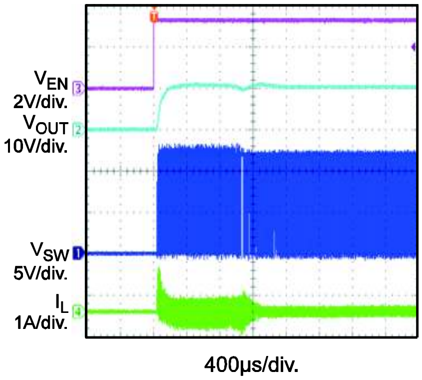
Shutdown through V_{IN}

I_{LED} = 1.5A



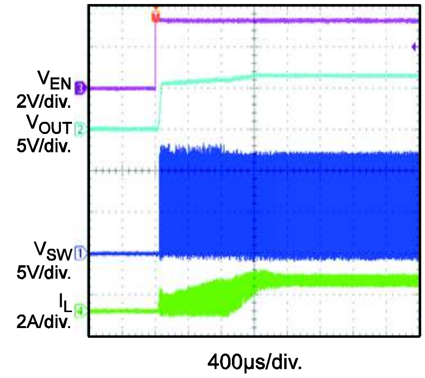
Start-Up through EN

I_{LED} = 0A



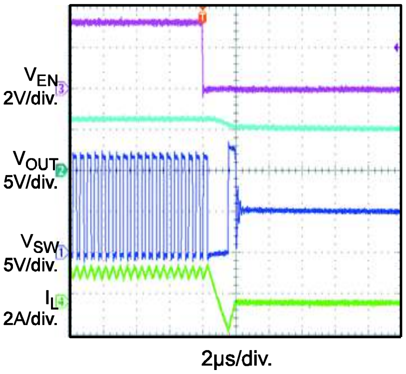
Start-Up through EN

I_{LED} = 1.5A



Shutdown through EN

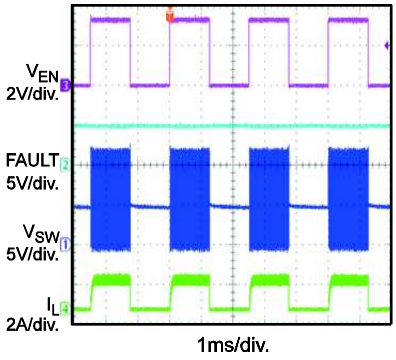
I_{LED} = 1.5A



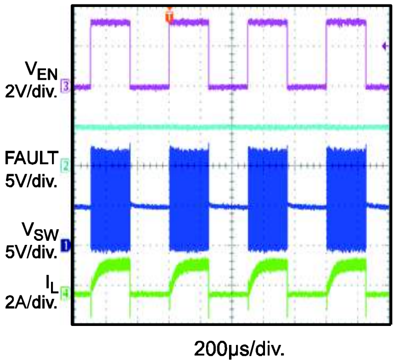
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, LOAD=2 series LED, L=2.2µH, F_{SW}=2.2MHz, T_A = +25°C, unless otherwise noted.

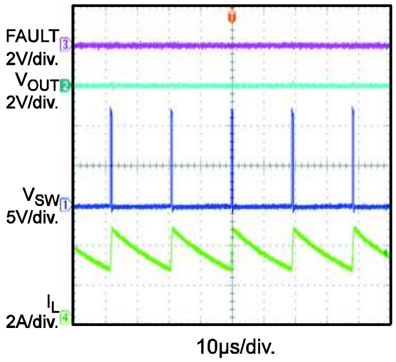
PWM Dimming
400Hz



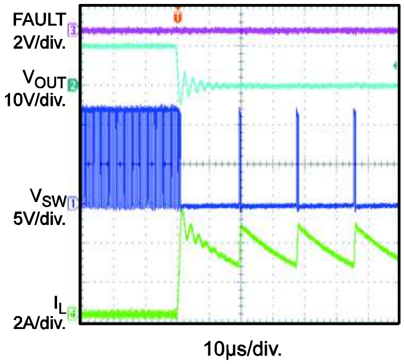
PWM Dimming
2kHz



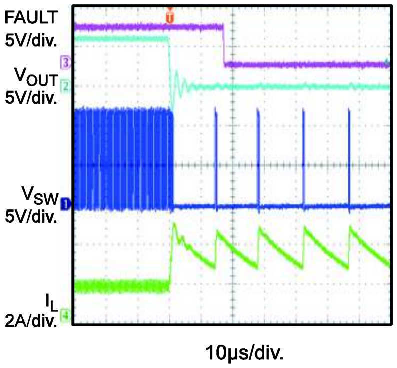
LED+ Short to GND Steady State



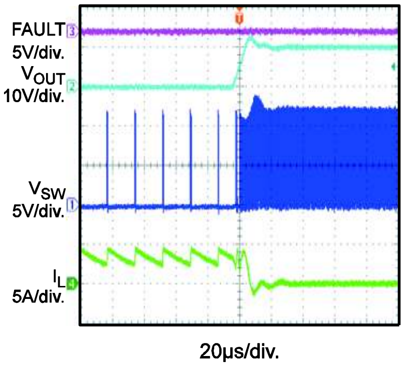
LED+ Short to GND Entry
I_{LED} = 0A



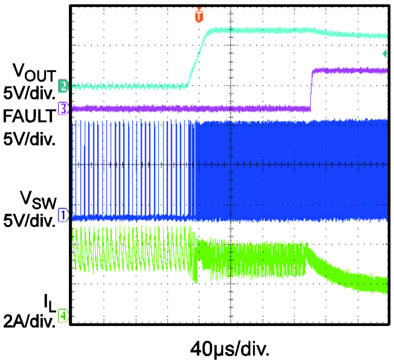
LED+ Short to GND Entry
I_{LED} = 1.5A



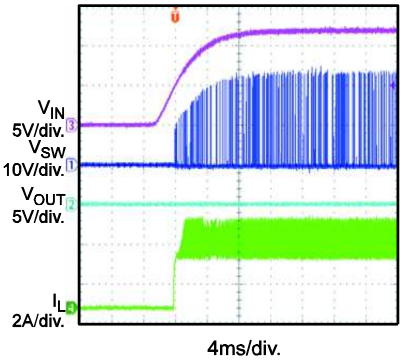
LED+ Short to GND Recovery
I_{LED} = 0A



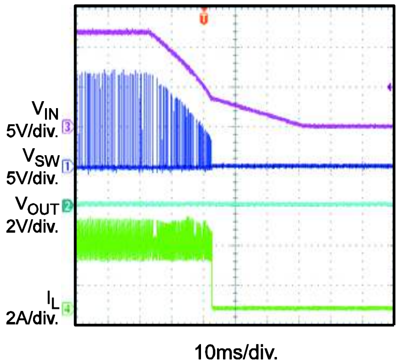
LED+ Short to GND Recovery
I_{LED} = 1.5A



LED+ Short to GND Input Power On



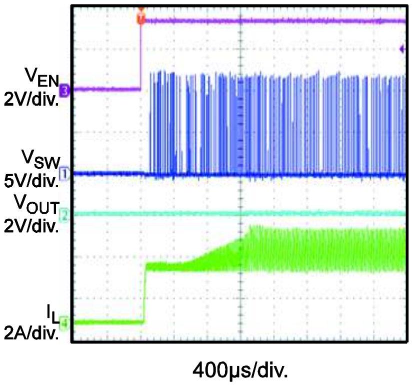
LED+ Short to GND Input Power Off



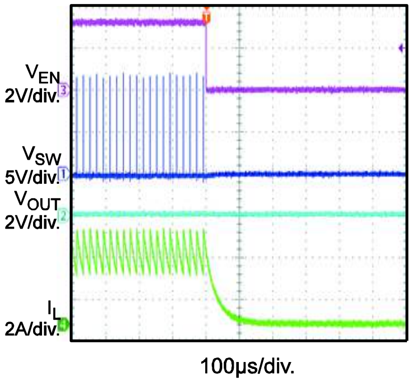
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, LOAD=2 series LED, L=2.2µH, F_{SW}=2.2MHz, T_A = +25°C, unless otherwise noted.

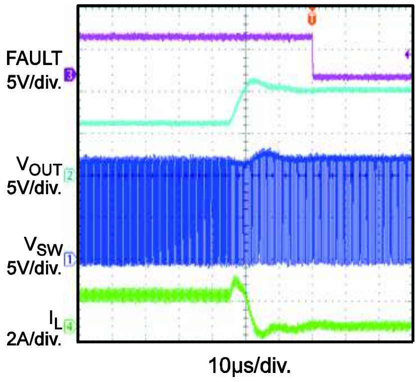
LED+ Short to GND EN On



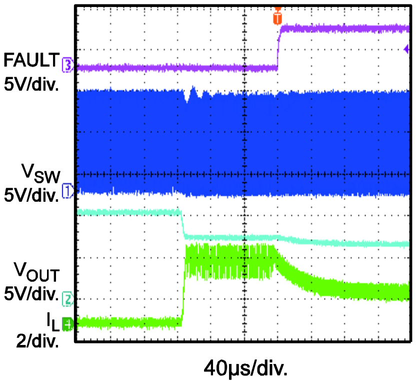
LED+ Short to GND EN Off



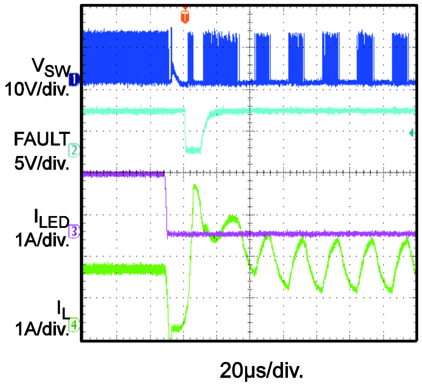
LED Open Entry



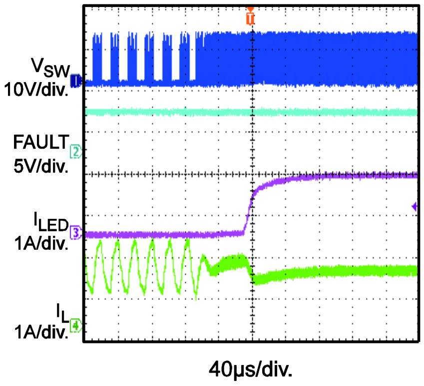
LED Open Recovery



LED+ and LED- Short Entry



LED+ and LED- Short Recovery



BLOCK DIAGRAM

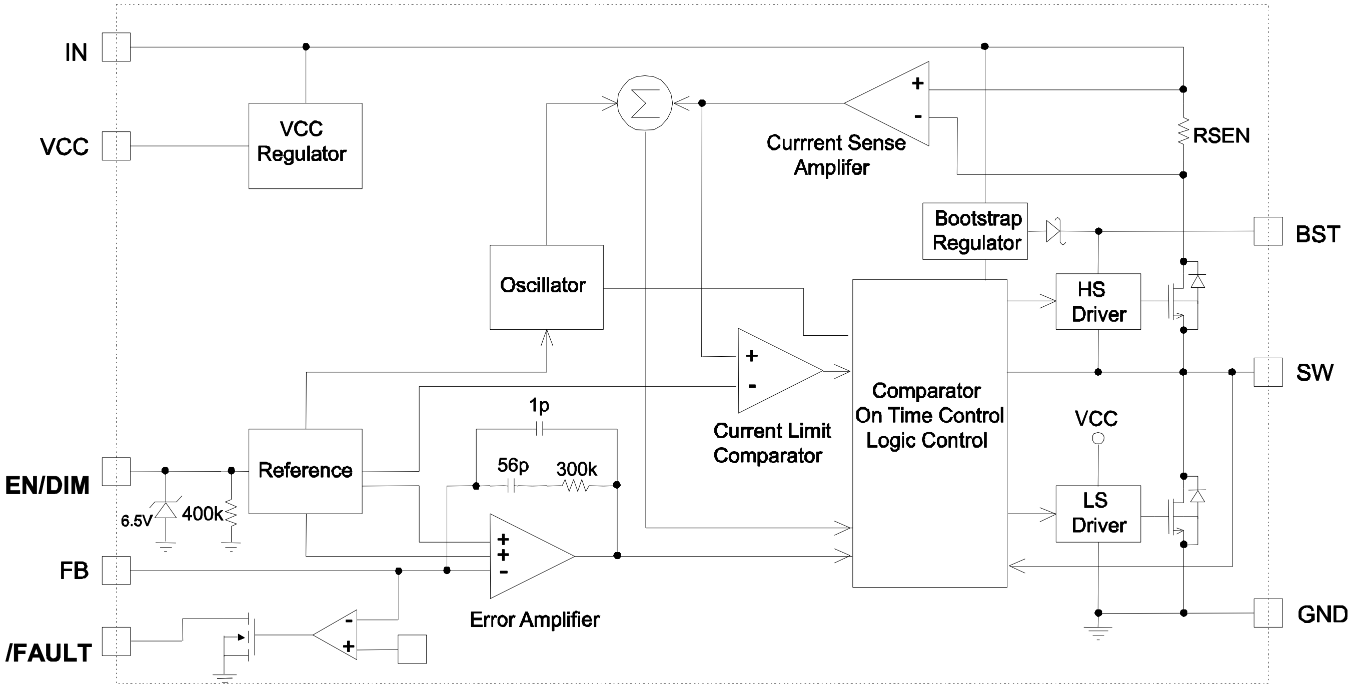


Figure 1: Functional Block Diagram

OPERATION

The MPQ4425M is a high-frequency, synchronous rectified, step-down, switch-mode white LED driver with built-in power MOSFETs. It offers a very compact solution to achieve 1.5A continuous output current with excellent load and line regulation over a 4V to 36V input supply range.

The MPQ4425M operates in a fixed-frequency, peak-current–control mode to regulate the output current. An internal clock initiates a PWM cycle. The integrated high-side power MOSFET turns on and remains on until its current reaches the value set by the COMP voltage (V_{COMP}). When the power switch is off, it remains off until the next clock cycle starts. If the current in the power MOSFET does not reach the current value set by V_{COMP} within 87% of one PWM period, the power MOSFET is forced off.

Internal Regulator

The 4.9V internal regulator power most of the internal circuitries. This regulator takes the V_{IN} input and operates in the full V_{IN} range: When V_{IN} exceeds 4.9V, the output of the regulator is in full regulation; when V_{IN} falls below 4.9V, the output decreases following V_{IN}. A 0.1uF decoupling ceramic capacitor is needed at the pin.

CCM Operation

The MPQ4425M uses continuous conduction modulation (CCM) mode to ensure that the part works with fixed frequency from a no-load to a full-load range. The advantage of CCM is the controllable frequency and lower output ripple at light load.

Frequency Foldback

The MPQ4425M enters frequency foldback when the input voltage is higher than about 21V. The frequency decreases to half the nominal value and changes to 1.1MHz.

Frequency foldback also occurs during soft start and short-circuit protection.

Error Amplifier (EA)

The error amplifier compares the FB pin voltage to the internal 0.2V reference (V_{REF}) and outputs a current proportional to the difference between the two. This output current then charges or discharges the internal compensation network to form V_{COMP}, which controls the power MOSFET current. The optimized internal compensation network minimizes the external component counts and simplifies the control loop design.

Enable Control (EN)

EN/DIM is a control pin that turns the regulator on and off. Drive EN/DIM high to turn on the regulator, and drive it low to turn it off. An internal resistor from EN/DIM to GND allows EN/DIM to be floated to shut down the chip.

EN/DIM is clamped internally using a 6.5V series Zener diode (see Figure 2). Connecting the EN/DIM input through a pull-up resistor to the voltage on V_{IN} limits the EN input current to less than 100µA.

For example, with 12V connected to V_{IN}, $R_{PULLUP} \geq (12V - 6.5V) \div 100\mu A = 55k\Omega$.

Connecting EN/DIM to a voltage source directly without a pull-up resistor requires limiting the amplitude of the voltage source to ≤6V to prevent damage to the Zener diode.

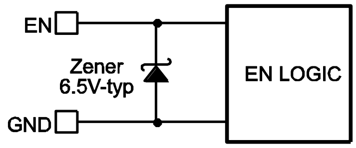


Figure 2: 6.5V Zener Diode Connection

Drive EN/DIM low longer than 25ms will shutdown the IC.

PWM Dimming

Apply an external 100Hz to 2kHz PWM waveform to the EN/DIM pin for PWM dimming. The average LED current is proportional to PWM duty. The minimum amplitude of the PWM signal is 1.8V. If dimming signal is applied before the chip starts up, the on time of dimming signal must be longer than 2ms to make sure the soft start is finished, so output current can be built. If dimming signal is applied after soft start is finished, the above 2ms limit is not required.

Under-Voltage Lockout (UVLO)

Under-voltage lockout (UVLO) protects the chip from operating at an insufficient supply voltage.The UVLO comparator monitors the output voltage of the internal regulator (VCC).

Internal Soft Start (SS)

The soft start (SS) prevents the converter output voltage from overshooting during start-up. When the chip starts up, the internal circuitry generates a soft start voltage (V_{SS}). When V_{SS} is lower than the internal reference (V_{REF}), V_{SS} overrides V_{REF}, so the error amplifier uses V_{SS} as the reference. When V_{SS} exceeds V_{REF}, the error amplifier uses V_{REF} as the reference.

Fault Indicator

The MPQ4425M has fault indication. The /FAULT pin is the open drain of a MOSFET. It should be connected to VCC or some other voltage source through a resistor (e.g. 100kΩ). /FAULT pin is pulled high at normal operation, and LED short, open or thermal shutdown will pulled down this pin to indicate a fault status.

Over-Current Protection (OCP)

The MPQ4425M has cycle-by-cycle peak current-limit protection with valley-current detection. The inductor current is monitored during the high-side MOSFET (HS-FET) on-state. If the inductor current exceeds the current-limit value set by the COMP high-clamp voltage, the HS-FET turns off immediately. Then the low-side MOSFET (LS-FET) turns on to discharge the energy, and the inductor current decreases. The HS-FET remains off unless the inductor valley current is lower than a certain current threshold (the valley current limit), even though the internal clock pulses high. If the inductor current does not drop below the valley current limit when the internal clock pulses high, the HS-FET misses the clock, and the switching frequency decreases to half the nominal value. Both the peak and valley current limits assist in keeping the inductor current from running away during an overload or short-circuit condition.

Thermal Shutdown (TSD)

Thermal shutdown prevents the chip from operating at exceedingly high temperatures. When the die temperature exceeds 170°C, the entire chip shuts down. When the temperature drops below its lower threshold (typically 140°C), the chip is enabled again.

Floating Driver and Bootstrap Charging

An external bootstrap capacitor powers the floating power MOSFET driver. This floating driver has its own UVLO protection, with a rising threshold of 2.2V and hysteresis of 150mV. The bootstrap capacitor voltage is regulated internally by V_{IN} through D1, M1, C3, L1 and C4 (see Figure 3). If (V_{IN} - V_{SW}) exceeds 5V, U1 regulates M1 to maintain a 5V BST voltage across C4. As long as V_{IN} is sufficiently higher than SW, the bootstrap capacitor can be charged. When the HS-FET is on, $V_{IN} \approx V_{SW}$, so the bootstrap capacitor cannot be charged. When the LS-FET is on, V_{IN} - V_{SW} reaches its maximum for fast charging. When there is no inductor current, $V_{SW} = V_{OUT}$, so the difference between V_{IN} and V_{OUT} can charge the bootstrap capacitor. A 20Ω resistor placed between SW and BST cap is strongly recommended to reduce SW spike voltage.

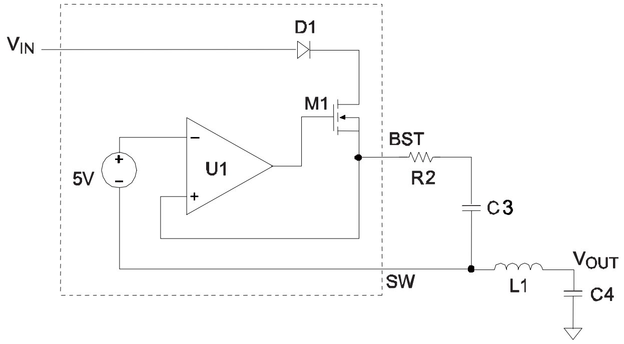


Figure 3: Internal Bootstrap Charging Circuit

Start-up and Shutdown

If both V_{IN} and EN exceed their appropriate thresholds, the chip starts up. The reference block starts first, generating stable reference voltage and currents, and then the internal regulator is enabled. The regulator provides a stable supply for the remaining circuitries.

Three events can shut down the chip: V_{IN} low, EN low, and thermal shutdown. During the shutdown procedure, the signaling path is first blocked to avoid any fault triggering. V_{COMP} and the internal supply rail are then pulled down. The floating driver is not subject to this shutdown command.

APPLICATION INFORMATION

Setting the Output Current

The output current is set by the external resistor R_{FB} (see Figure 4). Feedback reference voltage is 0.2V, I_{LED} is then given by Equation (1):

$$I_{LED} = \frac{0.2V}{R_{FB}} \tag{1}$$

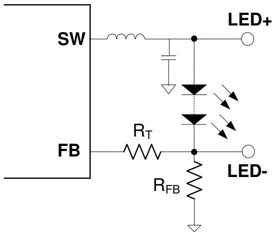


Figure 4: Feedback Network

R_T is used to set the loop bandwidth. Basically, lower R_T, higher bandwidth. But high bandwidth may cause insufficient phase margin, resulting in loop unstable. So a proper value of R_T is needed to make a trade-off between bandwidth and phase margin. Table 1 lists the recommended feedback resistor and R_T values for common output with 1 or 2 series LED.

Table 1: Resistor Selection for Common Output

I_{LED} (A)	R_{FB} (mΩ)	R_T (kΩ)
0.5	400(1%)	200 (1%)
1	200(1%)	150 (1%)
1.5	133(1%)	100 (1%)

Selecting the Input Capacitor

The input current to the step-down converter is discontinuous, therefore it requires a capacitor to supply the AC current to the converter while maintaining the DC input voltage. For the best performance, use low ESR capacitors. Ceramic capacitors with X5R or X7R dielectrics are highly recommended because of their low ESR and small temperature coefficients.

For most application, use a 4.7µF to 10µF capacitor. And it is strongly recommended to use another lower value capacitor (e.g. 0.1µF) with small package size (0603) to absorb high frequency switching noise. Make sure place the small size capacitor as close to IN and GND pins as possible.

Since C_{IN} absorbs the input switching current, it requires an adequate ripple current rating. The RMS current in the input capacitor can be estimated with Equation (2):

$$I_{CIN} = I_{LED} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times (1 - \frac{V_{OUT}}{V_{IN}})} \tag{2}$$

The worst case condition occurs at $V_{IN} = 2V_{OUT}$, shown in Equation (3):

$$I_{CIN} = \frac{I_{LED}}{2} \tag{3}$$

For simplification, choose an input capacitor with an RMS current rating greater than half of the maximum load current.

The input capacitor can be electrolytic, tantalum, or ceramic. When using electrolytic or tantalum capacitors, add a small, high-quality ceramic capacitor (e.g. 0.1μF) as close to the IC as possible. When using ceramic capacitors, ensure that they have enough capacitance to provide a sufficient charge to prevent excessive voltage ripple at input. The input voltage ripple caused by capacitance can be estimated with Equation (4):

$$\Delta V_{IN} = \frac{I_{LED}}{f_{SW} \times C_{IN}} \times \frac{V_{OUT}}{V_{IN}} \times (1 - \frac{V_{OUT}}{V_{IN}}) \tag{4}$$

Selecting the Output Capacitor

The output capacitor maintains the DC output voltage. Use ceramic, tantalum, or low-ESR electrolytic capacitors. For best results, use low ESR capacitors to keep the output voltage ripple low. The output voltage ripple can be estimated with Equation (5):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L} \cdot (1 - \frac{V_{OUT}}{V_{IN}}) \cdot (R_{ESR} + \frac{1}{8 f_{SW} \times C_{OUT}}) \tag{5}$$

Where L is the inductor value and R_{ESR} is the equivalent series resistance (ESR) value of the output capacitor.

For ceramic capacitors, the capacitance dominates the impedance at the switching frequency, and the capacitance causes the majority of the output voltage ripple. For simplification, the output voltage ripple can be estimated with Equation (6):

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times f_{SW}{}^{2} \times L \times C_{OUT}} \times (1 - \frac{V_{OUT}}{V_{IN}}) \qquad (6)$$

For tantalum or electrolytic capacitors, the ESR dominates the impedance at the switching frequency. For simplification, the output ripple can be approximated with Equation (7):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \times R_{ESR} \qquad (7)$$

The characteristics of the output capacitor also affect the stability of the regulation system. The MPQ4425M can be optimized for a wide range of capacitance and ESR values.

Selecting the Inductor

A 1µH to 10µH inductor with a DC current rating at least 25% higher than the maximum load current is recommended for most applications. For higher efficiency, choose an inductor with lower DC resistance. A larger value inductor results in less ripple current and a lower output ripple voltage. However, the larger value inductor also has a larger physical size, higher series resistance, and lower saturation current. A good rule for determining the inductor value is to allow the inductor ripple current to be approximately 30% of the maximum load current. The inductance value can be then be calculated with Equation (8):

$$L = \frac{V_{OUT}}{f_{SW} \times \Delta I_{L}} \times (1 - \frac{V_{OUT}}{V_{IN}}) \qquad (8)$$

Where ΔI_{L} is the peak-to-peak inductor ripple current.

Choose the inductor ripple current to be approximately 30% of the maximum load current. The maximum inductor peak current can be calculated with Equation (9):

$$I_{LP} = I_{LED} + \frac{V_{OUT}}{2f_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \qquad (9)$$

V_{IN} UVLO Setting

MPQ4425M has internal fixed under-voltage lockout (UVLO) threshold: rising threshold is 3.5V while falling threshold is about 3.1V. For the application needs higher UVLO point, external resistor divider between IN and EN/DIM pins can be used to get higher equivalent UVLO threshold (see Figure 5).

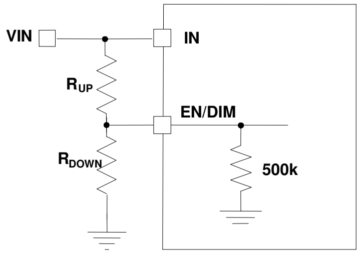


Figure 5: Adjustable UVLO using EN divider

The UVLO threshold can be computed with Equation (10) and Equation (11):

$$INUV_{RISING} = (1 + \frac{R_{UP}}{500k//R_{DOWN}}) \times V_{EN\_RISING} \qquad (10)$$

$$INUV_{FALLING} = (1 + \frac{R_{UP}}{500k//R_{DOWN}}) \times V_{EN\_FALLING} \qquad (11)$$

Where V_{EN_RISING}=1.45V, $V_{EN\_FALLING}$=1V.

When choosing R_{UP}, make sure it is big enough to limit the current flows into EN/DIM pin lower than 100uA.

BST Resistor and External BST Diode

A 20ohm resistor in series with BST capacitor is recommended to reduce the SW spike voltage. Higher resistance is better for SW spike reduction, but will compromise the efficiency on the other hand.

An external BST diode can enhance the efficiency of the regulator when the duty cycle is high (>65%). A power supply between 2.5V and 5V can be used to power the external bootstrap diode and VCC or V_{OUT} is the good choice of this power supply in the circuit (see Figure 6).

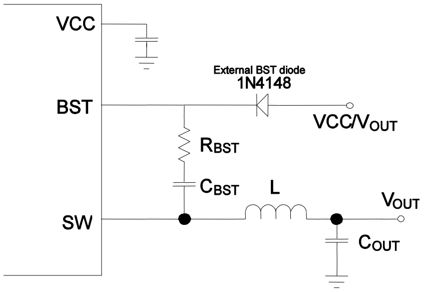


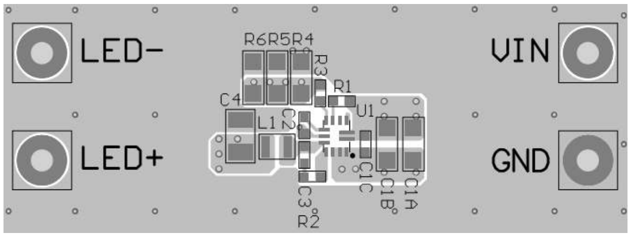
Figure 6: Optional External Bootstrap Diode to Enhance Efficiency

The recommended external BST diode is IN4148, and the BST capacitor value is 0.1µF to 1µF.

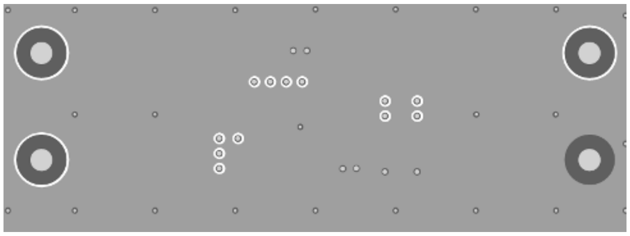
PCB Layout Guidelines

Efficient PCB layout is critical for stable operation, especially for input capacitor placement. For best results, refer to Figure 7 and follow the guidelines below: (7)

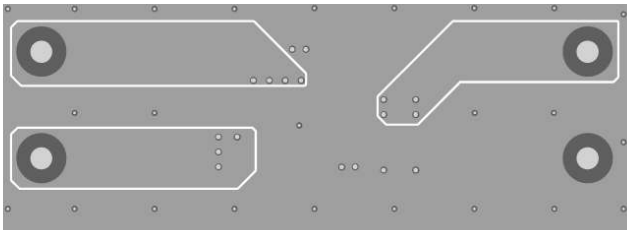
1. Use a large ground plane to connect directly to PGND. If the bottom layer is a ground plane, add vias near PGND.
2. Ensure that the high-current paths at PGND and IN have short, direct, and wide traces.
3. Place the ceramic input capacitor, especially the small package (0603) input bypass capacitor as close to IN and PGND pins as possible to minimize high frequency noise. Keep the connection of the input capacitor and IN as short and wide as possible.
4. Place the VCC capacitor to VCC pin and GND pin as close as possible.
5. Route SW, BST away from sensitive analog areas such as FB.
6. Place the feedback resistors close to chip to ensure the trace which connects to FB pin as short as possible.
7. A four-layer layout is strongly recommended to achieve better thermal performance. Use multiple vias to connect the power planes to internal layers.



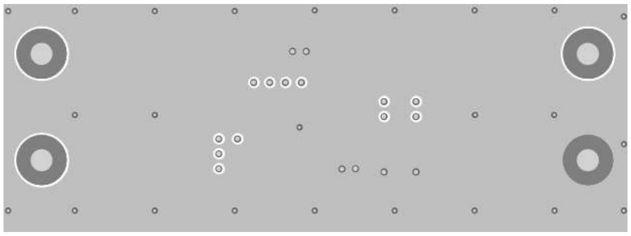
Top Layer



Inner1 Layer



Inner2 Layer



Bottom Layer

Figure 7: Recommended PCB Layout

Note:

7) The recommended layout is based on Figure 8.

TYPICAL APPLICATION CIRCUIT

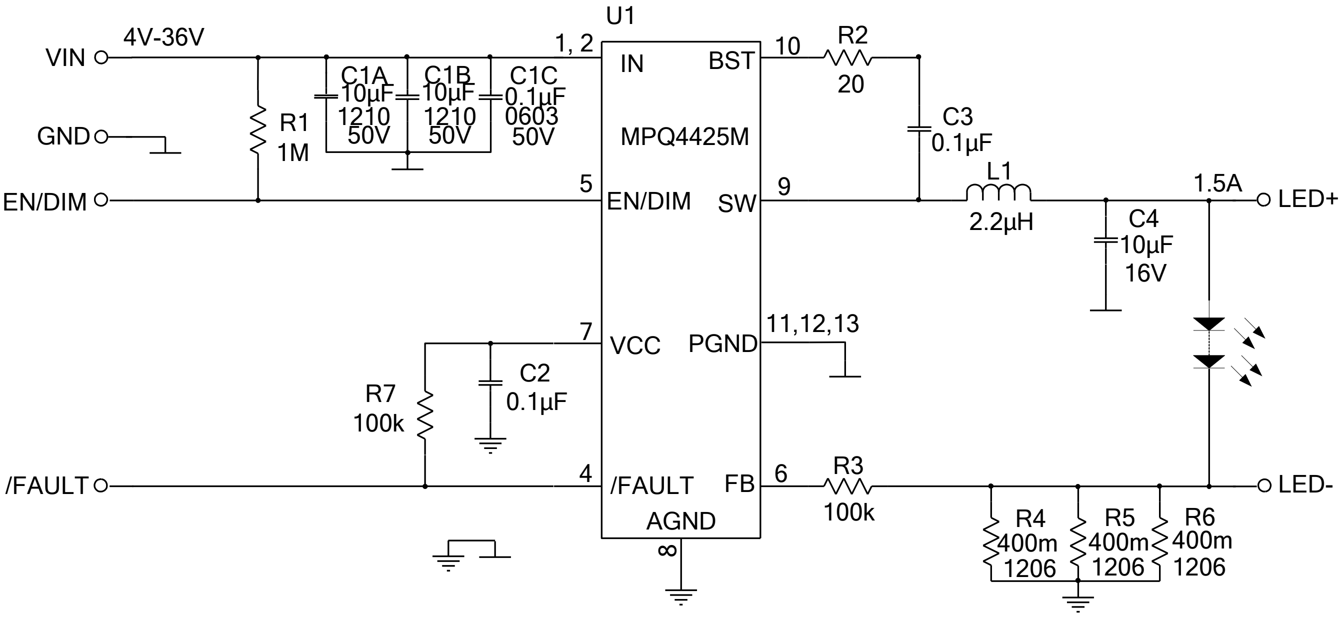


Figure 8: Io=1.5A Application Circuit

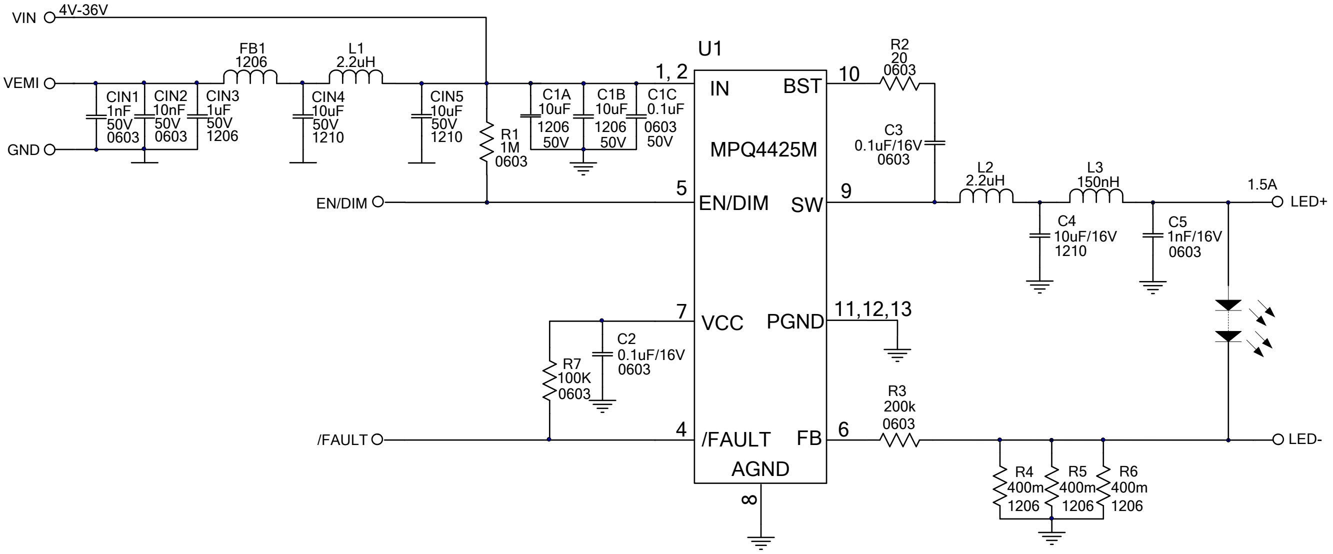
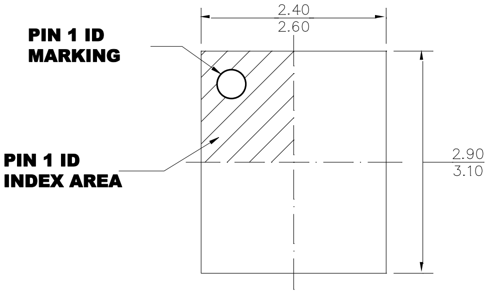


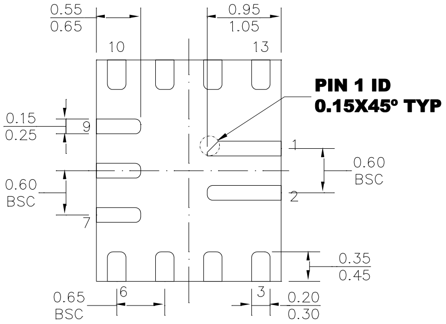
Figure 9: Io=1.5A Application Circuit with EMI Filters

PACKAGE INFORMATION

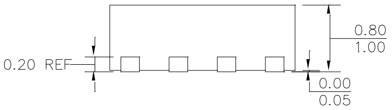
QFN-13 (2.5mmx3mm)
Non-Wettable Flank



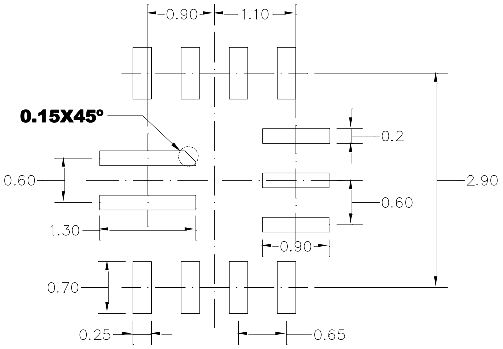
TOP VIEW



BOTTOM VIEW



SIDE VIEW



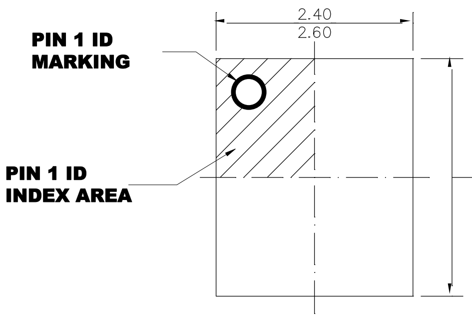
RECOMMENDED LAND PATTERN

NOTE:

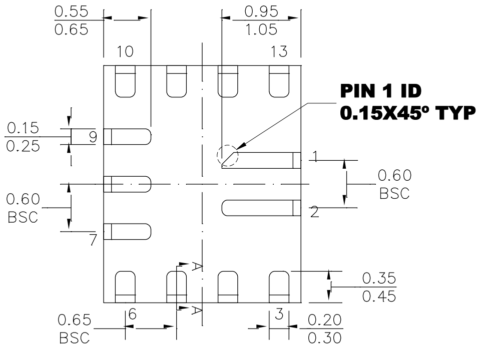
1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) LEAD COPLANARITY SHALL BE 0.10 MILLIMETERS MAX.
3) JEDEC REFERENCE IS MO-220.
4) DRAWING IS NOT TO SCALE.

PACKAGE INFORMATION

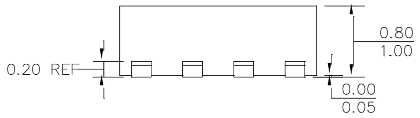
QFN-13 (2.5mmx3mm)
Wettable Flank



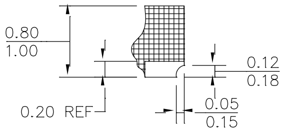
TOP VIEW



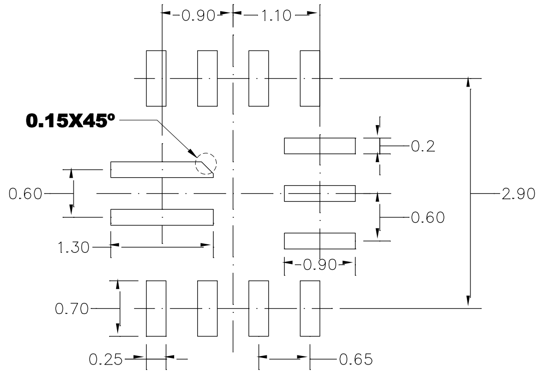
BOTTOM VIEW



SIDE VIEW



SECTION A-A



RECOMMENDED LAND PATTERN

NOTE:

1) THE LEAD SIDE IS WETTABLE.
2) ALL DIMENSIONS ARE IN MILLIMETERS.
3) LEAD COPLANARITY SHALL BE 0.08 MILLIMETERS MAX.
4) JEDEC REFERENCE IS MO-220.
5) DRAWING IS NOT TO SCALE.