A8292

Dual LNB Supply and Control Voltage Regulator

Discontinued Product

This device is no longer in production. The device should not be purchased for new design applications. Samples are no longer available.

Date of status change: January 4, 2019

Recommended Substitutions: Generation 4 and 5 devices

For existing customer transition, and for new customers or new applications, contact Allegro Sales.

NOTE: For detailed information on purchasing options, contact your local Allegro field applications engineer or sales representative.

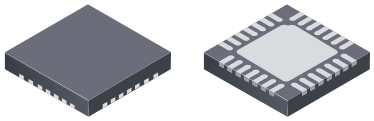
Dual LNB Supply and Control Voltage Regulator

Features and Benefits

- 2-wire serial I²C™ -compatible interface: control (write) and status (read)
- LNB voltages (16 programmable levels) compatible with all common standards
- Tracking switch-mode power converter for lowest dissipation
- Integrated converter switches and current sensing
- Provides up to 500 mA per channel and 750 mA total
- Static current limit circuit allows full current at startup and 13→18 V output transition; reliably starts wide load range
- Push-pull output stage minimizes 13→18 V and 18→13 V output transition times for highly capacitive loads
- Adjustable rise/fall time via external timing capacitor
- Built-in tone oscillator, factory-trimmed to 22 kHz facilitates DiSEqC™ tone encoding, even at no-load
- Four methods of 22 kHz tone generation, via I²C™ data bits and/or external pin
- 22 kHz tone detector facilitates DiSEqC™ 2.0 decoding
- Auxiliary modulation input
- LNB overcurrent with timer
- Diagnostics for output voltage level, input supply UVLO, and DiSEqC™ tone output
- Cable disconnect diagnostic

Package:

28 pin 5 mm × 5mm
MLP/QFN (suffix ET)



Description

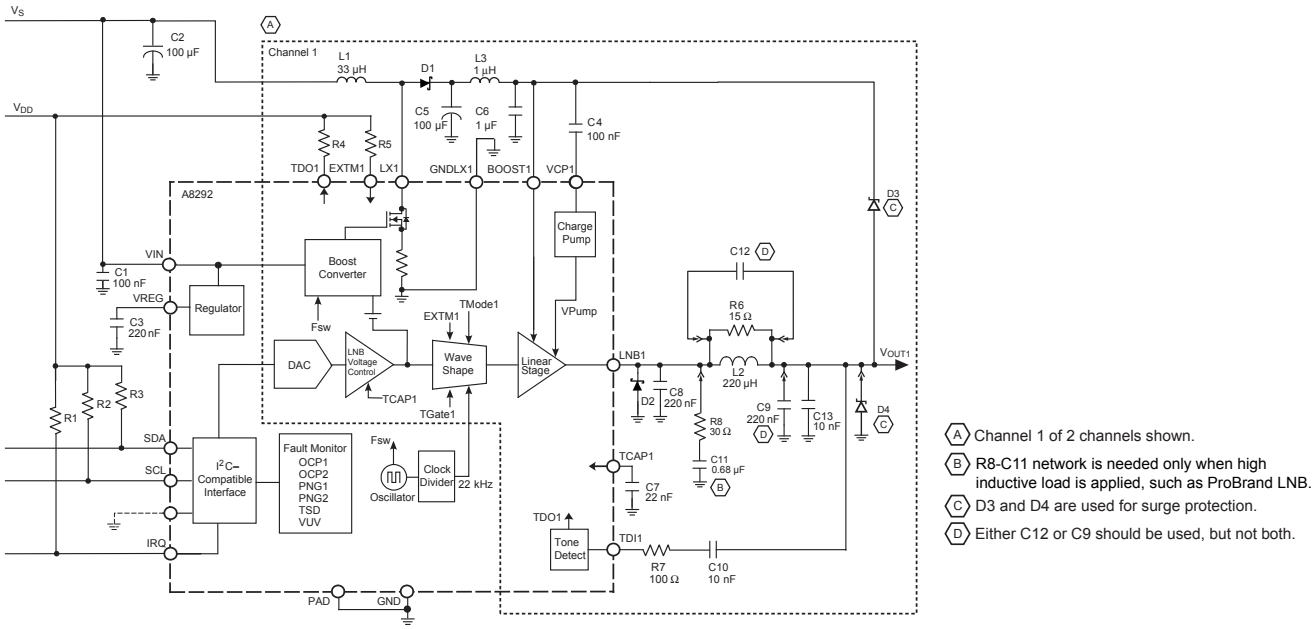
Intended for analog and digital satellite receivers, this dual low-noise block converter regulator (LNBR) is a monolithic linear and switching voltage regulator, specifically designed to provide the power and the interface signals to two LNB down converters via coaxial cables. The A8292 requires few external components, with the boost switches and compensation circuitry integrated inside of the device. A high switching frequency is chosen to minimize the size of the passive filtering components, further assisting in cost reduction. The high level of component integration ensures extremely low noise and ripple figures.

The A8292 has been designed for high efficiency, utilizing the Allegro™ advanced BCD process. The integrated boost switches have been optimized to minimize both switching and static losses. To further enhance efficiency, the voltage drop across the tracking regulators has been minimized.

The A8292 has integrated tone detection capability, to support full two-way DiSEqC™ communications. Several schemes are available for generating tone signals, all the way down to no-load, and using either the internal clock or an external time source.

Continued on the next page…

Functional Block Diagram



A Channel 1 of 2 channels shown.
B R8-C11 network is needed only when high inductive load is applied, such as ProBrand LNB.
C D3 and D4 are used for surge protection.
D Either C12 or C9 should be used, but not both.

Description (continued)

A comprehensive set of fault registers are provided which, comply with all the common standards, including: overcurrent, thermal shutdown, undervoltage, cable disconnect, power not good, and tone detect.

The device uses a 2-wire bidirectional serial interface, compatible with the I²C™ standard, that operates up to 400 kHz.

The A8292 is supplied in a lead (Pb) free 28-lead MLP/QFN with 100% matte tin leadframe plating.

Absolute Maximum Ratings

Characteristic	Symbol	Conditions	Rating	Units
Load Supply Voltage, VIN pin	V_{IN}		30	V
Output Current[1]	I_{OUT}		Internally Limited	A
Output Voltage, BOOST pin			–0.3 to 33	V
Output Voltage, LNB pin		Surge[2]	–1 to 33	V
Output Voltage, LX pin			–0.3 to 30	V
Output Voltage, VCP pin	V_{CP}		–0.3 to 41	V
Logic Input Voltage, EXTM pin			–0.3 to 5	V
Logic Input Voltage, other pins			–0.3 to 7	V
Logic Output Voltage			–0.3 to 7	V
Operating Ambient Temperature	T_A		–20 to 85	°C
Junction Temperature	T_J(max)		150	°C
Storage Temperature	T_{stg}		–55 to 150	°C

[1]Output current rating may be limited by duty cycle, ambient temperature, and heat sinking. Under any set of conditions, do not exceed the specified current ratings, or a junction temperature, T_J, of 150°C.
[2]Use Allegro recommended Application circuit.

Package Thermal Characteristics*

Package	$R_{\theta JA}$ (°C/W)	PCB
ET	32	4-layer

* Additional information is available on the Allegro website.

Ordering Information

Use the following complete part numbers when ordering:

Part Number	Packing[a]	Description
A8292SETTR-T[b]	7-in. reel, 1500 pieces/reel 12 mm carrier tape	ET package, MLP surface mount

[a]Contact Allegro for additional packing options.
[b]Leadframe plating 100% matte tin.

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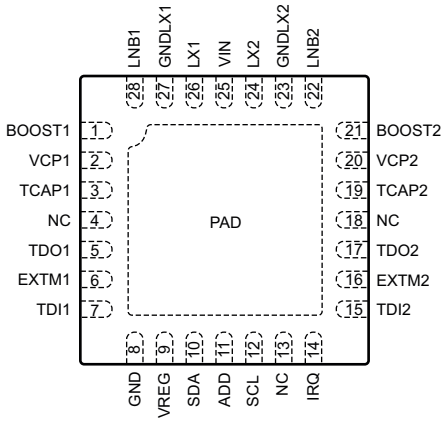
Device Pin-out Diagram



(Top View)

Terminal List Table

Name	Number	Function
GND	–	Fused internally; connect to ground plane for thermal dissipation
ADD	11	Address select
BOOST1	1	Tracking supply voltage to linear regulator (channel 1)
BOOST2	21	Tracking supply voltage to linear regulator (channel 2)
EXTM1	6	External modulation input (channel 1)
EXTM2	16	External modulation input (channel 2)
GND	8	Signal ground
PAD	Pad	Exposed thermal pad; connect to ground plane
GNDLX1	27	Boost switch ground (channel 1)
GNDLX2	23	Boost switch ground (channel 2)
IRQ	14	Interrupt request
LNB1	28	Output voltage to LNB (channel 1)
LNB2	22	Output voltage to LNB (channel 2)
LX1	26	Inductor drive point (channel 1)
LX2	24	Inductor drive point (channel 2)
NC	4, 13, 18	No connection
SCL	12	I²C™-compatible clock input
SDA	10	I²C™-compatible data input/output
TCAP1	3	Capacitor for setting the rise and fall time of the LNB output (channel 1)
TCAP2	19	Capacitor for setting the rise and fall time of the LNB output (channel 2)
TDI1	7	Tone detect input (channel 1)
TDI2	15	Tone detect input (channel 2)
TDO1	5	Tone detect output (channel 1)
TDO2	17	Tone detect output (channel 2)
VCP1	2	Gate supply voltage (channel 1)
VCP2	20	Gate supply voltage (channel 2)
VIN	25	Supply input voltage
VREG	9	Analog supply

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ELECTRICAL CHARACTERISTICS at T_A = 25°C, V_{IN} = 8 to 16 V, unless noted otherwise[1]

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Units
General						
Set-Point Accuracy, Load and Line Regulation	Err	Relative to selected V_{LNB} target level, I_{LOAD} = 0 to 450 mA	–3	–	3	%
Supply Current	$I_{IN(Off)}$	ENB bit = 0, LNB output disabled, V_{IN} = 12 V	–	–	12.0	mA
	$I_{IN(On)}$	ENB bit = 1, LNB output enabled, I_{LOAD} = 0 mA, V_{IN} = 12 V	–	–	20.0	mA
Boost Switch On Resistance	$R_{DS(on)BOOST}$	I_{LOAD} = 450 mA	–	300	600	mΩ
Switching Frequency	f_{SW}		320	352	384	kHz
Switch Current Limit	I_{LIMSW}	V_{IN} = 10 V, V_{OUT} = 20.3 V	–	3.0	–	A
Linear Regulator Voltage Drop	ΔV_{REG}	$V_{BOOST} - V_{LNB}$, no tone signal, I_{LOAD} = 450 mA	600	800	1000	mV
TCAP Pin Current	I_{CHG}	TCAP capacitor (C7) charging	–12.5	–10	–7.5	µA
	I_{DISCHG}	TCAP capacitor (C7) discharging	7.5	10	12.5	µA
Output Voltage Rise Time[2]	$t_{r(VLNB)}$	For V_{LNB} 13→18 V; C_{TCAP} = 5.6 nF, I_{LOAD} = 450 mA	–	500	–	µs
Output Voltage Pull-Down Time[2]	$t_{f(VLNB)}$	For V_{LNB} 18→13 V; C_{LOAD} = 100 µF, I_{LOAD} = 0 mA	–	12.5	–	ms
Output Reverse Current	I_{RLNB}	ENB bit = 0, V_{LNB} = 33 V , BOOST capacitor (C5) fully charged	–	1	5	mA
Ripple and Noise on LNB Output[3]	$V_{rip,n(pp)}$	20 MHz BWL; reference circuit shown in Functional Block diagram; contact Allegro for additional information on application circuit board design	–	30	–	mV_{PP}
Protection Circuitry						
Output Overcurrent Limit[4]	I_{LIMLNB}	$V_{BOOST} - V_{LNB}$ = 800 mV	500	600	700	mA
Overcurrent Disable Time	t_{DIS}		40.0	48	56.0	ms
VIN Undervoltage Lockout Threshold	V_{UVLO}	V_{IN} falling	7.05	7.35	7.65	V
VIN Turn On Threshold	$V_{IN(th)}$	V_{IN} rising	7.40	7.70	8.00	V
Undervoltage Hysteresis	$V_{UVLOHYS}$		–	350	–	mV
Thermal Shutdown Threshold[2]	T_J		–	165	–	°C
Thermal Shutdown Hysteresis[2]	ΔT_J		–	20	–	°C
Power Not Good Flag Set	PNG_{SET}	With respect to V_{LNB}	77	85	93	%
Power Not Good Flag Reset	PNG_{RESET}	With respect to V_{LNB}	82	90	98	%
Power Not Good Hysteresis	PNG_{HYS}	With respect to V_{LNB}	–	5	–	%
Cable Disconnect Boost Voltage	V_{CAD}	CADT bit = 1, ENB bit = 1, VSEL0 through VSEL3 = 1	22.0	22.8	23.5	V
Cable Disconnect Set	V_{CADSET}		20.16	21.00	21.84	V
Cable Disconnect Current Source	I_{CADSRC}	V_{LNB} = 21.00 V, V_{BOOST} = 22.8 V	1.0	1.75	2.5	mA

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ELECTRICAL CHARACTERISTICS (continued) at T_A = 25°C, V_{IN} = 8 to 16 V, unless noted otherwise[1]

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Tone						
Tone Frequency	f_{TONE}		20	22	24	kHz
Tone Amplitude, Peak-to-Peak	$V_{TONE(pp)}$	I_{LOAD} = 0 to 450 mA, C_{LOAD} = 750 nF	400	620	800	mV
Tone Duty Cycle	DC_{TONE}	I_{LOAD} = 0 to 450 mA, C_{LOAD} = 750 nF	40	50	60	%
Tone Rise Time	t_{rTONE}	I_{LOAD} = 0 to 450 mA, C_{LOAD} = 750 nF	5	10	15	µs
Tone Fall Time	t_{fTONE}	I_{LOAD} = 0 to 450 mA, C_{LOAD} = 750 nF	5	10	15	µs
EXTM Logic Input	$V_{EXTM(H)}$		2.0	–	–	V
	$V_{EXTM(L)}$		–	–	0.8	V
EXTM Input Leakage	$I_{EXTMLKG}$		–1	–	1	µA
Tone Detector						
Tone Detect Input Amplitude Receive, Peak-to-Peak	$V_{TDR(pp)}$	f_{TONE} = 22 kHz sine wave, TMODE = 0	300	–	–	mV
Tone Detect Input Amplitude Transmit, Peak-to-Peak	$V_{TDT(pp)Int}$	f_{TONE} = 22 kHz sine wave, using internal tone (options 1 and 2, in figure 1)	400	–	–	mV
	$V_{TDT(pp)Ext}$	f_{TONE} = 22 kHz sine wave, using external tone (options 3 and 4, in figure 1)	300	–	–	mV
Tone Reject Input Amplitude, Peak-to-Peak	$V_{TRI(pp)}$	f_{TONE} = 22 kHz sine wave	–	–	100	mV
Frequency Capture	f_{TDI}	600 mVpp sine wave	17.6	–	26.4	kHz
Input Impedance[2]	Z_{TDI}		–	8.6	–	kΩ
TDO Output Voltage	$V_{TDO(L)}$	Tone present, I_{LOAD} = 3 mA	–	–	0.4	V
TDO Output Leakage	I_{TDOLKG}	Tone absent, V_{TDO} = 7 V	–	–	10	µA
I²C™-Compatible Interface						
Logic Input (SDA,SCL) Low Level	$V_{SCL(L)}$		–	–	0.8	V
Logic Input (SDA,SCL) High Level	$V_{SCL(H)}$		2.0	–	–	V
Logic Input Hysteresis	$V_{I2CIHYS}$		–	150	–	mV
Logic Input Current	I_{I2CI}	V_{I2CI} = 0 to 7 V	–10	<±1.0	10	µA
Logic Output Voltage SDA and IRQ	$V_{t2COut(L)}$	I_{LOAD} = 3 mA	–	–	0.4	V
Logic Output Leakage SDA and IRQ	V_{t2CLKG}	V_{t2COut} = 0 to 7 V	–	–	10	µA
SCL Clock Frequency	f_{CLK}		–	–	400	kHz
Output Fall Time	$t_{fI2COut}$	$V_{t2COut(H)}$ to $V_{t2COut(L)}$	–	–	250	ns
Bus Free Time Between Stop/Start	t_{BUF}		1.3	–	–	µs
Hold Time Start Condition	$t_{HD:STA}$		0.6	–	–	µs
Setup Time for Start Condition	$t_{SU:STA}$		0.6	–	–	µs

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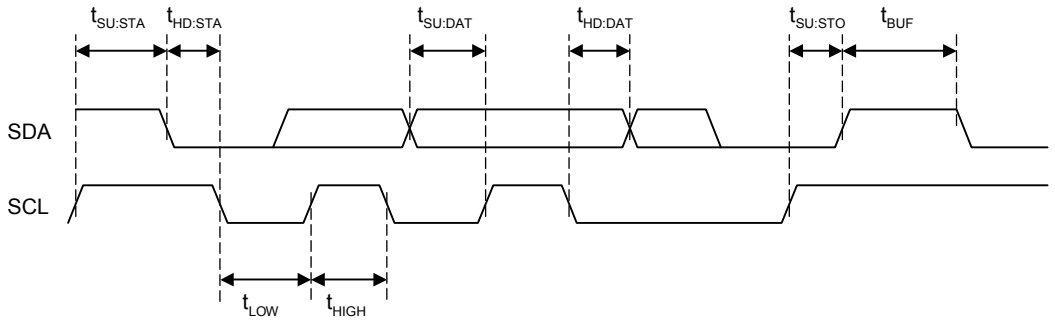
ELECTRICAL CHARACTERISTICS (continued) at T_A = 25°C, V_{IN} = 8 to 16 V, unless noted otherwise[1]

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Units
I²C™-Compatible Interface (continued)						
SCL Low Time	t_{LOW}		1.3	–	–	µs
SCL High Time	t_{HIGH}		0.6	–	–	µs
Data Setup Time	$t_{SU:DAT}$		100	–	–	ns
Data Hold Time	$t_{HD:DAT}$	For $t_{HD:DAT}$(min), the master device must provide a hold time of at least 300 ns for the SDA signal in order to bridge the undefined region of the SCL signal falling edge	0	–	900	ns
Setup Time for Stop Condition	$t_{SU:STO}$		0.6	–	–	µs
I²C™ Address Setting						
ADD Voltage for Address 0001,000	Address1		0	–	0.7	V
ADD Voltage for Address 0001,001	Address2		1.3	–	1.7	V
ADD Voltage for Address 0001,010	Address3		2.3	–	2.7	V
ADD Voltage for Address 0001,011	Address4		3.3	–	5.0	V

[1]Operation at 16 V may be limited by power loss in the linear regulator.
[2]Guaranteed by worst case process simulations and system characterization. Not production tested.
[3]LNB output ripple and noise are dependent on component selection and PCB layout. Refer to the Application Schematic and PCB layout recommendations. Not production tested.
[4]Current from the LNB output may be limited by the choice of Boost components.

I²C™ Interface Timing Diagram



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Functional Description

Protection

The A8292 has a wide range of protection features and fault diagnostics which are detailed in the Status Register section.

Boost Converter/Linear Regulator

Each channel contains a tracking current-mode boost converter and linear regulator. The boost converter tracks the requested LNB voltage to within 800 mV, to minimize power dissipation. Under conditions where the input voltage, V_{BOOST}, is greater than the output voltage, V_{LNB}, the linear regulator must drop the differential voltage. When operating in these conditions, care must be taken to ensure that the safe operating temperature range of the A8292 is not exceeded.

The A8292 has internal pulse-by-pulse current limit on the boost converter, and DC current limiting on the LNB output, to protect the IC against short circuits. When the LNB output is shorted, the LNB output current is limited to 600 mA typical, and the IC will be shut down if the overcurrent condition lasts for more than 48 ms. If this occurs, the A8292 must be re-enabled for normal operation. The system should provide sufficient time between successive restarts to limit internal power dissipation; a period of 2 s is recommended.

Each of the boost converters operates at 352 kHz typical: 16 times the internal 22 kHz tone frequency. All the loop compensation, current sensing, and slope compensation functions are provided internally.

At extremely light loads, the boost converters operate in a pulse-skipping mode. Pulse skipping occurs when the BOOST voltage rises to approximately 450 mV above the BOOST target output voltage. Pulse skipping stops when the BOOST voltage drops 200 mV below the pulse skipping level.

In the case that two or more set top box LNB outputs are connected together by the customer (e.g., with a splitter), it is possible that one output could be programmed at a higher voltage than the other. This would cause a voltage on one output that is higher than its programmed voltage (e.g., 19 V on the output of a 13 V programmed voltage). The output with the highest voltage will effectively turn off the other outputs. As soon as this voltage is reduced below the value of the other outputs, the A8292 output will autorecover to their programmed levels.

Charge Pump. Each generates a supply voltage above the internal tracking regulator output to drive the linear regulator control.

Slew Rate Control. During either start-up, or when the output voltage at the LNB pin is transitioning, the output voltage rise and fall times can be set by the value of the capacitor connected from the TCAP pin to GND (C_{TCAP} or C7 in the Applications Schematic). Note that during start-up, the BOOST pin is precharged to the input voltage minus a voltage drop. As a result, the slew rate control for the BOOST pin occurs from this voltage.

The value of C_{TCAP} can be calculated using the following formula:

$$C_{TCAP} = (I_{TCAP} \times 6) / SR \ ,$$

where SR is the required slew rate of the LNB output voltage, in V/s, and I_{TCAP} is the TCAP pin current specified in the data sheet. The recommended value for C_{TCAP}, 10 nF, should provide satisfactory operation for most applications. However, in some cases, it may be necessary to increase the value of C_{TCAP} to avoid activating the current limit of the LNB output. One such situation is when two set-top boxes are connected in parallel. If this is the case, the following formula can be used to calculate C_{TCAP}:

$$C_{TCAP} \geq (I_{TCAP} \times 6)(2 \times C_{BOOST}) / I_{LIMLNB} \ ,$$

$$C_{TCAP} \geq (10\ \mu A \times 6)(2 \times 100\ \mu F) / 500\ mA = 24\ nF \ .$$

The minimum value of C_{TCAP} is 2.2 nF. There is no theoretical maximum value of C_{TCAP} however too large a value will probably cause the voltage transition specification to be exceeded. Tone generation is unaffected by the value of C_{TCAP}.

Pull-Down Rate Control. In applications that have to operate at very light loads and that require large load capacitances (in the order of tens to hundreds of microfarads), the output linear stage provides approximately 40 mA of pull-down capability. This ensures that the output volts are ramped from 18 to 13 V in a reasonable amount of time.

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ODT (Overcurrent Disable Time)

If the LNB output current exceeds 600 mA, typical, for more than 48 ms, then the LNB output will be disabled and the OCP bit will be set (see figure 1).

Short Circuit Handling

If the LNB output is shorted to ground, the LNB output current will be clamped to 600 mA, typical. If the short circuit condition lasts for more than 48 ms, the A8292 will be disabled and the OCP bit will be set.

Auto-Restart

After a short circuit condition occurs, the host controller should periodically re-enable the A8292 to check if the short circuit has been removed. Consecutive startup attempts should allow at least 2 s of delay between restarts.

In-rush Current

At start-up or during an LNB reconfiguration event, a transient surge current above the normal DC operating level can be provided by the A8292. This current increase can be as high as 600 mA, typical, for as long as required, up to a maximum of 48 ms. The 8292 can also provide up to 500 mA per channel individually, or 900 mA to both channels simultaneously, for a period of up to 2 s (see figure 1). Operating at this level for a longer period is not recommended.

Tone Detection

A 22 kHz tone detector is provided in each channel of the A8292 solution. The detector extracts the tone signal and provides it as an open-drain signal on the TDO pins. The maximum tone out error is ±1 tone cycle, and the maximum tone out delay with respect to the input is 1 tone cycle. Detection thresholds are given in table 1.

Table 1. Detection Thresholds for Tone Generation Options

Option (Fig. 1)	Transmit				Receive	
	1	2	3	4	n.a.	n.a.
TMODE	1	1	0	0	0	1
TGATE	Control 0/1	1	Control 0/1	1	At least one must be 0 to prevent tone transmission	
EXTM	1	Control 0/1	22 kHz logic signal, continuous	Control gated 22 kHz logic signal		
Guaranteed Detection Threshold (mV_{PP})	400	400	300	300	300	400
Rejection Threshold (mV_{PP})	100	100	100	100	100	100

ODT (Overcurrent Disable Timing) Mode Timing Diagram

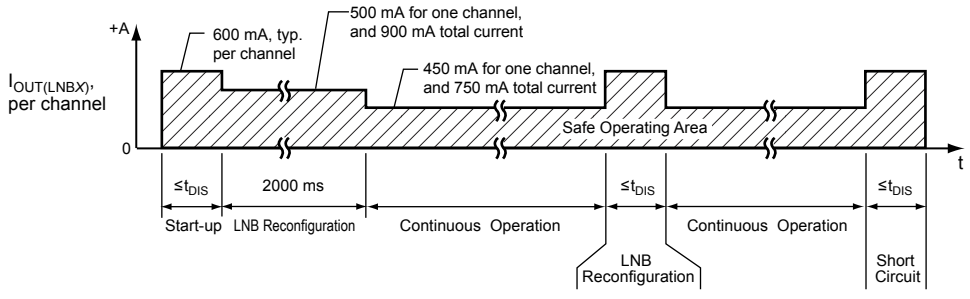

Figure 1. ODT (Overcurrent Disable Timing) Mode Timing Diagram

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Tone Generation

The A8292 solution offers four options for tone generation, providing maximum flexibility to cover every application. The EXTM pins (external modulation), in conjunction with the I²C™ control bits: TMODE (tone modulation) and TGATE (tone gate), provide the necessary control. The TMODE bit controls whether the tone source is either internal or external (via the EXTM pin). Both the EXTM pin and TGATE bit determine the 22 kHz control, whether gated or clocked.

Four options for tone generation are shown in figure 2. Note that when using option 4, when EXTM stops clocking, the LNB volts park at the LNB voltage, either plus or minus half the tone signal amplitude, depending on the state of EXTM. For example, if the EXTM is held low, the LNB DC voltage is the LNB programmed voltage minus 325 mV (typical).

With any of the four options, when a tone signal is generated, TDET is set in the status register. When the internal tone is used (options 1 or 2), the minimum tone detect amplitude is 400 mV, and when an external tone is used (options 3 or 4), the minimum tone detection amplitude is 300 mV.

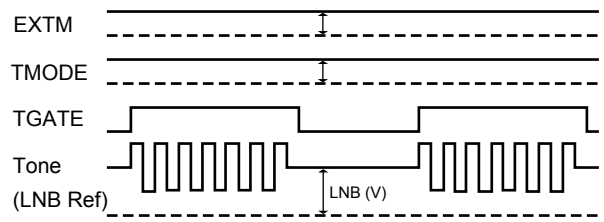
I²C™-Compatible Interface

This is a serial interface that uses two bus lines, SCL and SDA, to access the internal Control and Status registers of the A8292. Data is exchanged between a microcontroller (master) and the A8292 (slave). The clock input to SCL is generated by the master, while SDA functions as either an input or an open drain output, depending on the direction of the data.

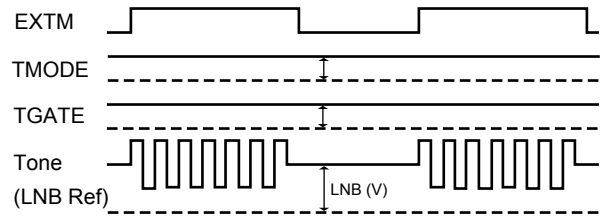
Timing Considerations

The control sequence of the communication through the I²C™-compatible interface is composed of several steps in sequence:

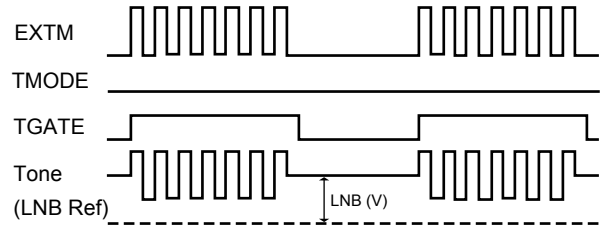
1. Start Condition. Defined by a negative edge on the SDA line, while SCL is high.
2. Address Cycle. 7 bits of address, plus 1 bit to indicate read (1) or write (0), and an acknowledge bit. The first five bits of the address are fixed as: 00010. The four optional addresses, defined by the remaining two bits, are selected by the ADD input. The address is transmitted MSB first.



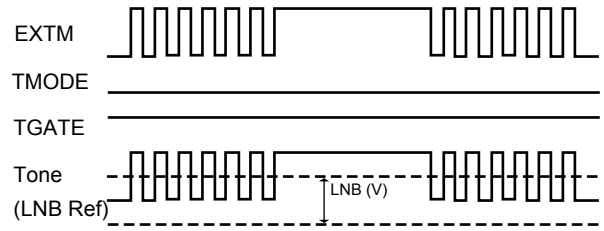
Option 1 – Use internal tone, gated by the TGATE bit.



Option 2 – Use internal tone, gated by the EXTM pin.



Option 3 – Use external tone, gated by the TGATE bit.



Option 4 – Use external tone.

Figure 2. Options for tone generation

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3. Data Cycles.
   Write – 6 bits of data and 2 bits for addressing four internal control registers, followed by an acknowledge bit. See Control Register section for more information.
   Read – Two status registers, where register 1 is read first, followed by register 2, then register 1, and so on. At the start of any read sequence, register 1 is always read first. Data is transmitted MSB first.
4. Stop Condition. Defined by a positive edge on the SDA line, while SCL is high. Except to indicate a Start or Stop condition, SDA must be stable while the clock is high. SDA can only be changed while SCL is low. It is possible for the Start or Stop condition to occur at any time during a data transfer. The A8292 always responds by resetting the data transfer sequence.

The Read/Write bit is used to determine the data transfer direction. If the Read/Write bit is high, the master reads the contents of register 1, followed by register 2 if a further read is performed. If the Read/Write bit is low, the master writes data to one of the four Control registers. Note that multiple writes are not permitted. All write operations must be preceded with the address.

The Acknowledge bit has two functions. It is used by the master to determine if the slave device is responding to its address and data, and it is used by the slave when the master is reading data back from the slave. When the A8292 decodes the 7-bit address field as a valid address, it responds by pulling SDA low during the ninth clock cycle.

During a data write from the master, the A8292 also pulls SDA low during the clock cycle that follows the data byte, in order to indicate that the data has been successfully received. In both cases, the master device must release the SDA line before the ninth clock cycle, in order to allow this handshaking to occur.

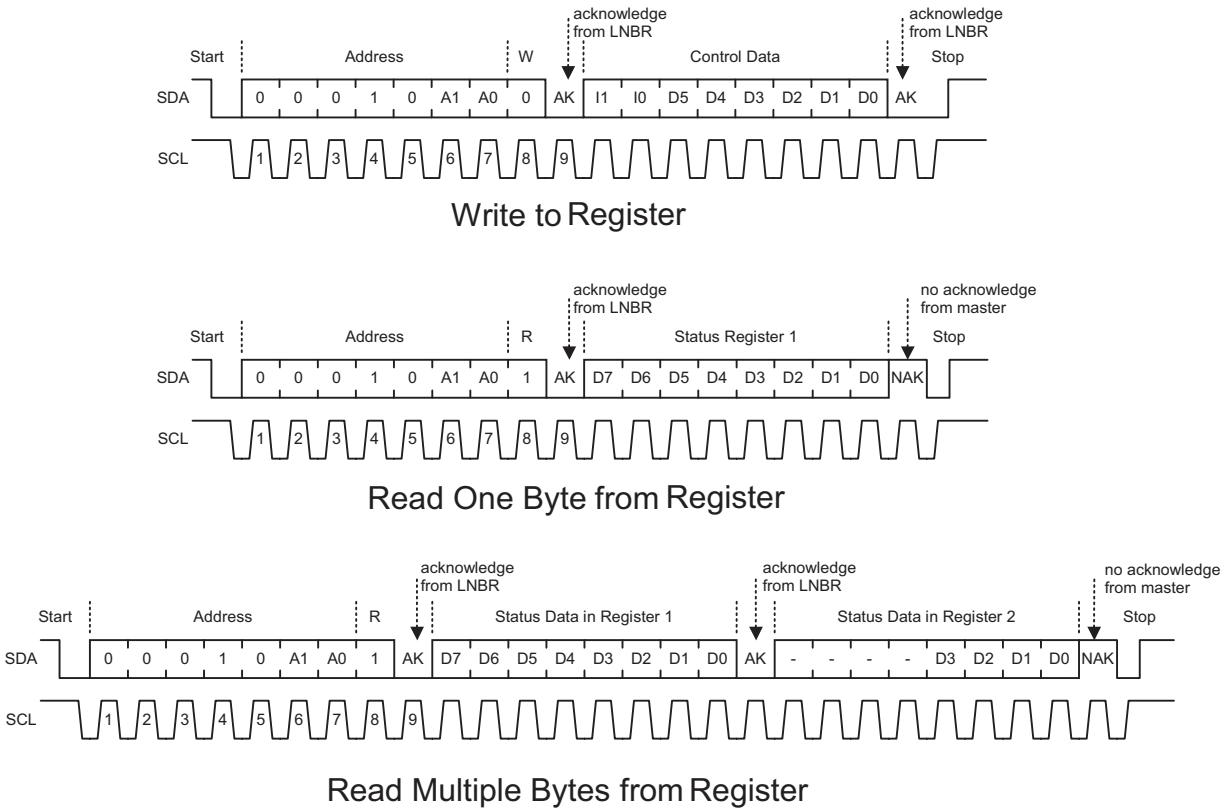

Figure 3. I²C™ Interface. Read and write sequences.

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During a data read, the A8292 acknowledges the address in the same way as in the data write sequence, and then retains control of the SDA line and send the data from register 1 to the master. On completion of the eight data bits, the A8292 releases the SDA line before the ninth clock cycle, in order to allow the master to acknowledge the data. If the master holds the SDA line low during this Acknowledge bit, the A8292 responds by sending the data from register 2 to the master. Data bytes continue to be sent to the master until the master releases the SDA line during the Acknowledge bit. When this is detected, the A8292 stops sending data and waits for a stop signal.

Interrupt Request

The A8292 also provides an interrupt request pin, IRQ, which is an open-drain, active-low output. This output may be connected to a common IRQ line with a suitable external pull-up and can be used with other I²C™-compatible devices to request attention from the master controller.

The IRQ output becomes active when either the A8292 first recognizes a fault condition, or at power-on, when the main supply, V_{IN}, and the internal logic supply, V_{REG}, reach the correct operating conditions. It is only reset to inactive when the I²C™ master addresses the A8292 with the Read/Write bit set (causing a read). Fault conditions are indicated by the TSD, VUV, and OCP bits, and are latched in the Status register. See the Status register section for full description.

The DIS, PNG, CAD and TDET status bits do not cause an interrupt. All these bits are continually updated, apart from the DIS bit, which changes when the LNB is either disabled, intentionally or due to a fault, or is enabled.

When the master recognizes an interrupt, it addresses all slaves connected to the interrupt line in sequence, and then reads the status register to determine which device is requesting attention. The A8292 latches all conditions in the Status register until the completion of the data read. The action at the resampling point is further defined in the Status Register section. The bits in the Status register are defined such that the all-zero condition indicates that the A8292 is fully active with no fault conditions.

When V_{IN} is initially applied, the I²C™-compatible interface does not respond to any requests until the internal logic supply V_{REG} has reached its operating level. Once V_{REG} has reached this point, the IRQ output goes active, and the VUV bit is set. After the A8292 acknowledges the address, the IRQ flag is reset. After the master reads the status registers, the registers are updated with the VUV reset.

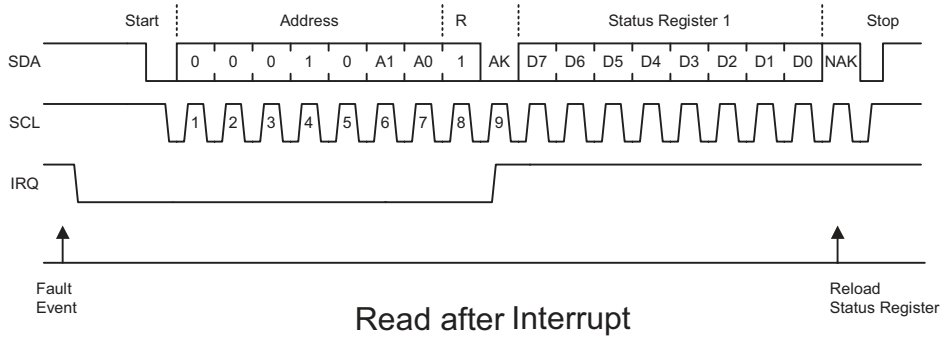

Figure 4. I²C™ Interface. Read sequences after interrupt request.

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Control Registers (I²C™-Compatible Write Register)

All main functions of the A8292 are controlled through the I²C™-compatible interface via the 8-bit Control registers. As the A8292 contains numerous control options, as well as featuring two channels, it is necessary to have four Control registers. Each register contains up to 6 bits of data (bit 0 to bit 5), followed by 2 bits for the register address (bit 6 and bit 7). The power-up states for the control functions are all 0s.

The following tables define the control bits for each address and the settings for output voltage:

Table 2. Control Registers with Address (I1, I0) = 00 and 01

Bit	Name		Setting
	Channel 1 (Address: I1, I0 = 00)	Channel 2 (Address: I1, I0 = 01)	
0	$VSEL_0$1	$VSEL_0$2	See table 4, Output Voltage Amplitude Selection
1	$VSEL_1$1	$VSEL_1$2	
2	$VSEL_2$1	$VSEL_2$2	
3	$VSEL_3$1	$VSEL_3$2	0: LNB*x* = Low range 1: LNB*x* = High range
4	ODT1	ODT2	1 (recommended): The ODT functions are always enabled, but setting 1 recommended at all times.
5	ENB1	ENB2	0: Disable LNB*x* Output 1: Enable LNB*x* Output
6	I0	I0	Address Bit Channel 1: 0 Channel 2: 1
7	I1	I1	Address Bit Channel 1: 0 Channel 2: 0

Bit 0	$VSEL_0x$	These three bits provide incremental control over the voltage on the LNB*x* output.
Bit 1	$VSEL_1x$	The available voltages provide the necessary levels for all the common standards
Bit 2	$VSEL_2x$	plus the ability to add line compensation in increments of 333 mV. The voltage levels are defined in table 4, Output Voltage Amplitude Selection.
Bit 3	$VSEL_3x$	Switches between the low level and high level output voltages on the LNB*x* output. 0 selects the low level voltage and 1 selects the high level. The low-level center voltage is 12.709 V nominal and the high level is 18.042 V nominal. These may be increased in steps of 333 mV using the $VSEL_2x$, $VSEL_1x$ and $VSEL_0x$ control register bits.
Bit 4	ODT*x*	The overcurrent disable timers are always enabled.
Bit 5	ENB*x*	Enables the LNB*x* output. When set to 1 the LNB*x* output is switched on. When set to 0, the LNB*x* output is disabled.
Bit 6	I0	Address
Bit 7	I1	Address

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Table 3. Control Registers with Address (I1, I0) = 10 and 11

Bit	Name		Setting
	Channel 1 (Address: I1, I0 = 10)	Channel 2 (Address: I1, I0 = 11)	
0	TMODE1	TMODE2	0: External Tone 1: Internal Tone
1	TGATE1	TGATE2	0: Tone Gated Off 1: Tone Gated On
2	CADT1	CADT2	0: Cable Disconnect Test Off 1: Cable Disconnect Test On
3	–	–	Not Used
4	–	–	Not Used
5	–	–	Not Used
6	I0	I0	Address Bit Channel 1: 0 Channel 2: 1
7	I1	I1	Address Bit Channel 1: 1 Channel 2: 1

Bit 0 TMODE*x* ToneMode. Selects between the use of an external 22 kHz logic signal or the use of the internal 22 kHz oscillator to control the tone generation on the LNB*x* output. A 0 selects the external tone and a 1 selects the internal tone. See the Tone Generation section for more information

Bit 1 TGATE*x* Tone Gate. Allows either the internal or external 22 kHz tone signals to be gated, unless the EXTM*x* is selected for gating. When set to 0, the selected tone (via TMODE*x*) is off. When set to 1, the selected tone is on. See Tone Generation Section for more information.

Bit 2 CADT*x* Cable Disconnect Test. To perform this test, set bits CADT, ENB, and VSEL0 through VSEL3 through the I^2C-compatible interface. During this test, the LNB linear regulator is disabled, a 1 mA current source between the BOOST output and the LNB output is enabled, and the BOOST voltage is increased to 22.8 V. After these conditions are set, if the LNB voltage is above 21 V, it is assumed that the coaxial cable connection between the LNBR output and the LNB head has been disconnected. In this case, the CAD bit is set in the Status register. If there is a load on the LNB pin, then the LNB voltage will decrease proportionally to the load current. If the LNB volts drop below 19.95 V, it is assumed that the coaxial cable is connected and the CAD bit in the Status register is set to 0.

Bit 3 – Not Used.

Bit 4 – Not Used.

Bit 5 – Not Used.

Bit 6 I0 Address.

Bit 7 I1 Address.

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Table 4. Output Voltage Amplitude Selection

$VSEL_3x$	$VSEL_2x$	$VSEL_1x$	$VSEL_0x$	LNB (V)
0	0	0	0	12.709
0	0	0	1	13.042
0	0	1	0	13.375
0	0	1	1	13.709
0	1	0	0	14.042
0	1	0	1	14.375
0	1	1	0	14.709
0	1	1	1	15.042
1	0	0	0	18.042
1	0	0	1	18.375
1	0	1	0	18.709
1	0	1	1	19.042
1	1	0	0	19.375
1	1	0	1	19.709
1	1	1	0	20.042
1	1	1	1	20.375

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Status Registers (I²C™-Compatible Read Register)

The main fault conditions: overcurrent (OCP), under voltage (VUV) and overtemperature (TSD), are all indicated by setting the relevant bits in the Status registers. In all fault cases, once the bit is set, it remains latched until the A8292 is read by the I²C™ master, assuming the fault has been resolved.

The current status of each LNB output is indicated by the disable bit, DIS, for that channel. A DIS bit is set when either a fault occurs or if the LNB is disabled intentionally. These bits are latched and are reset when the LNB is commanded on again. The power not good (PNG), tone detect (TDET), and cable disconnected (CAD) flags are the only bits which may be reset without an I²C™ read sequence. Table 5 summarizes the condition of each bit when set and how it is reset.

As the A8292 has a comprehensive set of status reporting bits, it is necessary to have two Status registers. When performing a multiple read function, register 1 is read followed by register 2, then register 1 again and so on. Whenever a new read function is performed, register 1 is always read first.

The normal sequence of the master in a fault condition will be to detect the fault by reading the Status registers, then rereading the Status registers until the status bit is reset indicating the fault condition is reset. The fault may be detected either by continuously polling, by responding to an interrupt request (IRQ), or by detecting a fault condition externally and performing a diagnostic poll of all slave devices. Note that the fully-operational condition of the Status registers is all 0s, to simplify checking of the Status bit.

Table 5. Status Register Bit Setting

Status Bit	Function	Set	Reset Condition
CAD1, CAD2	Cable disconnected	Non-latched	Cable disconnect test off or cable connected
DIS1, DIS2	LNB disabled, either intentionally or due to fault	Latched	LNB enabled and no fault
OCP1, OCP2	Overcurrent	Latched	I²C™ read and fault removed
PNG1, PNG2	Power not good	Non-latched	LNB volts in range
TDET1, TDET2	Tone detect	Non-latched	Tone removed
TSD	Thermal shutdown	Latched	I²C™ read and fault removed
VUV	Undervoltage	Latched	I²C™ read and fault removed

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Table 6. Status Register 1

Bit	Name	Function
0	DIS1	LNB output disabled (Channel 1)
1	DIS2	LNB output disabled (Channel 2)
2	OCP1	Overcurrent (Channel 1)
3	OCP2	Overcurrent (Channel 2)
4	PNG1	Power Not Good (Channel 1)
5	PNG2	Power Not Good (Channel 2)
6	TSD	Thermal Shutdown
7	VUV	V_{IN} Undervoltage

Bit 0 DIS1 LNB Output Disabled. DIS is used to indicate the current condition of the LNB output for channel 1. At power-on, or if a fault condition occurs, DIS1 is set. This bit changing to 1 does not cause the IRQ to activate because the LNB output may be disabled intentionally by the I²C™ master. This bit will be reset at the end of a write sequence if the LNB output is enabled.

Bit 1 DIS2 See description for DIS1. This indicates status for channel 2.

Bit 2 OCP1 Overcurrent. If the LNB output detects an overcurrent condition for greater than 48 ms, the LNB output will be disabled. The OCP bit will be set to indicate that an overcurrent has occurred and the disable bit, DIS1, will be set. The Status register is updated on the rising edge of the 9th clock pulse in the data read sequence, where the OCP bit is reset in all cases, allowing the master to reenable the LNB output. If the overcurrent timer is not enabled, the device operates in current limit indefinitely and the OCP bit will be set. If the overcurrent condition is removed, the OCP bit will automatically be reset. Note that if the overcurrent remains long enough, and a thermal shutdown occurs, the LNB output will be disabled and the TSD bit set.

Bit 3 OCP2 See description for OCP1. This indicates status for channel 2.

Bit 4 PNG1 Power Not Good. Set to 1 when the LNB voltage is below 85% of the programmed voltage. The PNG bit is reset when the LNB voltage is within 90% of the programmed LNB voltage. PNG is always active so, if the LNB output is disabled, then PNG will be a logic 1. At power-up, PNG reports a logic 1 until the LNB output is enabled and within 90% of the programmed LNB voltage.

Bit 5 PNG2 See description for PNG1. This indicates status for channel 2.

Bit 6 TSD Thermal shutdown. 1 indicates that the A8292 has detected an overtemperature condition and has disabled the LNB outputs. The disable bits, DIS*x*, will also be set. The status of the overtemperature condition is sampled on the rising edge of the 9th clock pulse in the data read sequence. If the condition is no longer present, then the TSD bit will be reset, allowing the master to reenable the LNB output if required. If the condition is still present, then the TSD bit will remain at 1.

Bit 7 VUV Undervoltage Lockout. 1 indicates that the A8292 has detected that the input supply, V_{IN} is, or has been, below the minimum level and an undervoltage lockout has occurred disabling the LNB outputs. The disable bits, DIS*x*, will also be set, and the A8292 will not reenable the output until so instructed by writing the relevant bit into the control registers. The status of the undervoltage condition is sampled on the rising edge of the 9th clock pulse in the data read sequence. If the condition is no longer present, then the VUV bit will be reset allowing the master to reenable the LNB output if required. If the condition is still present, then the VUV bit will remain at 1.

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Table 7. Status Register 2

Bit	Name	Function
0	CAD1	Cable Disconnected (Channel 1)
1	CAD2	Cable Disconnected (Channel 2)
2	TDET1	Tone Detect (Channel 1)
3	TDET2	Tone Detect (Channel 2)
4	–	Not Used
5	–	Not Used
6	–	Not Used
7	–	Not Used

Bit 0 CAD1 Cable between LNB and the LNB head is disconnected. When cable disconnect test mode is applied, the LNB linear regulator is disabled and a 1 mA current source is applied between the BOOST1 and LNB1 output. If the LNB volts rise above 21 V, CAD1 will be set to 1. The CAD1 bit is reset if the LNB volts drop below 19.95 V.

Bit 1 CAD2 See description for CAD1. This indicates status for channel 2.

Bit 2 TDET1 Tone Detect. When tone is enabled by whatever option, or if a tone signal is received from the LNB, TDET1 will be set to 1 if the tone appears at the LNB1 output. When the tone is disabled and no tone is received from the LNB, TDET1 is reset.

Bit 3 TDET2 See description for CAD1. This indicates status for channel 2.

Bits 4 to 7 Not used.

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Table 8. Component Selection Table[a]

Component	Characteristics	Manufacturer and Device
C3	220 nF, 10 V_{MIN}, X5R or X7R, 0402 or 0603	
C8, C9[b], C12[b]	220 nF, 50 V, X5R or X7R, 0805	
C1, C4	100 nF, 50 V, X5R or X7R, 0603	
C2, C5	100 µF, 35 V_{MIN}, ESR < 75 mΩ, I_{RIPPLE} > 500 mA	ChemiCon: EKZE500ELL101MHB5D Nichicon: UHC1V101MPT Panasonic: EEU-FM1H101B
C7	22 nF, 10 V_{MIN}, X5R or X7R, 0402 or 0603	
C10, C13	10 nF, 50 V, X5R or X7R, 0402 or 0603	
C11	0.68 µF, 25 V_{MIN}, X5R or X7R, 0805	TDK: C2012X5R1E684K Murata: GRM21BR71E684KA88 Kemet: C0805C684K3PAC AVX: 08053D684KAT2A
C6	1.0 µF, 25 V_{MIN}, X5R or X7R, 1206	TDK: C3216X7R1E105K Murata: GRM31MR71E105KA01 Taiyo Yuden: TMK316BJ105KL-T Kemet: C1206C105K3RACTU
D1, D2, D3	Schottky diode, 40 V, 1 A, SOD-123	Diodes, Inc.: B140HW-7 Central Semi: CMMSH1-40
D4	TVS, 20 V_{RM}, 32 V_{CL} at 500 A (8/20 µs), 3000 W	Littelfuse: SMDJ20A ST: LNBTVS6-221S
L1	33 µH, I_{SAT} > 1.3 A, DCR < 130 mΩ	TDK: TSL0808RA-330K1R4-PF Taiyo Yuden: LHLC08TB330K Coilcraft: DR0608-333L
L2	220 µH, I_{SAT} > 0.5 A, DCR < 0.8 Ω	TDK: TSL0808RA-221KR54-PF Taiyo Yuden: LHLC08TB221K Coilcraft: DR0608-224L
L3	1 µH, 1 A, DCR < 120 mΩ, 1206	Kemet: LB3218-T1R0MK Murata: LQM31PN1R0M00L Taiyo Yuden: LB3218T1R0M TDK: MLP3216S1R0L
R1 to R5	Determined by V_{DD}, bus capacitance, etc.	
R6	15 Ω, 1%, $^1/_8$ W	
R7	100 Ω, 1%, $^1/_8$ W	
R8	30 Ω, 1%, $^1/_8$ W	

[a]Components for channel 1 and channel 2 are identical.
[b]Either C9 or C12 are used, but not both.

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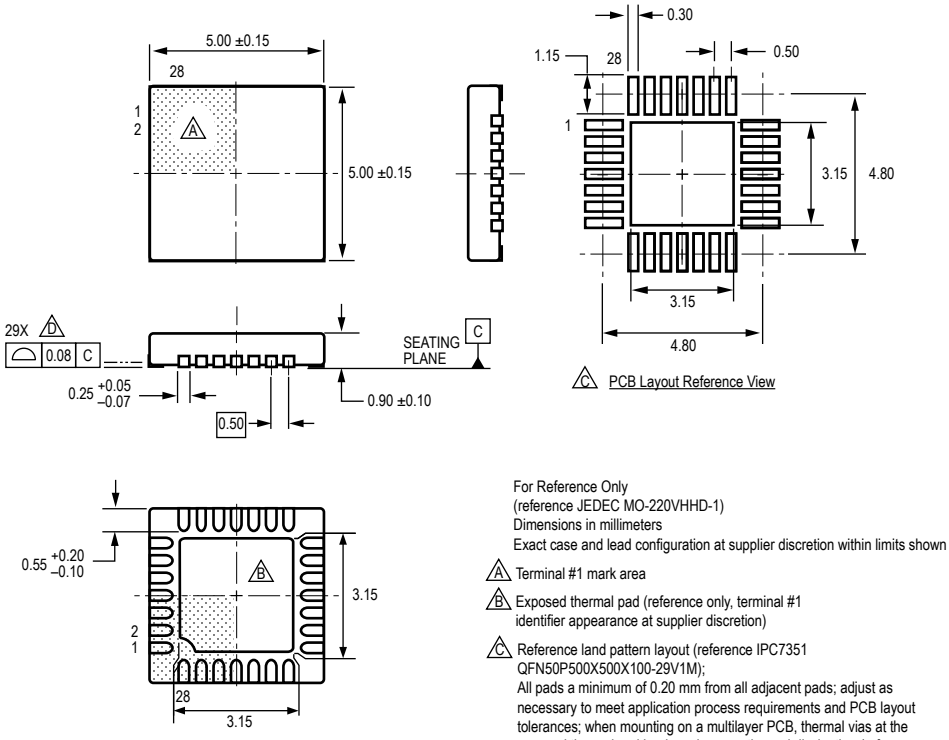
Package ET 28-Pin MLP/QFN



For Reference Only
(reference JEDEC MO-220VHHD-1)
Dimensions in millimeters
Exact case and lead configuration at supplier discretion within limits shown

A Terminal #1 mark area

B Exposed thermal pad (reference only, terminal #1 identifier appearance at supplier discretion)

C Reference land pattern layout (reference IPC7351 QFN50P500X500X100-29V1M);
All pads a minimum of 0.20 mm from all adjacent pads; adjust as necessary to meet application process requirements and PCB layout tolerances; when mounting on a multilayer PCB, thermal vias at the exposed thermal pad land can improve thermal dissipation (reference EIA/JEDEC Standard JESD51-5)

D Coplanarity includes exposed thermal pad and terminals

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Revision History

Revision	Revision Date	Description of Revision
Rev. 15	February 15, 2012	Updated Absolute Maximum Ratings
Rev. 16	January 4, 2018	Updated product status to Last-Time Buy
Rev. 17	January 14, 2019	Updated product status to Discontinued
Rev. 18	January 20, 2020	Minor editorial updates

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