



Two Outputs Clock Generator

AK8146B

Features

- Pin Selectable External Input
 - 74.17582MHz
 - 74.25MHz
 - 60MHz
- Clock out Frequencies:
 - 12.000MHz
 - 13.5MHz
- Low Jitter Performance
 - Period Jitter
 - 125 psec (max) at CLK1
 - 205 psec (max) at CLK2
- Low Current Consumption:
 - 5.0mA (Typ.) at 3.0V
- Supply Voltage:
 - 2.7 – 3.3V
- Operating Temperature Range:
 - 20 to +85°C
- Package:
 - 8-pin USON (Lead free) 2.2mm x 2.2mm

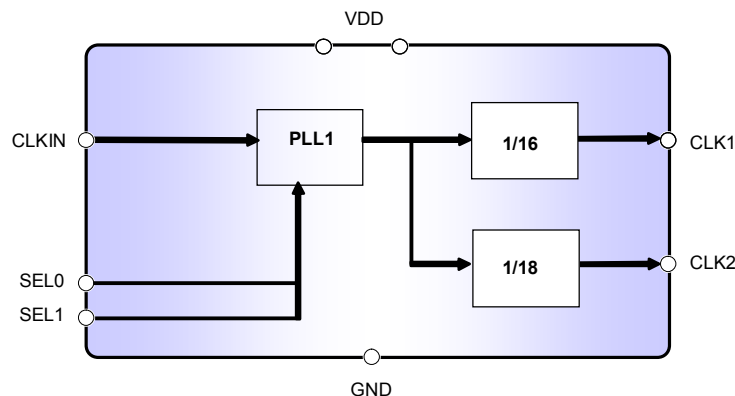
Description

The AK8146B is a low power multi clock generator which generates different frequency clocks from an external clock input. It provides two outputs of 12MHz and 13.5MHz. PLL in AK8146B are derived from AKEMD's long-term-experienced clock device technology, and enable clock output to perform low jitter and to operate with very low current consumption. The AK8146B is available in a 8-pin USON package.

Applications

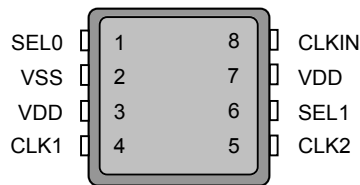
- Digital Video Camera

Block Diagram



AK8146B Multi Clock Generator

Pin Descriptions



Package: 8-Pin USON(Top View)

Pin No.	Pin Name	Pin Type	Description
1	SEL0	IN	SEL0 and SEL1 pins select the external clock frequency from among 74.17582MHz, 74.25MHz and 60MHz. Please refer to the table of External clock frequency selection" shown below.
2	GND	PWR	Ground
3	VDD	PWR	Power
4	CLK1	OUT	12.0 MHz clock output
5	CLK2	OUT	13.5 MHz clock output
6	SEL1	IN	External clock frequency selection pin. Same as SEL0.
7	VDD	PWR	Power
8	CLKIN	IN	External clock input pin. It accepts one of the four frequencies selected by SEL0 and SEL1.

SEL1	SEL0	Input Frequency
0	0	74.17582MHz (=74.25 MHz/1.001)
0	1	74.25 MHz
1	0	Not in use
1	1	60.0 MHz

Ordering Information

Part Number	Marking	Shipping Packaging	Package	Temperature Range
AK8146B	146B	Tape and Reel	8-pin USON	-20 to 85 °C

Absolute Maximum Rating

Over operating free-air temperature range unless otherwise noted ⁽¹⁾

Items	Symbol	Ratings	Unit
Supply voltage	VDD	-0.3 to 4.6	V
Input voltage	V _{in}	VSS-0.3 to VDD+0.3	V
Input current (any pins except supplies)	I _{IN}	±10	mA
Storage temperature	Tstg	-55 to 130	°C

Note

(1) Stress beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated under “Recommended Operating Conditions” is not implied. Exposure to absolute-maximum-rating conditions for extended periods may affect device reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.



ESD Sensitive Device

This device is manufactured on a CMOS process, therefore, generically susceptible to damage by excessive static voltage. Failure to observe proper handling and installation procedures can cause damage. AKEMD recommends that this device is handled with appropriate precautions.

Recommended Operation Conditions

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Operating temperature	T _a		-20		85	°C
Supply voltage ⁽¹⁾	VDD		2.7	3.0	3.3	V
Output Load Capacitance	C _{p1}	Pin: CLK1,CLK2			15	pF

Note:

(1) Power to VDD requires to be supplied from a single source. A decoupling capacitor of 0.1μF for power supply line should be installed close to each VDD pin.

DC Characteristics

All specifications at VDD: over 2.7 to 3.3V, Ta: -20 to +85°C, unless otherwise noted

Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit
High Level Input Voltage	V_{IH}	Pin: SEL0 SEL1	0.7*VDD			V
Low Level Input Voltage	V_{IL}	Pin: SEL0 SEL1			0.3*VDD	V
Input Leakage Current	I_L	Pin: SEL0 SEL1	-10		+10	μ A
High Level Output Voltage 1	V_{OH}	Pin: CLK1, CLK2 $I_{OH}=-4.0mA$	0.8VDD			V
Low level Output Voltage 1	V_{OL}	Pin: CLK1, CLK2 $I_{OL}=+4.0mA$			0.2VDD	V
High Level Output Voltage 2	V_{OH}	Pin: CLK1, CLK2 $I_{OH}=-1.5mA$	0.9VDD			V
Low level Output Voltage 2	V_{OL}	Pin: CLK1, CLK2 $I_{OL}=+0.1mA$			0.05VDD	V
Current Consumption	I_{DD}	No load, CLKIN=74.25MHz TYP case is VDD=3.0V, Ta=25°C		5.0	6.4	mA

AC Characteristics

All specifications at VDD: over 2.7 to 3.3V, Ta: over -20 to +85°C, unless otherwise noted

Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit
External Clock Input		Pin: CLKIN		74.17582 74.25 60.0		MHz
External Clock Input		Pin: CLKIN	0.7			Vpp
External Clock Duty		Pin: CLKIN, Specified at 0.5*Clock Amplitude	30		70	%
Period Jitter ⁽¹⁾⁽²⁾		Pin: CLK1			125	ps
		Pin: CLK2			205	ps
Output Clock Duty Cycle ⁽¹⁾		Pin: CLK1	45	50	55	%
Output Clock Rise Time ⁽¹⁾	t_{rise}	Pin: CLK1, CLK2 Cp1=15pF			4.0	ns
Output Clock Fall Time ⁽¹⁾	t_{fall}	Pin: CLK1, CLK2 Cp1=15pF			4.0	ns
Power-up Time ⁽³⁾		Pin: CLK1 Cp1=15pF		1.4	2.8	ms

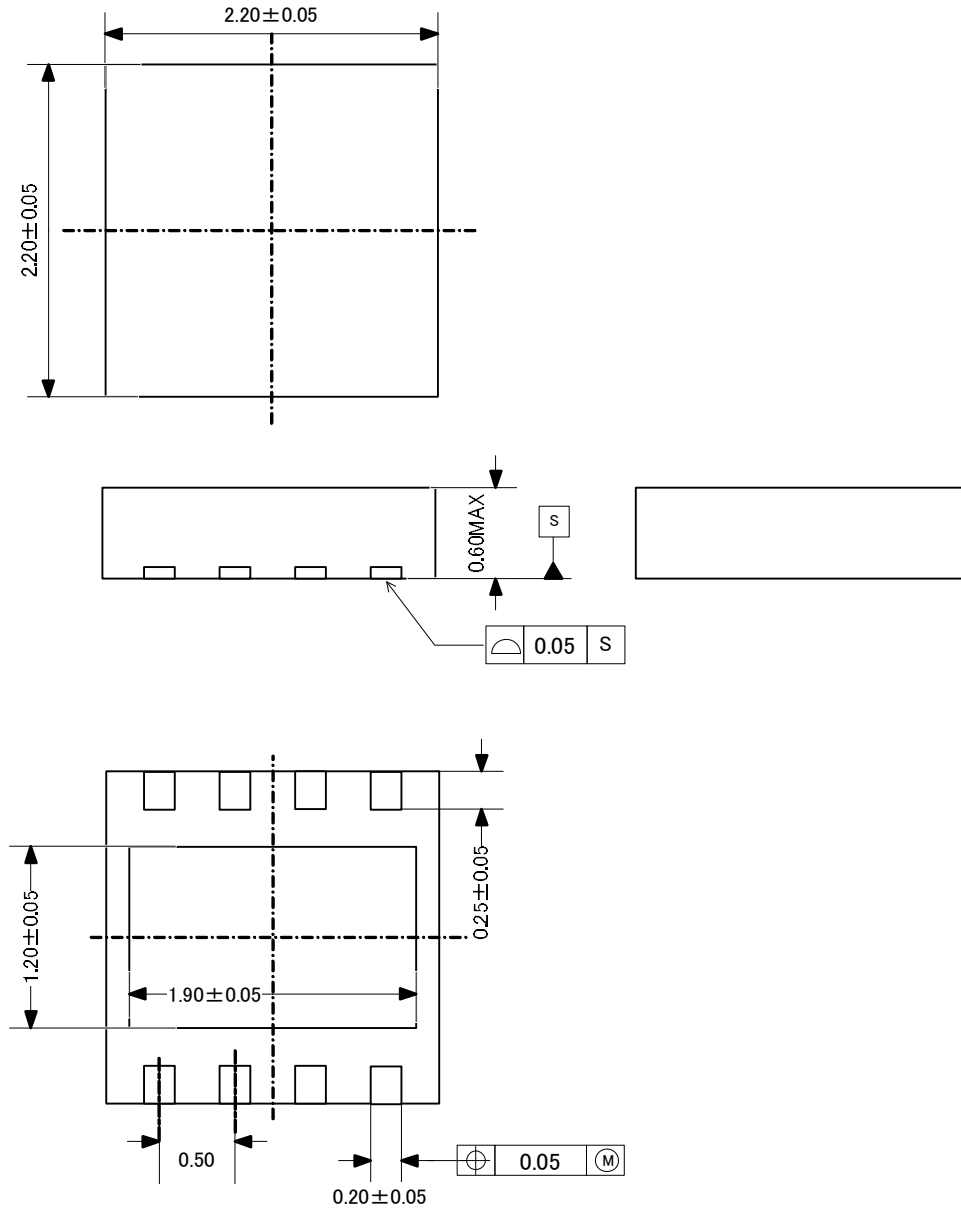
(1) Design Value

(2) 5sigma in 10000 sampling

(3) The time that output reaches the target frequency within accuracy of $\pm 100ppm$ from the point that the power supply reaches VDD

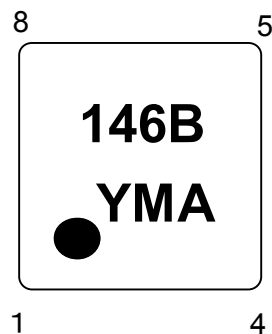
Package Information

• Mechanical data



• Marking

- a: #1 Pin Index : Circle
- b: Part number : 146B
- c: Date code (3 digits) : YMA



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