







10Gbps, 2-Port, USB 3.1 Mux/Demux ReDriver™

### **Features**

### ReDriver

- → 10Gbps Serial Link with Linear Equalizer
- → Full Compliancy to USB 3.1 Gen-2 and Gen-1 Super-Speed Standard
- → 1-to-2 DeMux from Host Tx to Device Rx
- → 2-to-1 Mux from Device Tx to Host Rx
- → Adjustable-Output Linear Swing, Flat Gain and Equalization via I2C or Pin Control
- → 100Ω Differential CML I/Os
- → Automatic Receiver Detect
- → Auto "Slumber" Mode for Adaptive Power Management
- → Supply Voltage 3.3V
- → Temperature Range: -40°C to 70°C
- → Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)
- → Halogen and Antimony Free. "Green" Device (Note 3)
- → Packaging (Pb-free & Green):
  - 40-contact, ZLC40 (TQFN)

## **Applications**

- → Notebooks
- → Mobile Phones
- **→** Tablets
- → Docking Station

## **Description**

PI3EQX10612 is a low-power, high-performance 10Gbps 2-Port USB 3.1 Gen-2/Gen-1 Mux/DeMux ReDriver.

### The Two-Port Mux/Demux ReDriver

The ReDriver provides programmable equalization, swing, and flat gain to optimize performance over a variety of physical mediums by reducing intersymbol interference. The ReDriver supports two  $100\Omega$  differential CML data I/Os between the Protocol ASIC to a switch fabric, overcable, or to extend the signals across other distant data pathways on the user's platform.

The integrated equalization circuitry provides flexibility with signal integrity of the signal before the ReDriver. A low-level input-signal detection and output-squelch function is provided for each channel. Each channel operates fully independently. The channels' input-signal level determines whether the output is active.

The ReDriver also includes an adaptive power management feature to maximize battery life for power-sensitive consumer devices.

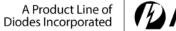
### Notes:

1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.

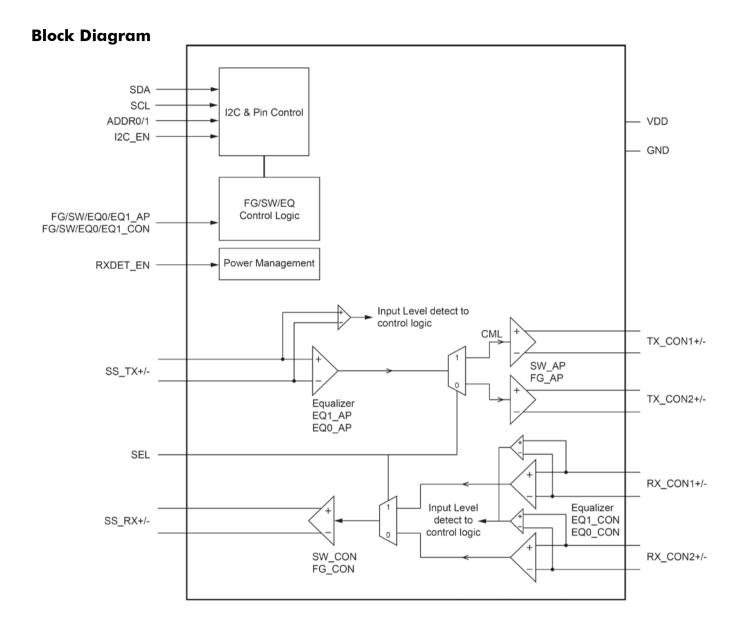
2. See https://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.

3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.





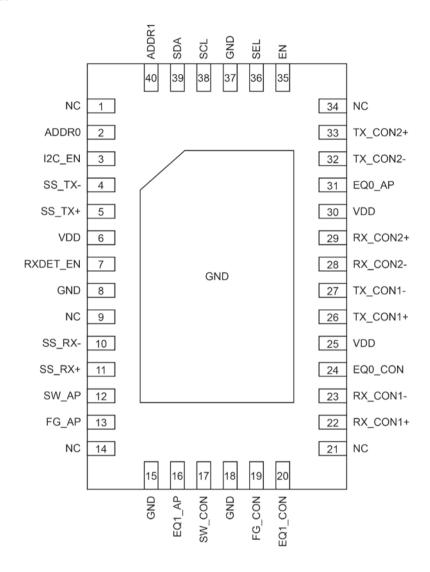








# **Pin Configuration**



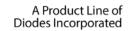




**Pin Descriptions** 

Pin #	Pin Name	I/O	Description
Thermal PAD, 8, 15,18,37	GND	Ground	Ground pin. Thermal pad.
2, 40	ADDR0, ADDR1	I	Input pins to indicate I2C address: Refer to I2C Slave Address table.
3	I2C_EN	I	Input pin to enable I2C mode
5,4 22,23 29,28	SS_TX+, SS_TX-, RX_CON1+, RX_CON1-, RX_CON2+, RX_CON2-	I	Input terminals. Selectable input termination between $50\Omega$ to VDD, $75k\Omega$ to VbiasRX, or $75k\Omega$ to GND.
6,25,30	VDD	Power	Dedicated 3.3V power supply.
7	RXDET_EN	I	ReDriver loading detection enable pin.  1 = ReDriver loading detection enabled (default setting in application)  0 = ReDriver loading detection disabled
11,10 26,27 33,32	SS_RX+,SS_RX-, TX_CON1+,TX_CON1-, TX_CON2+, TX_CON2-	0	Output terminals. Selectable output termination between $50\Omega$ to VbiasTx, $6k\Omega$ to VbiasTx, $75k\Omega$ to VbiasTx, and $75k\Omega$ to GND.
12,13,16,31	SW_AP FG_AP EQ1_AP, EQ0_AP	I	SW/FG/EQ setup for USB channels with receiver terminal is connected to AP side.
17,19,20,24	SW_CON FG_CON EQ1_CON, EQ0_CON	I	SW/FG/EQ setup for USB channels with receiver terminal is connected to connector side.
35	EN	I	Active-high enable input pin (with internal weak pull high).  EN=GND — disabled/low power state  EN=VDD — enabled/active state
36	SEL	I	Input pin to select USB channel.
38	SCL	I	I2C communication clk signal.
39	SDA	I/O	I2C communication data signal.
1,9,14,21,34	NC	_	No connection.







**Maximum Ratings** 

Storage Temperature	-65 to 150	$^{\circ}$ C
Supply Voltage	-0.5 to 3.8	V
Voltage of 3.3V IO pins (SCL, SDA, RXDET_EN, ADDR0/1, SEL, EN, SW_AP,FG_AP,EQ1_AP, EQ0_AP,SW_CON,FG_CON,EQ1_CON,EQ0_CON)	-0.5 to VDD+0.5	V
Voltage of SS_TX+/-,SS_RX+/-,TX_CON1/2 +/-, RX_CON1/2 +/-	-0.5 to VDD+0.5	V
Sink Current from SDA	10	mA
Continuous Input Current to SS_TX+/-, RX_CON1/2 +/-	±30	mA
ESD (HBM)	2	KV

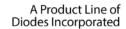
### Note:

Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

**Recommended Operation Conditions** 

Symbol	Parameter	Min.	Max.	Units
$V_{DD}$	Supply Voltage	3.0	3.6	V
V <sub>IO</sub>	Voltage of IO pins (SCL, SDA, RXDET_EN, ADDR0/1, SEL, EN, SW_AP,FG_AP, EQ1_AP, EQ0_AP,SW_CON,FG_CON, EQ1_CON,EQ0_CON)	0	3.6	V
V <sub>TXRX</sub>	Voltage of SS_TX+/-,SS_RX+/-,TX_CON1/2 +/-, RX_CON1/2 +/-	0	3.6	V
V <sub>NOISE</sub>	Supply Noise up to 50MHz	_	100	mVpp
$T_A$	Operating Temperature	-40	70	°C







## **ReDriver AC/DC Electrical Characteristics**

**Power Consumption (VDD)** 

Symbol	Parameter	Conditions	Min.	Тур.	Max.	Units
$I_{PD}$	Typical Pin Power-Down Current	EN=0	_	26	100	μΑ
$I_{DDQ\_PD}$	I2C Power-Down Current	EN=1 I2C Byte4<7:4>=1111	_	_	340	μA
USB 3.1 Ge	n 2 Mode	-				
$I_{U0}$	Current in USB U0 Mode	EN=1, USB U0 mode	_	80	112	mA
$I_{U1}$	Current in USB U1 Mode	EN=1, USB U1 mode	_	16	20	mA
I <sub>U2/U3</sub>	Current in USB U2/U3 Mode	EN=1, USB U2/U3 mode	_	0.5	0.6	mA
I <sub>RXDET</sub>	Current RXDET Mode	EN=1, RXDET mode	_	0.5	0.6	mA
Four-Level	Control Pins (FG_AP, FG_CON, EQ	1_AP, EQ0_AP, EQ1_CON,E	Q0_CON, SW_	AP, SW_CON	)	
$V_{\mathrm{IH}}$	DC-Input Logic High	_	0.92 × VDD	VDD		V
$V_{ m IF}$	DC-Input Logic "Float"	_	$0.59 \times VDD$	$0.67 \times VDD$	$0.75 \times VDD$	V
$V_{IR}$	DC-Input Logic with Rext to GND	_	0.25 × VDD	0.33 × VDD	0.41 × VDD	V
$V_{ m IL}$	DC-Input Logic Low	_	_	GND	$0.08 \times VDD$	V
$I_{\mathrm{IH}}$	Input-High Current	_	_	_	50	μA
$I_{\mathrm{IL}}$	Input-Low Current	_	-75	_	_	μA
Rext	External Resistance Connects to GND (±5%)	_	64.6	68	71.4	kΩ
Two-Level	Control Pins (EN, SEL, ADDR0/1, R	XDET_EN)				
$V_{\mathrm{IH}}$	DC-Input Logic High	_	2.0	_	_	V
$V_{ m IL}$	DC-Input Logic Low	_	_	_	0.8	V
I <sub>IH</sub>	Input-High Current	_	_	_	25	μA
$I_{ m IL}$	Input-Low Current	_	-25	_	_	μA
I2C Interfac	e Pins (SCL, SDA)		•	•	•	
$V_{\mathrm{IH}}$	DC-Input Logic High	_	1.1	_	_	V
$V_{ m IL}$	DC-Input Logic Low		_	_	0.4	V

## **USB Differential Channel**

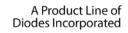
Symbol	Parameter	Conditions	Min.	Тур.	Max.	Units
USB Differential	Input	•				
C <sub>RXPARASITIC</sub>	Parasitic Capacitor for RX	_	_	_	1.0	pF
R <sub>RX-DIFF-DC</sub>	DC Differential Input Impedance	_	72	_	120	Ω
R <sub>RX-SINGLE-DC</sub>	DC Single-ended Input Impedance	DC impedance limits are required to guarantee RxDet. Measured with respect to GND over a voltage of 500mV max.	18	_	30	Ω
$Z_{RX ext{-HIZ-DC-PD}}$	DC Input CM Input Impedance for V>0 During Reset or Power Down	(Vcm=0 to 500mV)	25	_	_	kΩ
C <sub>AC COUPLING</sub>	AC-Coupling Capacitance	_	75	_	265	nF
V <sub>RX-CM-AC-P</sub>	Common-Mode Peak Voltage	AV up to 5GHz	_	_	150	mVpeak
V <sub>RX-CM-DC-Active-</sub> Idle-Delta-P	Common-Mode Peak Voltage	Between U0 and U1, Ac up to 5GHz	_	_	200	mVpeak
USB Differential	Output					
V <sub>TX-DIFF-PP</sub>	Output Differential p-p Voltage Swing	Differential Swing  V <sub>TX-D+</sub> -V <sub>TX-D-</sub>	_	_	1.2	Vppd
R <sub>TX-DIFF-DC</sub>	DC Differential TX Impedance		72	_	120	Ω
V <sub>TX-RCV-DET</sub>	Amount of Voltage Change Allowed During RxDet	_	_	_	600	mV





Symbol	Parameter	Conditions	Min.	Тур.	Max.	Units	
Cac coupling	AC-Coupling Capacitance	_	75	_	265	nF	
T <sub>TX-EYE(10Gbps)</sub>	Transmitter eye, Include all Jitter	At the silicon pad, 10Gbps	0.646	_		UI	
T <sub>TX-EYE(5Gbps)</sub>	Transmitter eye, Include all jitter	At the silicon pad, 5Gbps	0.625	_		UI	
$T_{TX\text{-DJ-DD}(10Gbps)}$	Transmitter Deterministic Jitter	At the silicon pad, 10Gbps		_	0.17	UI	
T <sub>TX-DJ-DD(5Gbps)</sub>	Transmitter Deterministic Jitter	At the silicon pad, 5Gbps		_	0.205	UI	
C <sub>TXPARASITIC</sub>	Parasitic Capacitor for TX			_	1.1	pF	
R <sub>TX-DC-CM</sub>	Common Mode DC Output Impedance	_	18	_	30	Ω	
$V_{TX ext{-}DC ext{-}CM}$	Instantaneous-Allowed DC Common-Mode Voltage at the Connector Side of the AC-Coupling Capacitors	V <sub>TX-D+</sub> +V <sub>TX-D-</sub>  /2	0	_	2.2	V	
V <sub>TX-C</sub>	Common-Mode Voltage	$ V_{TX-D+}+V_{TX-D-} /2$	VDD-2	_	VDD	V	
V <sub>TX-CM-AC-PP-</sub> Active	Active-Mode TX AC Common- Mode Voltage	$V_{TX-D_+}+V_{TX-D}$ for both time and amplitude	_	_	100	mVpp	
$ m V_{TX\text{-}CM\text{-}DC\text{-}}$ Active_Idle-Delta	Common-Mode Delta Voltage $\begin{aligned} & Avg_{uo}( V_{TEX-D+}+V_{TX-D-} )/2-\\ &Avg_{u1}( V_{TX-D+}+V_{TX-D-} )/2  \end{aligned}$	Between U0 to U1	l	_	200	mV-peak	
$V_{TX ext{-Idle-Diff-AC-pp}}$	Idle-Mode AC Common-Mode Delta Voltage  V <sub>TX-D+</sub> -V <sub>TX-D-</sub>	Between Tx+ and Tx- in idle mode. Use the HPF to remove DC components. =1/LPF. No AC and DC signals are applied to Rx terminals.	_	_	10	mVppd	
$V_{ ext{TX-Idle-Diff-DC}}$	Idle-Mode DC Common-Mode Delta Voltage $ V_{TX-D+}-V_{TX-D-} $	Between Tx+ and Tx- in idle mode. Use the LPF to remove DC components. =1/HPF. No AC and DC signals are applied to Rx terminals.	_	_	10	mV	
$G_p$	Peaking Gain (Compensation at 5GHz, Relative to 100MHz, 100mV <sub>p-p</sub> Sine Wave Input)	EQ<3:0>=0000 EQ<3:0>=0101 EQ<3:0>=1010 EQ<3:0>=1111	_	6.42 9.5 11.77 13.54	_	dB	
	rr .	Variation around typical	-3		+3	dB	
$G_{\rm F}$	Flat Gain (100MHz, EQ<3:0>=0000, SW<1:0>=01)	FG<1:0>=00 FG<1:0>=01 FG<1:0>=10 FG<1:0>=11	_	-2.07 -0.24 +0.62 +1.77	_	dB	
		Variation around typical	-3	_	+3	dB	
$V_{\rm SW\_100M}$	-1dB Compression Point Output Swing (at 100MHz)	SW<1:0>=00 SW<1:0>=01	<u> </u>	900 1000		mVppd	
$V_{\rm SW\_5G}$	-1dB Compression Point Output Swing (at 5GHz)	SW<1:0>=00 SW<1:0>=01	_	600 750	_	mVppd	
DD <sub>NEXT</sub> Note3	Differential Near-End Crosstalk	100MHz to 5GHz		-45	_	dB	
DD <sub>FEXT</sub> Note3	Differential Far-End Crosstalk	100MHz to 5GHz		-45	_	dB	
	Input-Referred Noise <sup>(2)</sup>	100MHz to 5GHz, FG<1:0>=11, EQ<3:0>=0000, SW<1:0>=01	_	0.6	_	mV	
V <sub>NOISE-INPUT</sub>	input-keierrea ivoise	100MHz to 5GHz, FG<1:0>=11, EQ<3:0>=1111, SW<1:0>=01	to 5GHz, =11, =1111, — 0.5			- mV <sub>RMS</sub>	







Symbol	Parameter	Conditions	Min.	Тур.	Max.	Units
V	Outside Defermed Nation (2)	100MHz to 5GHz, FG<1:0>=11, EQ<3:0>=0000, SW<1:0>=01	_	0.8	_	$mV_{RMS}$
V <sub>NOISE-OUTPUT</sub>	Output-Referred Noise <sup>(2)</sup>	100MHz to 5GHz, FG<1:0>=11, EQ<3:0>=1111, SW<1:0>=01	_	1	_	$mV_{RMS}$
S11	Input Datum Laga	10 MHz to 4.1 GHz differential	_	-13.0	-5.0 —	
511	Input-Return Loss	1 GHz to 4.1 GHz common mode	_	-5.0	_	dB
Gaa.	Output Detum Loss	10 MHz to 4.1 GHz differential	_	-15	_	dB
S22	Output-Return Loss	1 GHz to 4.1 GHz common mode		-6.0	_	dB
Signal and Freq	uency Detectors					
$ m V_{TH\_UPM}$	Unplug-Mode Detector Threshold	Threshold of LFPS when the input impedance of the ReDriver is $67k\Omega$ to VbiasRx only. Used in the unplug mode.	200	_	800	mVppd
V <sub>TH_DSM</sub>	Deep-Slumber Mode Detector Threshold	LFPS signal threshold in deep-slumber mode	100	_	600	mVppd
V <sub>TH_AM</sub>	Active-Mode Detector Threshold	Signal threshold in active and slumber mode	65	_	175	mVppd
$F_{TH}$	LFPS Frequency Detector	Detect the frequency of the input CLK pattern	100	_	400	MHz
T <sub>ON UPM</sub>	Turn-on of Unplug Mode	TX pin-to-RX pin latency	_		3	ms
T <sub>ON DSM</sub>	Turn-on of Deep Slumber Mode	when input signal is LFPS	_		5	μs
T <sub>ON SM</sub>	Turn-on of Slumber Mode	"Ten input signal is El I s		_	20	ns

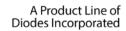
### Note:

<sup>1.</sup> Measured using a vector-network analyzer (VNA) with -15dBm power level applied to the adjacent input. The VNA detects the signal at the output of the victim channel. All other inputs and outputs are terminated with  $50\Omega$ .

<sup>2.</sup> Guaranteed by design and characterization.

<sup>3.</sup> Subtract the Channel Gain from the Total Gain to get the Actual Crosstalk.





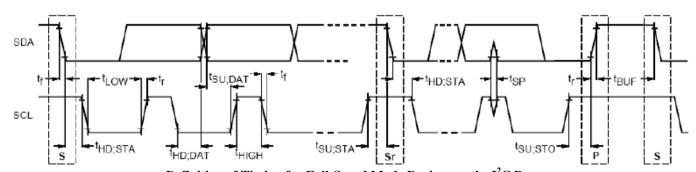


### I<sup>2</sup>C AC Electrical Characteristics

Symbol	Parameter	Standard Mode I <sup>2</sup> C		Fast Mode I <sup>2</sup> C		Fast Mod	Unit	
Symbol	1 at affecter	Min	Max	Min	Max	Min	Max	Omt
$f_{SCL}$	SCL Clock Frequency	0	100	0	400	0	1000	kHz
$t_{\mathrm{BUF}}$	Bus Free Time Between a STOP and START Condition	4.7	_	1.3	_	0.5	_	μs
t <sub>HD;STA</sub>	Hold Time (Repeated) START Condition	4.0	_	0.6	_	0.26	_	μs
$t_{SU;STA}$	Setup Time for a Repeated START Condition	4.7	_	0.6	_	0.26	_	μs
$t_{\rm SU;STO}$	Setup Time for STOP Condition	4.0	_	0.6	_	0.26	_	μs
t <sub>VD;ACK</sub> <sup>[1]</sup>	Data Valid Acknowledge Time	_	3.45	_	0.9	_	0.45	μs
$t_{\mathrm{HD;DAT}}^{[2]}$	Data Hold Time	0	_	0	_	0	_	ns
$t_{\mathrm{VD;DAT}}$	Data Valid Time	_	3.45	_	0.9	_	0.45	ns
$t_{SU;DAT}$	Data Setup Time	250	_	100	_	50	_	ns
$t_{LOW}$	LOW Period of the SCL Clock	4.7	_	1.3	_	0.5	_	μs
$t_{HIGH}$	HIGH Period of the SCL Clock	4.0	_	0.6	_	0.26	_	μs
$t_{\mathrm{f}}$	Fall Time of Both SDA and SCL Signals	_	300	_	300		120	ns
$t_{\rm r}$	Rise Time of Both SDA and SCL Signals		1000	_	300		120	ns
$t_{SP}$	Pulse Width of Spikes that must be Suppressed by the Input Filter		50		50	_	50	ns

### Notes

2.  $C_b$  equals the total capacitance of one BUS line in pF. If mixed with high-speed devices, faster fall times are allowed according to the  $I^2$ C specification.



Definition of Timing for Full-Speed Mode Devices on the I<sup>2</sup>C Bus

A fast-mode 1<sup>2</sup>C-bus device can be used in a standard-mode 1<sup>2</sup>C-bus system, but the requirement t<sub>SETDAT</sub> ≥ 250ns must be met. This is automatically the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line tr\_max + t<sub>SETDAT</sub> = 1000 + 250 = 1250ns (according to the standard-mode 1<sup>2</sup>C bus specification) before the SCL line is released.

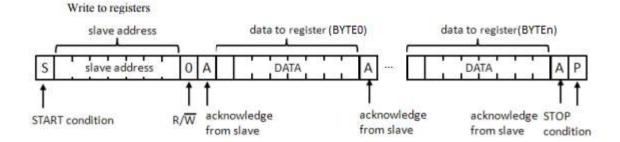


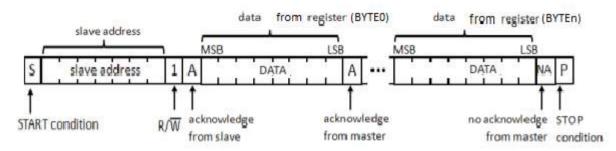


## I<sup>2</sup>C Slave Address

I2C_EN	ADDR1	ADDR0	RedriverI2C Slave Address
VDD	GND	GND	A0h
VDD	GND	VDD	A2h
VDD	VDD	GND	A4h
VDD	VDD	VDD	A6h
GND	X	X	Pin Mode

## I<sup>2</sup>C Data Transfer





\*Registers of ReDriver can be Read/Written in Bulk Mode only





# **ReDriver Detailed Description**

## **ReDriver Register Table**

Register Assignment
Bit   Type
7
6
S
4
3
2
RO
1
BYTE   (Device Type/ Device ID Register)   Bit   Type   Power-up Condition   Control Affected   Comment
Bit   Type   Power-up Condition   Control Affected   Device Type
7
Device Type
Device Type
3
A   RO
2         RO         0         Device ID         Device ID         Device ID = 0001           1         RO         0         0         0         Device ID = 0001         Device ID = 0001           BYTE 2 (Byte count Register 32 Bytes)           Bit         Type         Power-up Condition         Control Affected         Comment           7         RO         0         0         1
Device ID
1
Bit   Type   Power-up Condition   Control Affected   Comment
Bit   Type   Power-up Condition   Control Affected   Comment
Bit   Type   Power-up Condition   Control Affected   Comment
Total Price
6         RO         0           5         RO         1           4         RO         0           3         RO         0           2         RO         0           1         RO         0           0         RO         0           BYTE 3 (Channel Assignment and Receiver Detection Enable Control)           Bit         Type         Power-up Condition         Control Affected         Comment           7         R/W         0         —         Reserved           6         R/W         1         CONF<2>         Channel Assignment           4         R/W         1         CONF<<1>>         Channel Assignment           4         R/W         1         CONF<<1>>         Channel Assignment           4         R/W         1         CONF<<1>>         Channel Assignment           4         R/W         0         —         Reserved           8         R/W         0         —         RXDET_EN#         Far-end receiver detection enable/disable 0 = Enable 1 = Disable           1         R/W         1         —         Reserved           0         R/W         0         —         <
5         RO         1           4         RO         0           3         RO         0           2         RO         0           1         RO         0           0         RO         0           BYTE 3 (Channel Assignment and Receiver Detection Enable Control)           Bit         Type         Power-up Condition         Control Affected         Comment           7         R/W         0         —         Reserved           6         R/W         1         CONF<2>         Channel Assignment           4         R/W         1         CONF<0>         Channel Assignment           4         R/W         1         CONF<0>         Channel Assignment           5         R/W         0         —         Reserved           6         R/W         0         —         RXDET_EN#         Far-end receiver detection enable/disable 0 = Enable 1 = Disable           1         R/W         0         —         Reserved           BYTE 4 (Power Down Control)         Type         Power-up Condition         Control Affected         Comment           7         R/W         0         PD_CON_TX1         CONx power override
A
Register Byte count   12C byte count = 32 bytes
2         RO         0           1         RO         0           0         RO         0           BYTE 3 (Channel Assignment and Receiver Detection Enable Control)           Bit         Type         Power-up Condition         Control Affected         Comment           7         R/W         0         —         Reserved           6         R/W         1         CONF<2>         Channel Assignment           4         R/W         1         CONF<0>         Channel Assignment           3         R/W         0         —         Reserved           8         R/W         0         —         Reserved           9         R/W         0         —         Reserved           1         R/W         0         —         Reserved           8YTE 4 (Power Down Control)         Enable 1         —         Reserved           Bit         Type         Power-up Condition         Control Affected         Comment           7         R/W         0         PD_CON_TX1         Only represention
1 RO 0         0 RO 0           BYTE 3 (Channel Assignment and Receiver Detection Enable Control)           Bit Type Power-up Condition Control Affected Comment           7 R/W 0 — Reserved           6 R/W 1 CONF         CONF           5 R/W 0 CONF         CONF           4 R/W 1 CONF         CONF           3 R/W 0 — Reserved         RXDET_EN pin=1; 1 if RXDET_EN pin=1; 1 if RXDET_EN pin=0         Far-end receiver detection enable/disable 0 = Enable 1 = Disable           1 R/W 1 — Reserved         Reserved           0 R/W 0 — Reserved         Reserved           BYTE 4 (Power Down Control)         Control Affected         Comment           7 R/W 0 PD_CON_Rx1         CONx power override           6 R/W 0 PD_CON_Tx1         O Normal operation
BYTE 3 (Channel Assignment and Receiver Detection Enable Control)           Bit         Type         Power-up Condition         Control Affected         Comment           7         R/W         0         —         Reserved           6         R/W         1         CONF<2>         Channel Assignment           5         R/W         0         CONF<1>         Channel Assignment           4         R/W         1         CONF<0>         Control Affected           3         R/W         0         —         RXDET_EN#         Far-end receiver detection enable/disable 0 = Enable 1 = Disable           1         R/W         1         —         Reserved           0         R/W         0         —         Reserved           BYTE 4 (Power Down Control)         Control Affected         Comment           7         R/W         0         PD_CON_Rx1         CONx power override           6         R/W         0         PD_CON_Tx1         CONx power override
BYTE 3 (Channel Assignment and Receiver Detection Enable Control)           Bit         Type         Power-up Condition         Control Affected         Comment           7         R/W         0         —         Reserved           6         R/W         1         CONF<2>         Channel Assignment           5         R/W         0         CONF<1>         Channel Assignment           4         R/W         1         CONF<0>         Control Affected           3         R/W         0         —         Reserved           4         R/W         0 if RXDET_EN pin=1; 1 if RXDET_EN pin=0; 1 if RXDET_EN pin=0         Far-end receiver detection enable/disable 0 = Enable 1 = Disable           1         R/W         0         —         Reserved           BYTE 4 (Power Down Control)         —         Reserved         Comment           7         R/W         0         PD_CON_Rx1         CONx power override           6         R/W         0         PD_CON_Tx1         O_Normal operation
Bit         Type         Power-up Condition         Control Affected         Comment           7         R/W         0         —         Reserved           6         R/W         1         CONF<2>         Channel Assignment           5         R/W         0         CONF<0>         Channel Assignment           4         R/W         1         CONF<0>         Channel Assignment           3         R/W         0         —         Reserved           8         R/W         0 if RXDET_EN pin=1; 1 if RXDET_EN pin=0         Far-end receiver detection enable/disable 0 = Enable 1 = Disable           1         R/W         1         —         Reserved           BYTE 4 (Power Down Control)         —         Reserved           Bit         Type         Power-up Condition         Control Affected         Comment           7         R/W         0         PD_CON_Rx1         CONx power override           6         R/W         0         PD_CON_Tx1         O. Normal operation
7         R/W         0         —         Reserved           6         R/W         1         CONF<2>         Channel Assignment           5         R/W         0         CONF<0>         Channel Assignment           4         R/W         1         CONF<0>         Reserved           3         R/W         0         —         RXDET_EN#         Far-end receiver detection enable/disable to a part of the control o
6         R/W         1         CONF<2>           5         R/W         0         CONF<1>         Channel Assignment           4         R/W         1         CONF<0>         Reserved           3         R/W         0         —         RXDET_EN#         Far-end receiver detection enable/disable 0 = Enable 1 = Disable           1         R/W         1         —         Reserved           0         R/W         0         —         Reserved           BYTE 4 (Power Down Control)         Control Affected         Comment           7         R/W         0         PD_CON_Rx1         CONx power override           6         R/W         0         PD_CON_Tx1         CONx power override
5         R/W         0         CONF<1>         Channel Assignment           4         R/W         1         CONF<0>         Reserved           3         R/W         0         —         Reserved           2         R/W         0 if RXDET_EN pin=1; 1 if RXDET_EN pin=0         Far-end receiver detection enable/disable 0 = Enable 1 = Disable           1         R/W         1         —         Reserved           0         R/W         0         —         Reserved           BYTE 4 (Power Down Control)         Control Affected         Comment           7         R/W         0         PD_CON_Rx1         CONx power override           6         R/W         0         PD_CON_Tx1         On Normal operation
4         R/W         1         CONF<0>           3         R/W         0         —         Reserved           2         R/W         0 if RXDET_EN pin=1; 1 if RXDET_EN pin=0; 1 if RXDET_EN pin=0         Far-end receiver detection enable/disable 0 = Enable 1 = Disable           1         R/W         1         —         Reserved           0         R/W         0         —         Reserved           BYTE 4 (Power Down Control)           Bit         Type         Power-up Condition         Control Affected         Comment           7         R/W         0         PD_CON_Rx1         CONx power override           6         R/W         0         PD_CON_Tx1         O Normal operation
3         R/W         0         —         Reserved           2         R/W         0 if RXDET_EN pin=1; 1 if RXDET_EN pin=0         Far-end receiver detection enable/disable 0 = Enable 1 = Disable           1         R/W         1         —         Reserved           0         R/W         0         —         Reserved           BYTE 4 (Power Down Control)         Enable 1 = Disable
2         R/W         0 if RXDET_EN pin=1; 1 if RXDET_EN pin=0         RXDET_EN#         Far-end receiver detection enable/disable 0 = Enable 1 = Disable 1 = Disable 1 = Disable 1 = Disable 0 = Reserved 0 =
2       R/W       0 if RXDET_EN pin=1; 1 if RXDET_EN pin=0       0 = Enable 1 = Disable         1       R/W       1       —       Reserved         0       R/W       0       —       Reserved         BYTE 4 (Power Down Control)         Bit       Type       Power-up Condition       Control Affected       Comment         7       R/W       0       PD_CON_Rx1       CONx power override         6       R/W       0       PD_CON_Tx1       O Normal operation
2   R/W   1 if RXDET_EN pin=0   0 = Enable   1 = Disable   1 = Disable   1 = Reserved   0   R/W   0
1         R/W         1         —         Reserved           0         R/W         0         —         Reserved           BYTE 4 (Power Down Control)           Bit         Type         Power-up Condition         Control Affected         Comment           7         R/W         0         PD_CON_Rx1         CONx power override           6         R/W         0         PD_CON_Tx1         0         Normal operation
0         R/W         0         —         Reserved           BYTE 4 (Power Down Control)           Bit         Type         Power-up Condition         Control Affected         Comment           7         R/W         0         PD_CON_Rx1         CONx power override           6         R/W         0         PD_CON_Tx1         0         Normal operation
BYTE 4 (Power Down Control)           Bit         Type         Power-up Condition         Control Affected         Comment           7         R/W         0         PD_CON_Rx1         CONx power override           6         R/W         0         PD_CON_Tx1         0         Normal operation
Bit         Type         Power-up Condition         Control Affected         Comment           7         R/W         0         PD_CON_Rx1         CONx power override           6         R/W         0         PD_CON_Tx1         0         Normal operation
7         R/W         0         PD_CON_Rx1         CONx power override           6         R/W         0         PD_CON_Tx1         0         Normal operation
6 R/W 0 PD_CON_Tx1 CONx power override
0 R/W 0 PD_CON_IXI 0 Normal operation
5   R/W   0   PD_CON_TX2   1   Forms the CONy to mayor down sta
4 R/W 0 PD_CON_RX2
3 R/W 0 — Reserved
2 R/W 0 — Reserved
1 R/W 0 — Reserved
0 R/W 0 — Reserved





RYTE	5 (Equaliza	ation Flat Gain and -1dF	Linear Swing Setting of CON_Rx2)	
Bit	Type	Power-up Condition	Control Affected	Comment
7	R/W	0	EQ_CON<3>	Comment
6	R/W	0	EQ_CON<2>	
5	R/W	0	EQ_CON<1>	CON_Rx2 setting configuration
4	R/W	0	EQ_CON<0>	
3	R/W		FG_CON<1>	Equalizer
		0	_	Flat Gain
2	R/W	1	FG_CON<0>	Swing
1	R/W	0	SW_CON<1>	
0	R/W	l I	SW_CON<0>	
	· · ·		B Linear Swing Setting of AP_Tx2)	
Bit	Type	Power-up Condition	Control Affected	Comment
7	R/W	0	EQ_AP<3>	
6	R/W	0	EQ_AP<2>	CON_Tx2 setting configuration
5	R/W	0	EQ_AP<1>	COTY_TAZ Setting configuration
4	R/W	0	EQ_AP<0>	Equalizer
3	R/W	0	FG_AP<1>	Flat Gain
2	R/W	1	FG_AP<0>	Swing
1	R/W	0	SW_AP<1>	5 mig
0	R/W	1	SW_AP<0>	
BYTE	7 (Equalization	ation, Flat Gain, and -1dl	B Linear Swing Setting of AP_Tx1)	
Bit	Type	Power-up Condition	Control Affected	Comment
7	R/W	0	EQ_AP<3>	
6	R/W	0	EQ_AP<2>	
5	R/W	0	EQ_AP<1>	CON_Tx1 setting configuration
4	R/W	0	EQ_AP<0>	
3	R/W	0	FG_AP<1>	Equalizer
2	R/W	1	FG_AP<0>	Flat Gain
1	R/W	0	SW_AP<1>	Swing
0	R/W	1	SW AP<0>	
-		ation Flat Gain and -1dl	B Linear Swing Setting of CON_Rx1	<u>)</u>
Bit	Type	Power-up Condition	Control Affected	Comment
7	R/W	()	EQ_CON<3>	Comment
6	R/W	0	EQ_CON<2>	
5	R/W		EQ_CON<2>	CON_Rx1 setting configuration
		0	<del></del>	
4	R/W	0	EQ_CON<0>	Equalizer
3	R/W	0	FG_CON<1>	<del>-</del>
2			EC CONTO	Flat Gain
	R/W	1	FG_CON<0>	Flat Gain Swing
1	R/W	1 0	SW_CON<1>	
1 0	R/W R/W	1 0 1	_	
1 0 <b>BYTE</b>	R/W R/W 9-11 (Rese	1 0 1 erved)	SW_CON<1> SW_CON<0>	
1 0 <b>BYTE</b> <b>BYTE</b>	R/W R/W 9-11 (Rese 12 (Thresh	1 0 1 erved) old, Feature Enable/ Dis	SW_CON<1> SW_CON<0> able, and Timing Setting)	Swing
1 0 BYTE BYTE Bit	R/W R/W 9-11 (Rese 12 (Thresh Type	1 0 1 erved) oold, Feature Enable/ Dis Power-up Condition	SW_CON<1> SW_CON<0> able, and Timing Setting)  Control Affected	Swing  Comment
1 0 <b>BYTE</b> <b>BYTE</b>	R/W R/W 9-11 (Rese 12 (Thresh Type R/W	1 0 1 erved) old, Feature Enable/ Dis	SW_CON<1> SW_CON<0> able, and Timing Setting)	Swing  Comment  High-speed channel signal detector threshold
1 0 BYTE BYTE Bit	R/W R/W 9-11 (Rese 12 (Thresh Type	1 0 1 erved) oold, Feature Enable/ Dis Power-up Condition	SW_CON<1> SW_CON<0> able, and Timing Setting)  Control Affected	Comment High-speed channel signal detector threshold setting
1 0 <b>BYTE</b> <b>BYTE</b> Bit 7	R/W R/W 9-11 (Rese 12 (Thresh Type R/W	1 0 1 erved) oold, Feature Enable/ Dis Power-up Condition	SW_CON<1> SW_CON<0> able, and Timing Setting)  Control Affected  IDET_VTH<1>	Comment High-speed channel signal detector threshold setting 00 50mVppd
1 0 BYTE BYTE Bit	R/W R/W 9-11 (Rese 12 (Thresh Type R/W	1 0 1 erved) oold, Feature Enable/ Dis Power-up Condition	SW_CON<1> SW_CON<0> able, and Timing Setting)  Control Affected	Comment High-speed channel signal detector threshold setting 00 50mVppd 01 65mVppd (Default)
1 0 <b>BYTE</b> <b>BYTE</b> Bit 7	R/W R/W 9-11 (Rese 12 (Thresh Type R/W	1 0 1 erved) old, Feature Enable/ Dis Power-up Condition 0	SW_CON<1> SW_CON<0> able, and Timing Setting)  Control Affected  IDET_VTH<1>	Comment High-speed channel signal detector threshold setting 00 50mVppd 01 65mVppd (Default) 10 80mVppd
1 0 <b>BYTE</b> <b>BYTE</b> <b>Bit</b> 7	R/W R/W 9-11 (Rese 12 (Thresh Type R/W R/W	1 0 1 erved) old, Feature Enable/ Dis Power-up Condition 0	SW_CON<1> SW_CON<0> able, and Timing Setting)  Control Affected  IDET_VTH<1> IDET_VTH<0>	Comment High-speed channel signal detector threshold setting 00 50mVppd 01 65mVppd (Default)
1 0 <b>BYTE</b> <b>BYTE</b> <b>Bit</b> 7	R/W R/W 9-11 (Rese 12 (Thresh Type R/W R/W	1 0 1 erved) old, Feature Enable/ Dis Power-up Condition 0	SW_CON<1> SW_CON<0> able, and Timing Setting)  Control Affected IDET_VTH<1> IDET_VTH<0> Reserved	Comment High-speed channel signal detector threshold setting 00 50mVppd 01 65mVppd (Default) 10 80mVppd
1 0 <b>BYTE</b> <b>BYTE</b> <b>Bit</b> 7	R/W R/W 9-11 (Rese 12 (Thresh Type R/W R/W	1 0 1 erved) old, Feature Enable/ Dis Power-up Condition 0	SW_CON<1> SW_CON<0> able, and Timing Setting)  Control Affected  IDET_VTH<1> IDET_VTH<0>	Comment High-speed channel signal detector threshold setting 00 50mVppd 01 65mVppd (Default) 10 80mVppd
1 0 BYTE BYTE Bit 7 6	R/W R/W 9-11 (Rese 12 (Thresh Type R/W R/W	1 0 1 erved) sold, Feature Enable/ Dis Power-up Condition 0	SW_CON<1> SW_CON<0> able, and Timing Setting)  Control Affected IDET_VTH<1> IDET_VTH<0> Reserved	Comment High-speed channel signal detector threshold setting 00 50mVppd 01 65mVppd (Default) 10 80mVppd
1 0 BYTE BYTE Bit 7 6	R/W R/W 9-11 (Rese 12 (Thresh Type R/W R/W R/W	1 0 1 erved) old, Feature Enable/ Dis Power-up Condition 0 1	SW_CON<1> SW_CON<0> able, and Timing Setting)  Control Affected  IDET_VTH<1>  IDET_VTH<0>  Reserved  Reserved	Comment High-speed channel signal detector threshold setting 00 50mVppd 01 65mVppd (Default) 10 80mVppd
1 0 BYTE BYTE Bit 7 6	R/W R/W 9-11 (Rese 12 (Thresh R/W R/W R/W R/W	1 0 1 erved) cold, Feature Enable/ Dis Power-up Condition 0 1 1 1 0	SW_CON<1> SW_CON<0> able, and Timing Setting)  Control Affected  IDET_VTH<1>  IDET_VTH<0>  Reserved  Reserved  Reserved  Reserved	Comment High-speed channel signal detector threshold setting 00 50mVppd 01 65mVppd (Default) 10 80mVppd
1 0 BYTE BYTE 7 6 5 4 3 2	R/W R/W 9-11 (Rese 12 (Thresh R/W R/W R/W R/W R/W R/W R/W R/W R/W	1 0 1 erved) cold, Feature Enable/ Dis Power-up Condition 0 1 1 1 0 0 0	SW_CON<1> SW_CON<0> able, and Timing Setting)  Control Affected  IDET_VTH<1>  IDET_VTH<0>  Reserved  Reserved  Reserved  Reserved  Reserved  Reserved  Reserved	Comment High-speed channel signal detector threshold setting 00 50mVppd 01 65mVppd (Default) 10 80mVppd
1 0 BYTE BYTE 7 6 5 4 3 2 1 0	R/W R/W 9-11 (Rese 12 (Thresh R/W	1 0 1 1 erved) rold, Feature Enable/ Dis Power-up Condition 0 1 1 1 0 0 0 0 1	SW_CON<1> SW_CON<0> able, and Timing Setting)  Control Affected  IDET_VTH<1>  IDET_VTH<0>  Reserved  Reserved  Reserved  Reserved  Reserved  Reserved  Reserved  Reserved  Reserved  Reserved	Comment High-speed channel signal detector threshold setting 00 50mVppd 01 65mVppd (Default) 10 80mVppd







**Equalization Setting (dB):** 

		<u> </u>	<u></u>								
EQ1pin	EQ0pin	EQ3	EQ2	EQ1	EQ0	@ 2.5GHz	@ 3GHz	@ 4GHz	@ 5GHz	@ 6GHz	Note
0	F	0	0	0	0	3.57	4.22	5.44	6.42	7.27	Default
0	1	0	0	0	1	3.83	4.56	5.93	7.04	8.00	_
0	0	0	0	1	0	4.13	4.93	6.47	7.71	8.76	_
0	R	0	0	1	1	4.41	5.29	6.95	8.29	9.42	_
R	1	0	1	0	0	4.98	5.89	7.61	8.99	10.14	_
R	F	0	1	0	1	5.25	6.23	8.05	9.50	10.70	_
R	R	0	1	1	0	5.55	6.59	8.51	10.04	11.28	_
R	0	0	1	1	1	5.82	6.92	8.93	10.51	11.78	_
F	0	1	0	0	0	6.39	7.44	9.39	10.93	12.16	_
F	R	1	0	0	1	6.63	7.74	9.76	11.34	12.60	_
F	F	1	0	1	0	6.90	8.05	10.14	11.77	13.05	_
F	1	1	0	1	1	7.14	8.34	10.49	12.15	13.44	_
1	R	1	1	0	0	7.51	8.71	10.87	12.53	13.81	_
1	0	1	1	0	1	7.74	8.97	11.18	12.87	14.15	_
1	1	1	1	1	0	7.98	9.25	11.51	13.23	14.51	_
1	F	1	1	1	1	8.20	9.51	11.81	13.54	14.82	_

## Flat Gain Setting:

FGpin is the selection pin for the DC gain

	- 0				
FGpin	FG<1:0>	Flat Gain Setting (dB)			
R	00	-2.07			
F	01	-0.24 (Default)			
0	10	0.62			
1	11	1.77			

# **Swing -1dB Compression Point Output Swing Setting:**

SWpin is the selection pin for SW

SWpin	SW<1:0>	Swing Setting	
0	00	900 mVppd	
1	01	1000 mVppd (Default)	
F	10	1100 mVppd	
R	11	1200 mVppd	

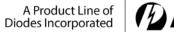
## **ReDriver Connection in Pin Mode**

EN	SEL	ReDriver Status
0	X	Inactive
1	1	TX_CON1/RX_CON1 Active
1	0	TX_CON2/RX_CON2 Active

## **ReDriver Connection in I2C Mode**

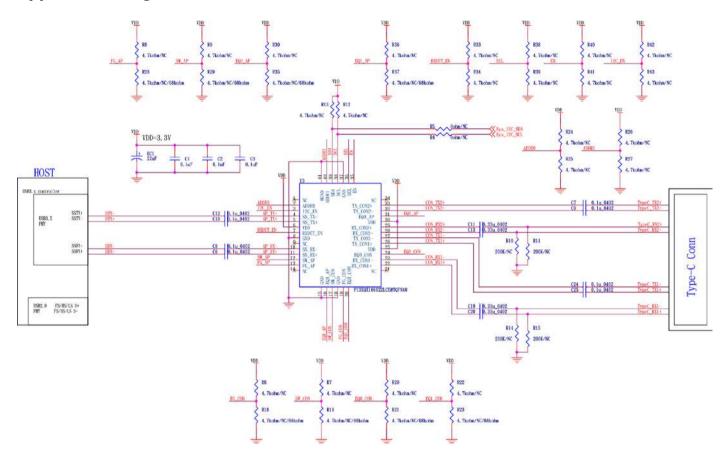
EN	BYTE3 CONF<2:0>	ReDriver Status
0	X	Inactive
1	100	TX_CON1/RX_CON1 Active
1	101 (default)	TX_CON2/RX_CON2 Active







# **Application Diagram**



## **Part Marking**

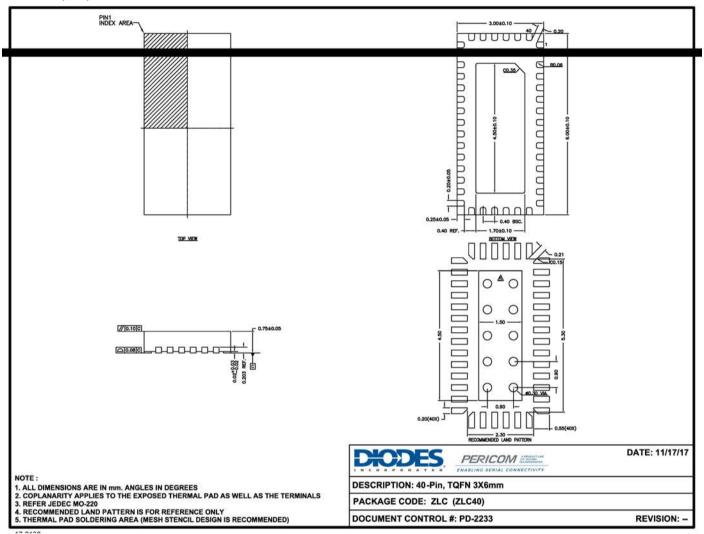
Top mark not available at this time. To obtain advanced information regarding the top mark, contact your local sales representative.





## **Packaging Mechanical**

40-TQFN (ZLC)



### For latest package information:

See http://www.diodes.com/design/support/packaging/pericom-packaging/packaging-mechanicals-and-thermal-characteristics/.

## **Ordering Information**

Ordering Number	Package Code	Package Description
PI3EQX10612ZLCEX ZLC		40-Pin, 3mm × 6mm (TQFN)

### Notes:

- 1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
- 2. See https://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
- 3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
- 4. E = Pb-free and Green
- 5. X suffix = Tape/Reel





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