IS31BL3555

2 CHANNELS, 200MA BOOST LED BACKLIGHT DRIVER

Preliminary Information
September 2017

GENERAL DESCRIPTION

The IS31BL3555 is a step-up controller with an integrated switching FET for driving white LED arrays in LCD panel backlight applications. The boost controller is a current mode, fixed frequency architecture with the switching frequency set by an external resistor. The integrated boost controller generates the minimum output voltage to keep all LEDs illuminated at the set current. The current in each of the 2 channels is programmed to a specific value with an external current set resistor and matched to within 1%.

LED dimming is achieved using an external digital PWM signal to either adjust the internal ISET current or pulse-width-modulate the LED intensity. The LED sinks have a fast response to a PWM input making it possible to achieve a high contrast ratio of 10,000:1.

A synchronization pin can be used to synchronize multiple IS31BL3555 devices or to synchronize with the external PWM source in the range of 580kHz to 1MHz.

The IS31BL3555 integrates protection features including output overvoltage, open or shorted diode, open or shorted LED, shorted FSET or ISET resistor, and IC over temperature. A dual level cycle-by-cycle current limit function provides soft start and protects the internal current switch against high current overloads.

The IS31BL3555 is available in a thermally enhanced eTSSOP-16 package.

FEATURES

- Input voltage range is 4.75V to 40V
- Excellent input voltage transient response
- Sync function to synchronize boost converter switching frequency up to 1MHz
- Single resistor primary OVP minimizes VOUT leakage
- Fully integrated LED current sinks and boost converter up to 55V
- LED current of 200mA per channel
- 1% LED to LED matching accuracy
- Internal secondary OVP for redundant protection
- Drives up to 12 series LEDs in 2 parallel strings
- 10000:1 PWM dimming at 100Hz
- PWM and analog dimming inputs
- Built-in protection features:
  - Shorted FSET or ISET resistor
  - Open or shorted LED
  - Open boost Schottky
  - Overtemperature (OTP)

APPLICATIONS

- LCD monitor
- LCD display module
- LCD TV
- Car infotainment
- Cluster

TYPICAL APPLICATION CIRCUIT

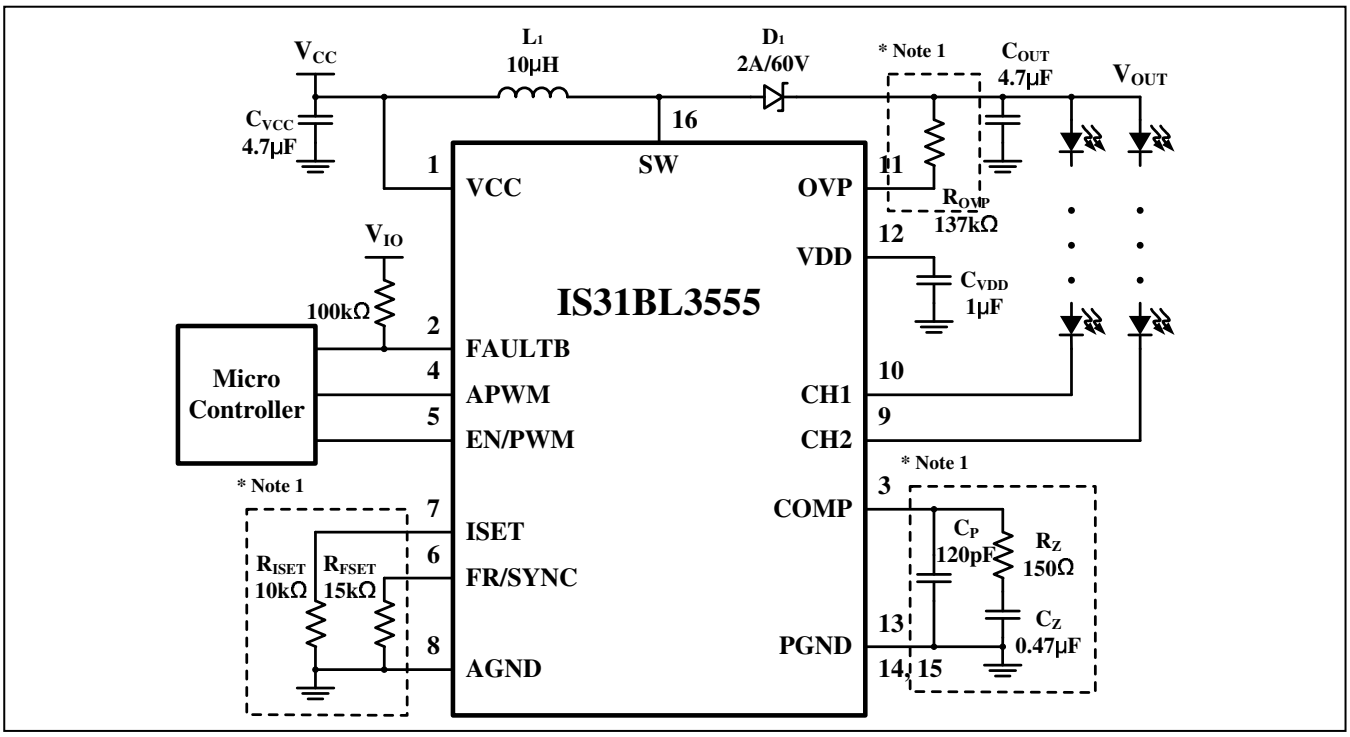
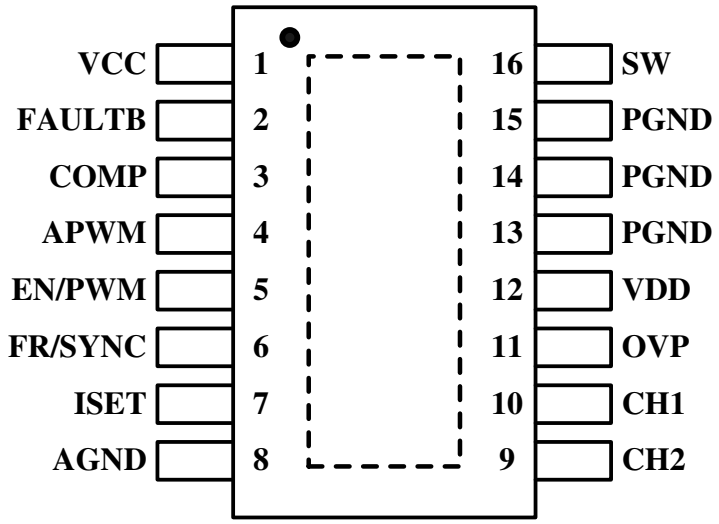


Figure 1 Typical Application Circuit

Note 1: Value of those devices need to adjust according different applications.

PIN CONFIGURATION

Package	Pin Configuration (Top View)
eTSSOP-16	

PIN DESCRIPTION

No.	Pin	Description
1	VCC	Power supply input. Bypass VCC to GND with a capacitor to keep the DC input voltage constant.
2	FAULTB	Open drain fault flag to indicate a fault condition. Connect a 100kΩ resistor between this pin and the required logic level voltage.
3	COMP	Soft-start and control loop compensation. Connect a series R_Z-C_Z network from this pin to ground for control loop compensation.
4	APWM	Analog trimming option for dimming. Applying a digital PWM signal to this pin adjusts the internal ISET current.
5	EN/PWM	PWM signal input for LED dimming, used to control the LED intensity by using pulse width modulation. Also used to enable the IS31BL3555.
6	FR/SYNC	Frequency and synchronization pin. A resistor R_{FR} from this pin to ground sets the switching frequency. This pin can also be used to synchronize two or more IS31BL3555s in the system. The maximum synchronization frequency is 1MHz.
7	ISET	LED current adjust input. Connect a resistor R_{ISET} between ISET pin and GND to set the reference current through each LED string.
8	AGND	LED signal ground.
9,10	CH2,CH1	Connect the cathodes of the LED strings to these pins. All unused pins should be connected with a 1.54kΩ resistor to ground.
11	OVP	Over voltage protection pin; connect the R_{OVP} resistor from VOUT to this pin to adjust the overvoltage protection.
12	VDD	Output of internal LDO; connect a 1μF decoupling capacitor between this pin and ground.
13~15	PGND	Power ground for internal NMOS.
16	SW	The drain of the internal NMOS switch of the boost converter.
	Thermal Pad	Connect to GND.

ORDERING INFORMATION

Industrial Range: -40°C to +125°C

Order Part No.	Package	QTY
IS31BL3555-ZLS4-TR	eTSSOP-16, Lead-free	2500/Reel
IS31BL3555-ZLS4		96/Tube

ABSOLUTE MAXIMUM RATINGS

Voltage in CHx, OVP pins	-0.3V ~ +55V
Voltage in VCC, FAULTB pins	-0.3V ~ +40V
Voltage in ISET, FR/SYNC, APWM, COMP pins	-0.3V ~ +5.5V
Voltage in SW pin, continuous Voltage in SW pin, t<50ns	-0.6V ~ 65V -1.0V
All other pins	-0.3V ~ +6.0V
Package thermal resistance, θ_{JA}, thermal simulation @25°C ambient temperature, still air convection, 2s2p boards according to JESD51	39.9°C/W
Operating junction temperature, T_A=T_J	+150°C
Storage temperature range, T_{STG}	-65°C ~ +150°C
ESD (HBM) ESD (CDM)	±2kV ±750V

Note:
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other condition beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS (NOTE 1, 2)

T_J= -40°C ~ +125°C, V_{CC}= 12V. Typical value is T_J= 25°C, unless otherwise specified.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
Input Supply						
V_{CC}	Input voltage	(Note 3, 4)	4.75		40	V
V_{UVLO_R}	UVLO start threshold	V_{CC} rising (Note 3)			4.35	V
V_{UVLO_F}	UVLO stop threshold	V_{CC} falling (Note 3)			3.90	V
V_{UVLO_HY}	UVLO hysteresis	(Note 2)	300	450	600	mV
I_{CC}	Quiescent current	$V_{EN/PWM}$= V_{IH}, f_{SW}= 1MHz, no load (Note 3)		5.5	10	mA
I_{SD}	Shutdown current	V_{CC}= 12V, $V_{EN/PWM}$= $V_{FR/SYNC}$= 0V (Note 3)		5.0	10	μA
Input Logic Levels (EN/PWM and APWM)						
V_{IL}	Input logic level-low	VCC throughout operating input voltage range (Note 3)			0.4	V
V_{IH}	Input logic level-high	VCC throughout operating input voltage range (Note 3)	1.5			V
$R_{EN/PWM}$	EN/PWM pin open drain pull-down resistor		60	100	140	kΩ
R_{APWM}	APWM pull-down resistor		60	100	140	kΩ

ELECTRICAL CHARACTERISTICS (CONTINUED)

T_J= -40°C ~ +125°C, V_{CC}= 12V. Typical value is T_J= 25°C, unless otherwise specified.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
APWM						
f_{APWM}	APWM frequency	V_{IH}= 1.5V, V_{IL}= 0.4V (Note 2,3)	20		1000	kHz
Overvoltage Protection						
V_{OVP1}	OVP threshold	OVP connected to V_{OUT} (Note 3)	7.7	8.1	8.5	V
I_{OVPS}	OVP sense current	(Note 3)	188	199	210	µA
I_{OVPL}	OVP leakage current	(Note 3)		0.1	1	µA
V_{OVP2}	Secondary over voltage protection	(Note 3)		60		V
Boost Switch						
R_{SW}	Switch on-resistance	I_{SW}= 0.750A, V_{CC}= 12V(Note 3)	75	300	600	mΩ
I_{SW_LKG}	Switch leakage current	V_{SW}= 16V, $V_{EN/PWM}$= V_{IL}(Note 3)		0.1	1	µA
I_{SW_LIM1}	Switch current limit	(Note 3)	3.0	3.5	4.2	A
I_{SW_LIM2}	Secondary switch current limit	Higher than maximum I_{SW_LIM1} for all conditions, device latches when detected (Note 2)		7.0		A
t_{SW_ON}	Minimum switch on-time	(Note 3)		200		ns
t_{SW_OFF}	Minimum switch off-time	(Note 3)		50		ns
Oscillator Frequency						
f_{SW}	Oscillator frequency	R_{FR}= 14.4kΩ (Note 3)	0.84	1	1.13	MHz
		R_{FR}= 20kΩ (Note 3)	0.675	0.75	0.875	
$V_{FR/SYNC}$	FR/SYNC pin voltage	R_{FR}= 15kΩ		1.0		V
f_{FR}	FR frequency range	(Note 2)	200		1000	kHz
Synchronization						
f_{SY}	Synchronized PWM frequency	(Note 2)	580		1000	kHz
t_{SY_OFF}	Synchronization input minimum off-time	(Note 2)	150			ns
t_{SY_ON}	Synchronization input minimum on-time	(Note 2)	150			ns
V_{SY_H}	SYNC input logic voltage	FR/SYNC pin, high level (Note 3)	2.0			V
V_{SY_L}		FR/SYNC pin, low level (Note 3)			0.4	V
Thermal Protection (TSD)						
T_{SD_TH}	Thermal shutdown threshold	Temperature rising (Note 2)		165		°C
T_{SD_HY}	Thermal shutdown hysteresis	(Note 2)		20		°C

ELECTRICAL CHARACTERISTICS (CONTINUED)

T_J= -40°C ~ +125°C, V_{CC}= 12V. Typical value is T_J= 25°C, unless otherwise specified.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
FAULTB Pin						
V_{FAULT_PD}	FAULTB pull-down voltage	I_{FAULTB}= 1mA (Note 3)			0.5	V
I_{FAULT_L}	FAULTB pin leakage current	V_{FAULTB}= 5V			1	μA
LED Current Sinks						
Err_{CH}	CHx accuracy	I_{SET}= 100μA (Note 3)			3	%
ΔI_{CH}	CHx matching	I_{SET}= 100μA (Note 3)			1	%
V_{CH}	CHx regulation voltage	V_{CH1}= V_{CH2}= V_{CH3}= V_{CH4}, I_{SET}= 100μA (Note 3)	620	720	820	mV
A_{ISET}	I_{SET} to I_{CHx} current gain	I_{SET}= 100μA (Note 3)	1940	2000	2060	A/A
V_{SET}	ISET pin voltage		0.99	1.00	1.01	V
I_{SET}	Allowable I_{SET} current	(Note 3)	20		100	μA
V_{CH_S}	V_{CH} short detect	While LED sinks are in regulation, sensed from CHx pin to ground (Note 3)	4.6	5.1	5.6	V
I_{CH_SS}	Soft start CHx current	Current through each enabled CHx pin during soft start		24		mA
t_{PWM_OFF}	Maximum PWM dimming until off-time (Note 2)	Measured while $V_{EN/PWM}$ = low, during dimming control and internal references are powered-on (exceeding t_{PWM_OFF} results in shutdown)		32,750		f_{SW} cycles
t_{PWM_ON}	Minimum PWM on-time	First cycle when powering-up device (Note 3)		0.75	2	μs
t_{PWMH_ON}	PWM high to LED-on delay	Time between PWM enable and LED current reaching 90% of maximum (Note 3)		0.5	0.9	μs
t_{PWML_OFF}	PWM low to LED-off delay	Time between PWM enable going low and LED current reaching 10% of maximum (Note 3)		0.9	1	μs

Note 1: For input and output current specifications, negative current is defined as coming out of the node or pin (sourcing); positive current is defined as going into the node or pin (sinking).

Note 2: Ensured by design and characterization, not production tested.

Note 3: Indicates specifications guaranteed by design and characterization over the full operating temperature range with T_A = T_J = –40°C ~ 125°C

Note 4: Minimum V_{CC}= 4.75V is only required at startup. After startup is completed, the IC is able to function down to V_{CC}= 4V.

TYPICAL PERFORMANCE CHARACTERISTICS

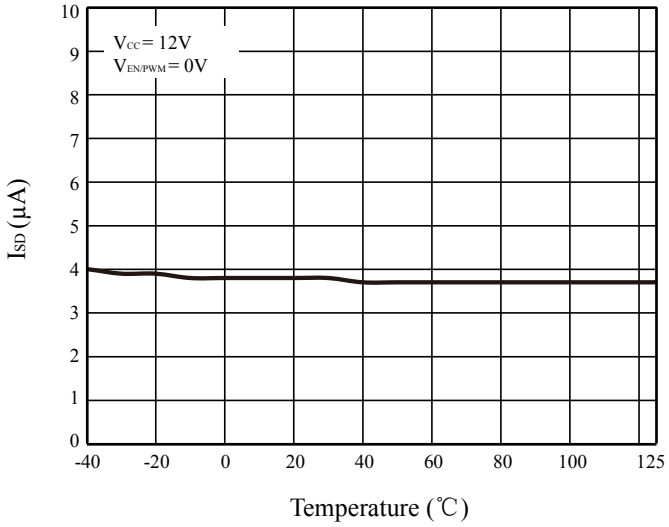


Figure 2 I_{SD} vs. Temperature

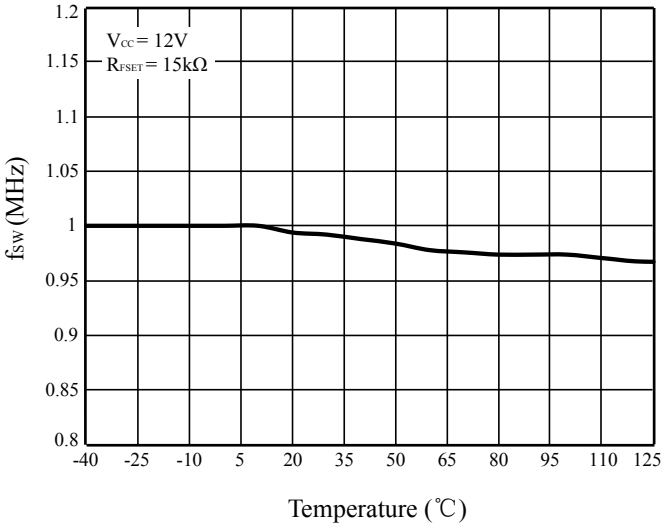


Figure 3 f_{SW} vs. Temperature

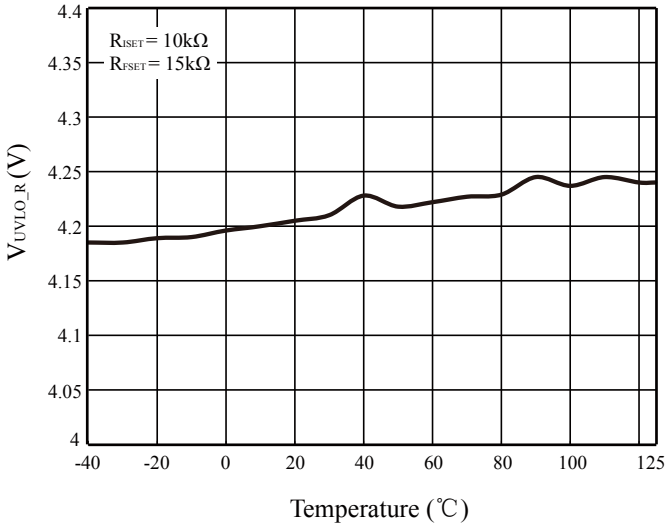


Figure 4 V_{UVLO_R} vs. Temperature

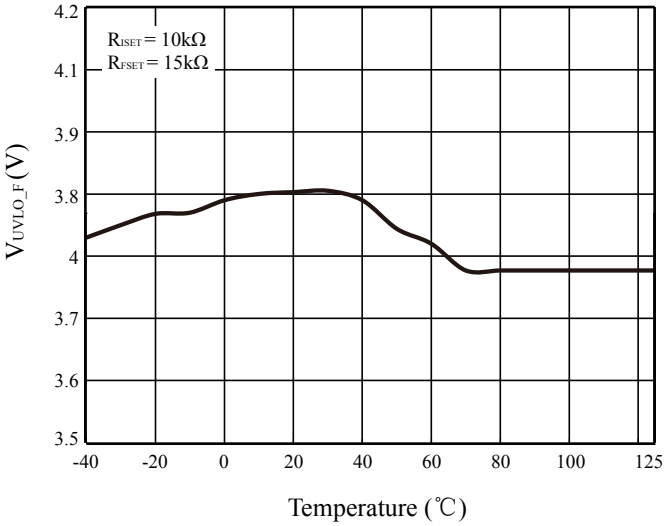


Figure 5 V_{UVLO_F} vs. Temperature

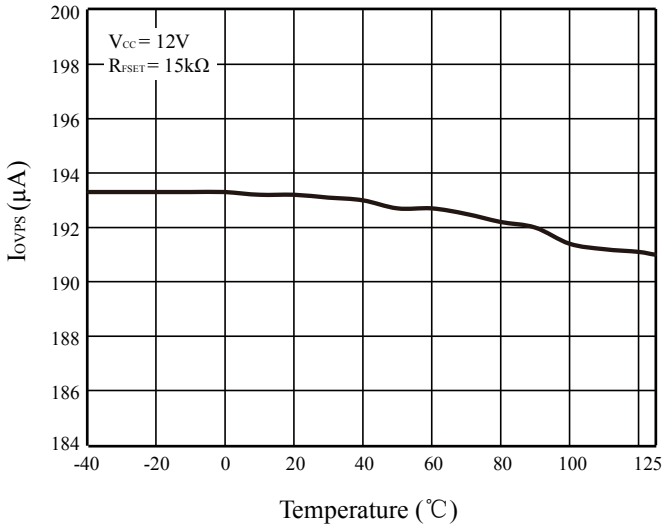


Figure 6 I_{OVPS} vs. Temperature

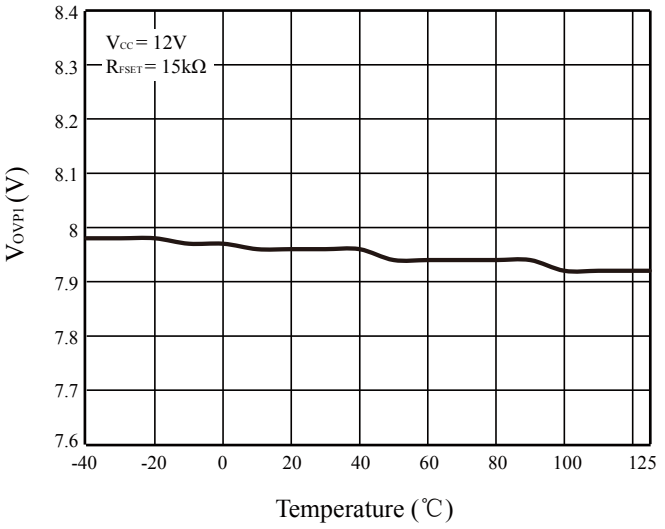


Figure 7 V_{OVP1} vs. Temperature

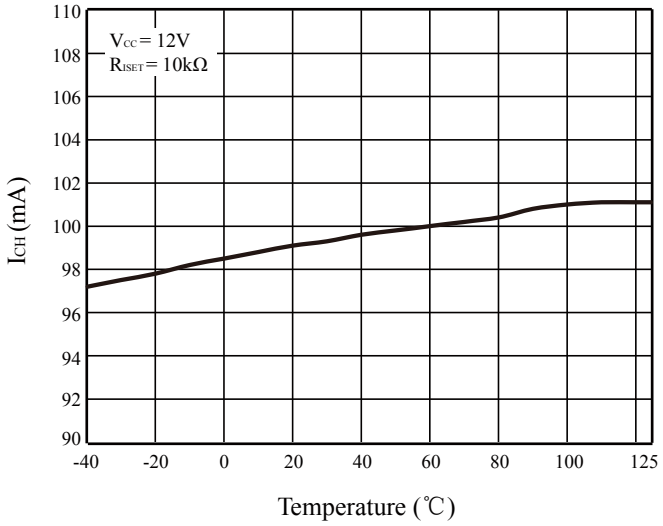


Figure 8 I_{CH} vs. Temperature

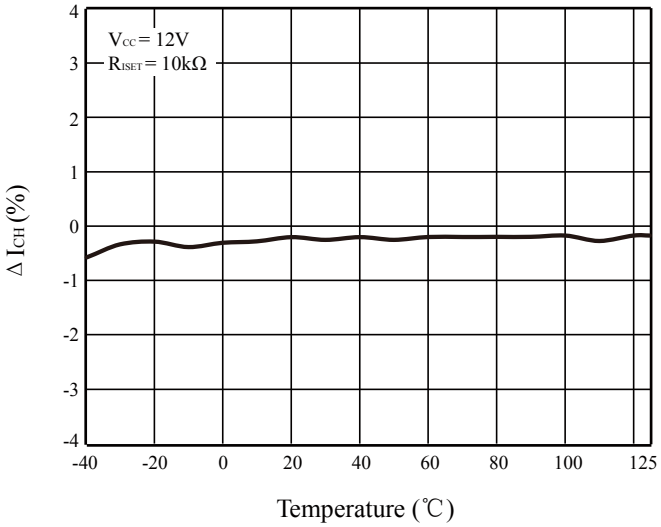


Figure 9 ΔI_{CH} vs. Temperature

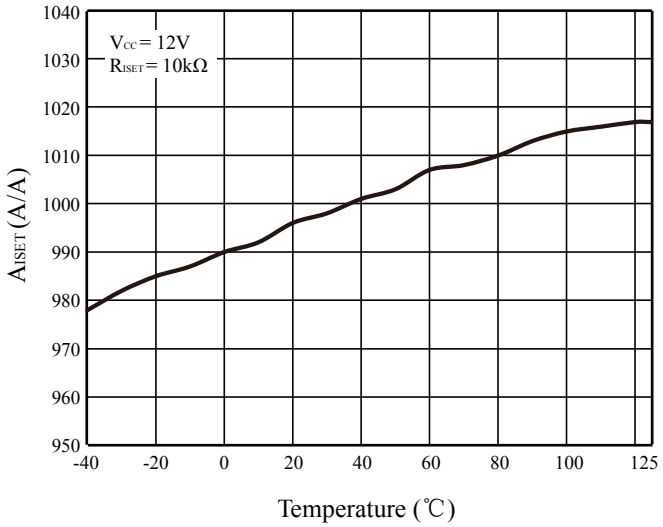


Figure 10 A_{ISET} vs. Temperature

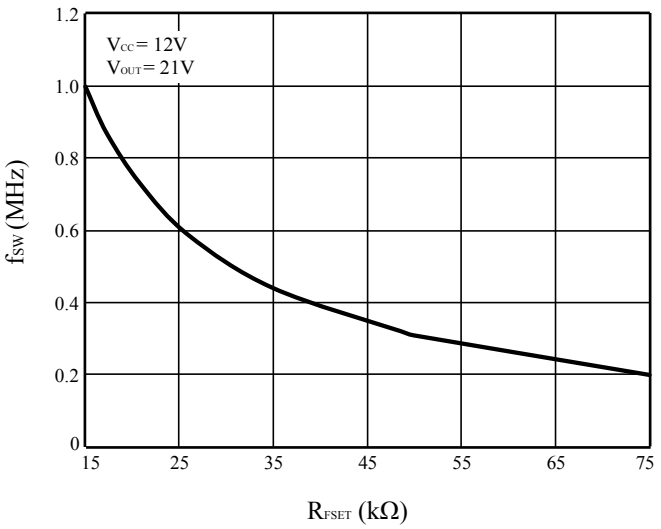


Figure 11 f_{SW} vs. R_{FSET}

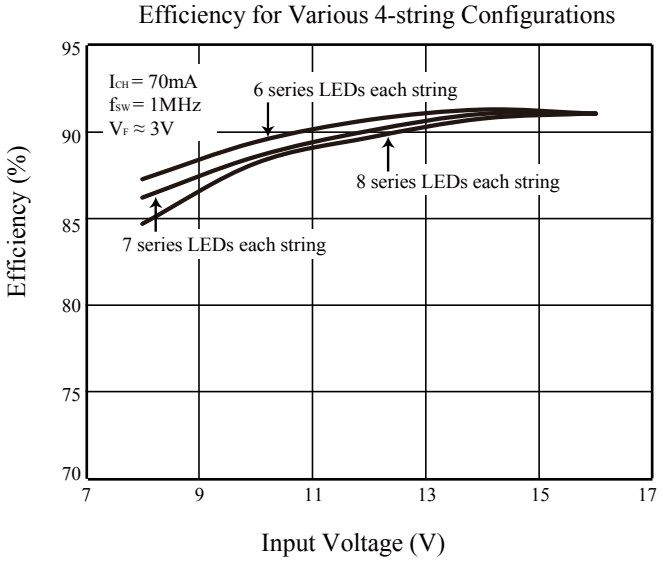


Figure 12 Efficiency vs. Voltage of String Configurations

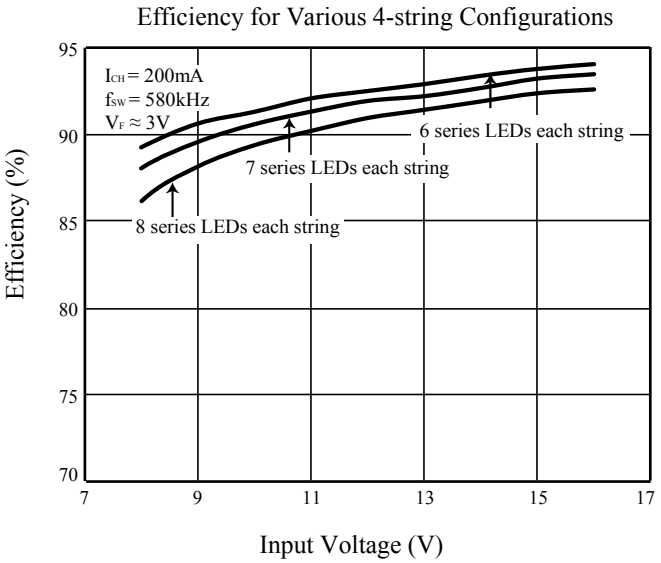


Figure 13 Efficiency vs. Voltage of String Configurations

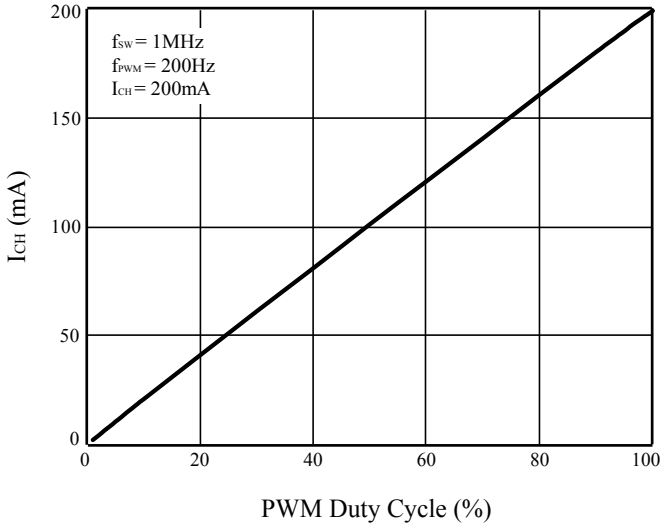


Figure 14 I_{CH} vs. PWM Duty Cycle

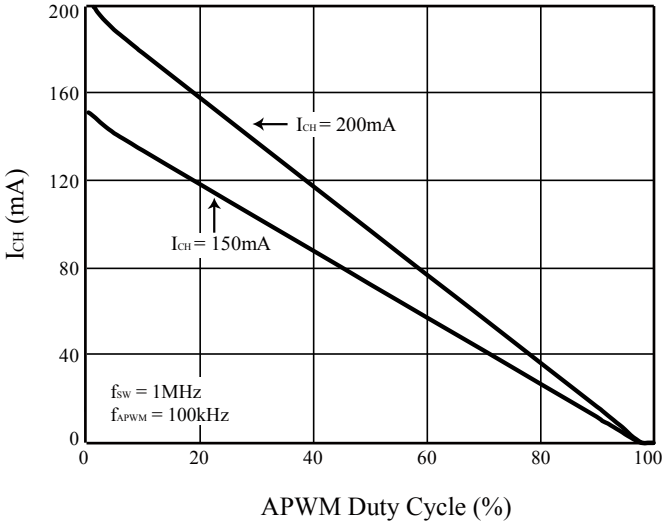


Figure 15 I_{CH} vs. APWM Duty Cycle

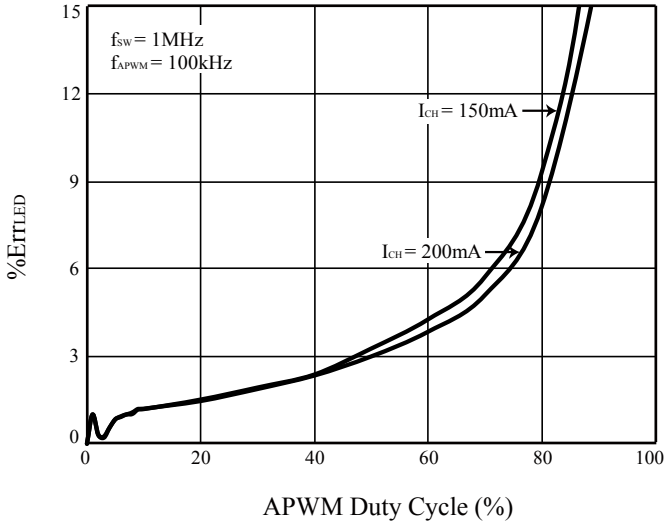


Figure 16 Percentage Error of I_{CH} vs. APWM Duty Cycle

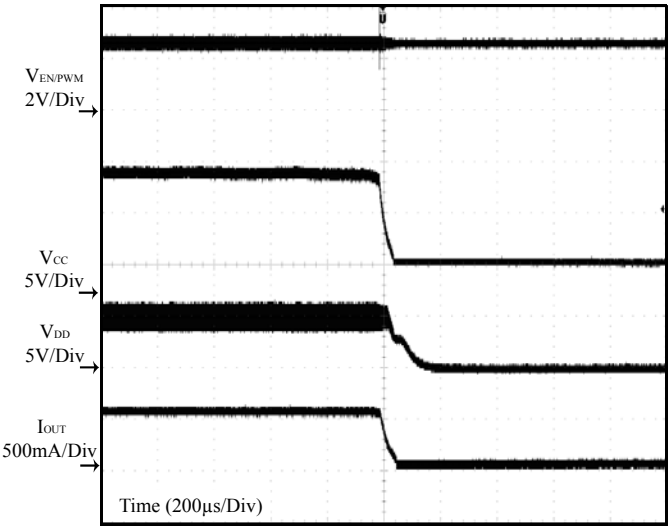


Figure 17 Power-Down

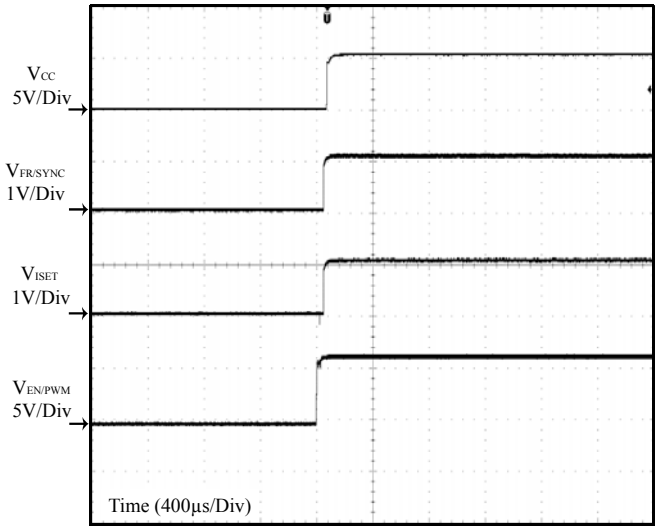


Figure 18 Power-Up

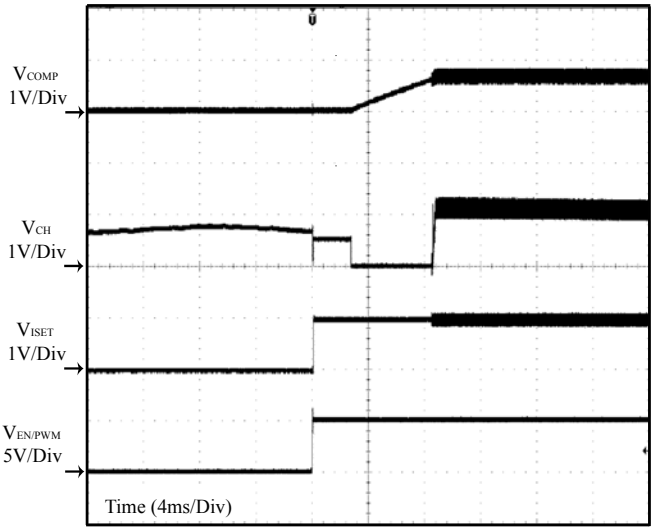


Figure 19 Power-Up

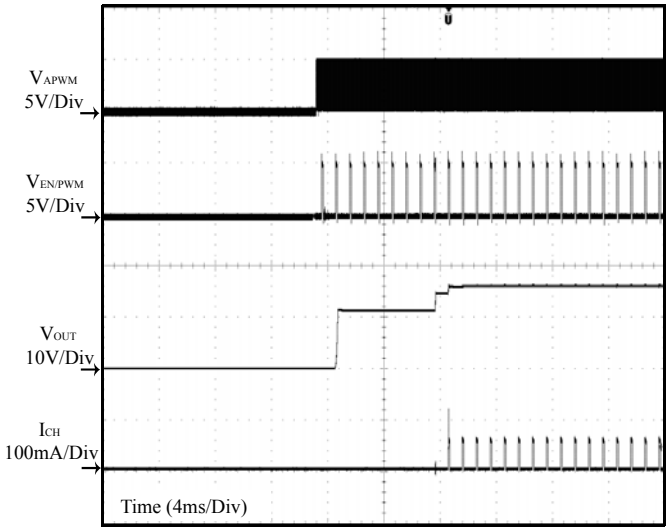


Figure 20 Power-Up With Both Dimming

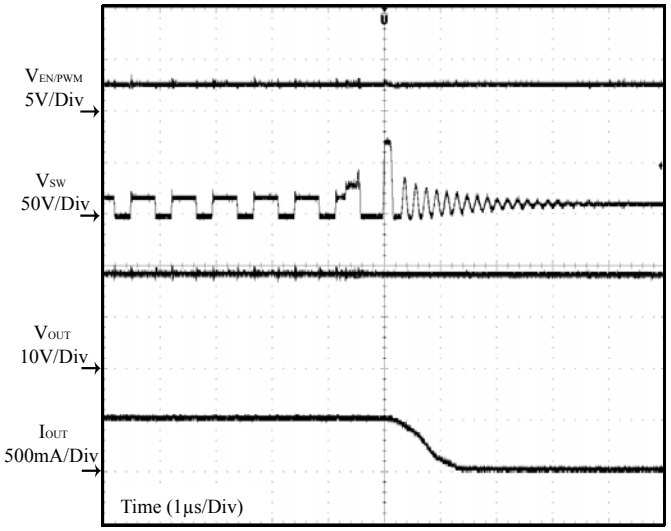


Figure 21 Open Schottky Diode During Normal Operation

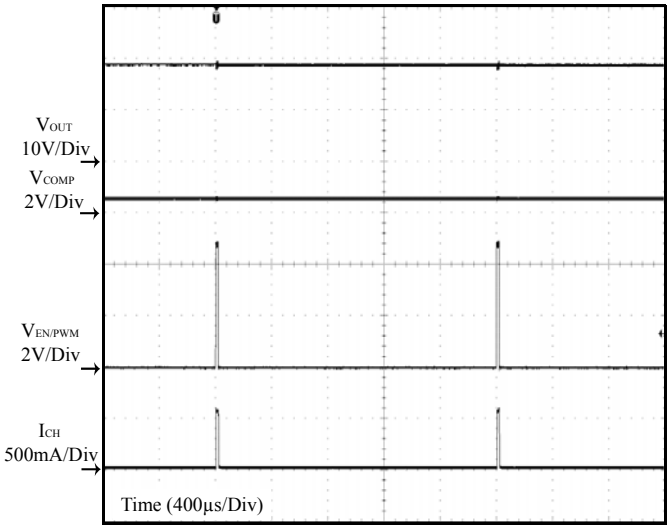


Figure 22 PWM Dimming Of Low Duty Cycle

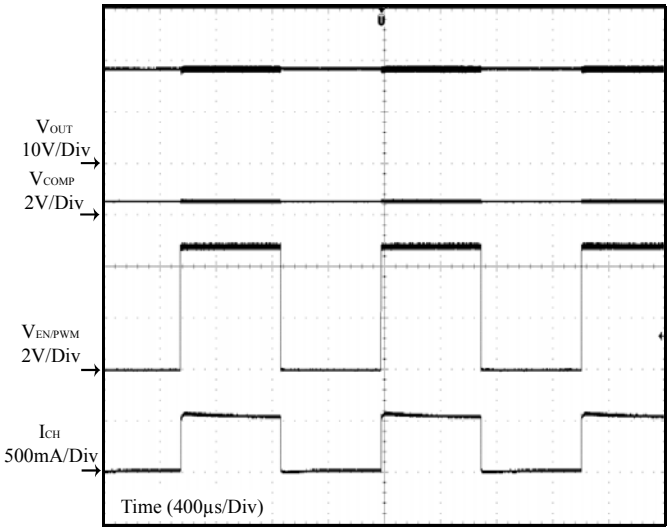


Figure 23 PWM Dimming Of High Duty Cycle

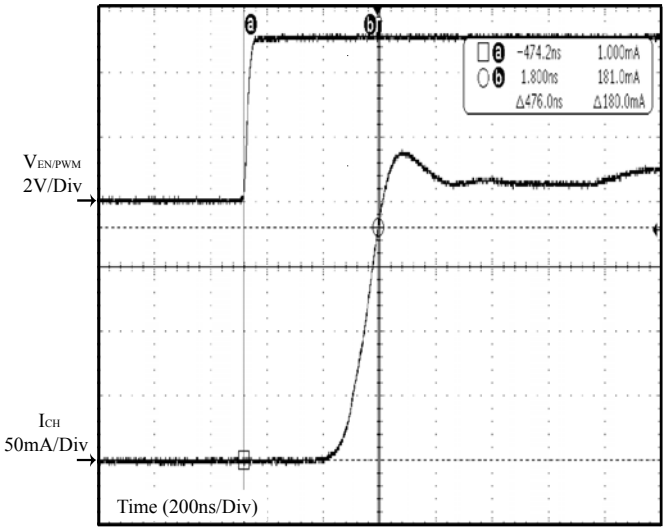


Figure 24 EN/PWM Rising

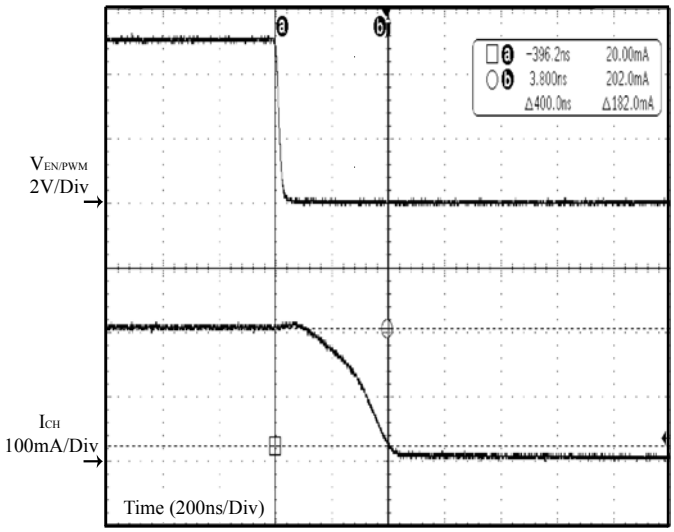


Figure 25 EN/PWM Falling

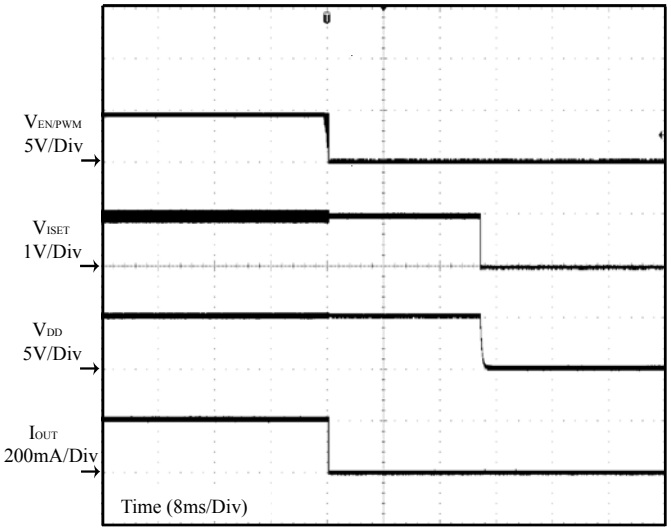


Figure 26 EN/PWM Disable

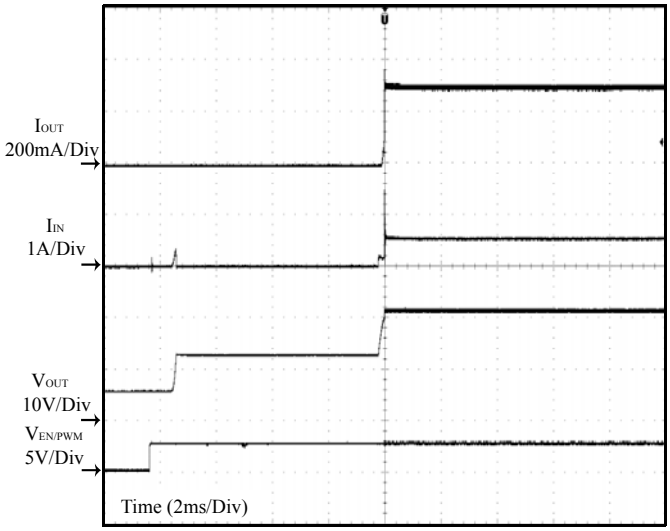


Figure 27 Startup by EN/PWM

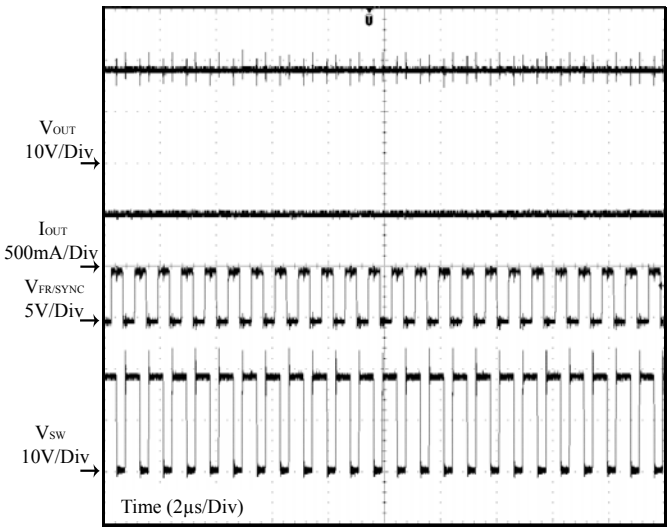


Figure 28 Normal Operation Of Synchronization

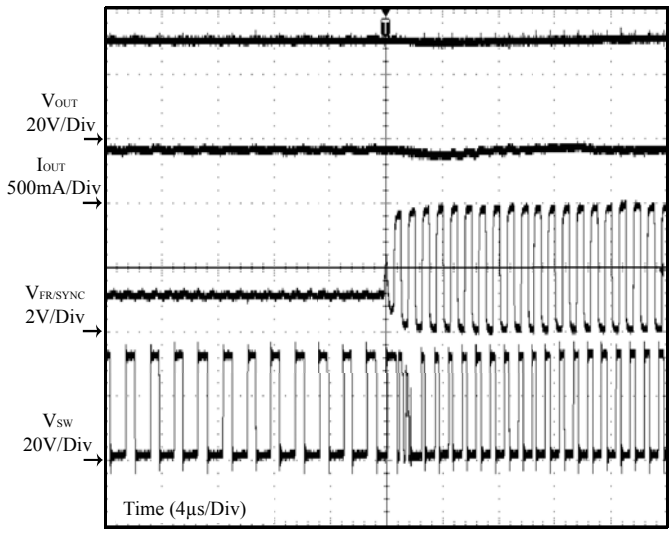


Figure 29 Transition Of Synchronization

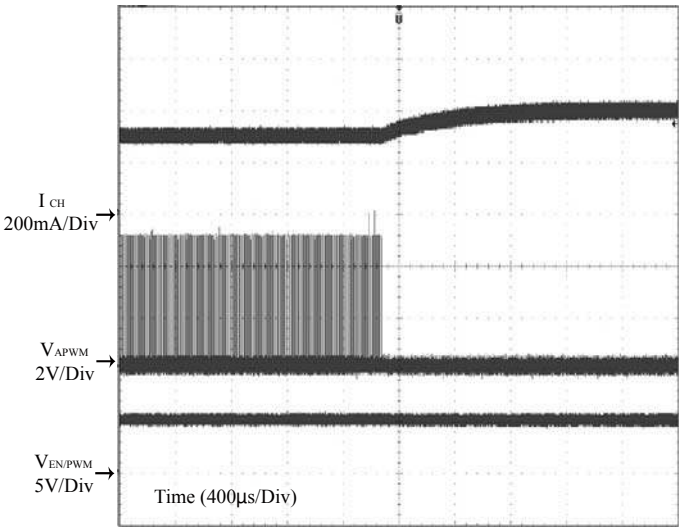


Figure 30 A 25% Duty Cycle Signal Removed From The APWM Pin

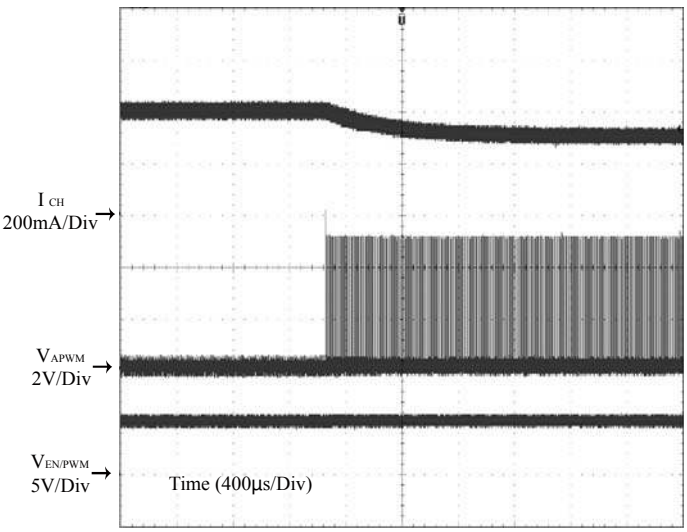


Figure 31 A 25% Duty Cycle Signal Applied To The APWM Pin

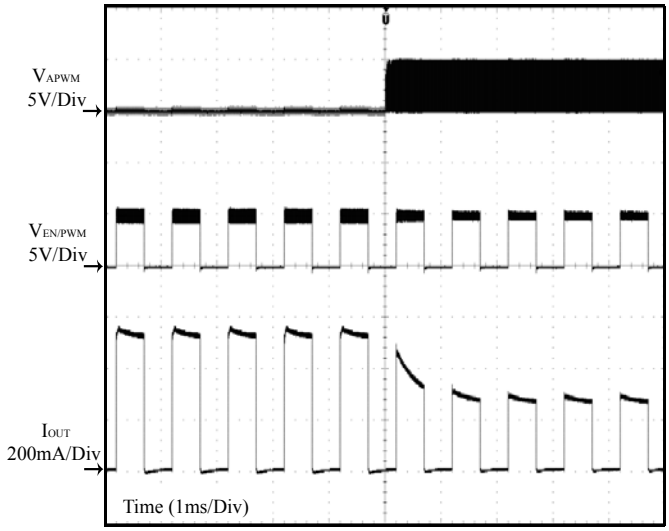


Figure 32 Signal Applied To The APWM Pin During PWM Dimming

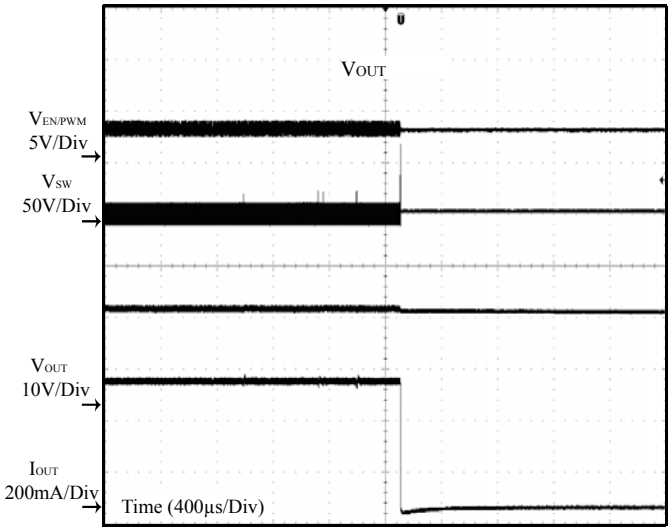


Figure 33 OVP Protection When The IC Is Enabled During An Open Diode Condition

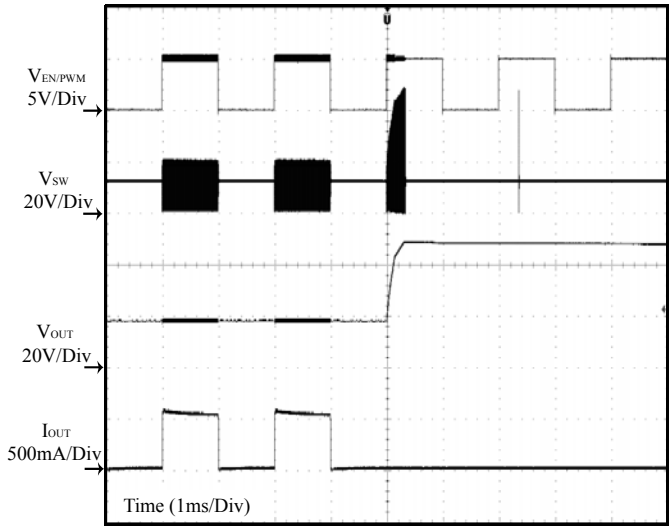


Figure 34 OVP Protection With Output Disconnect

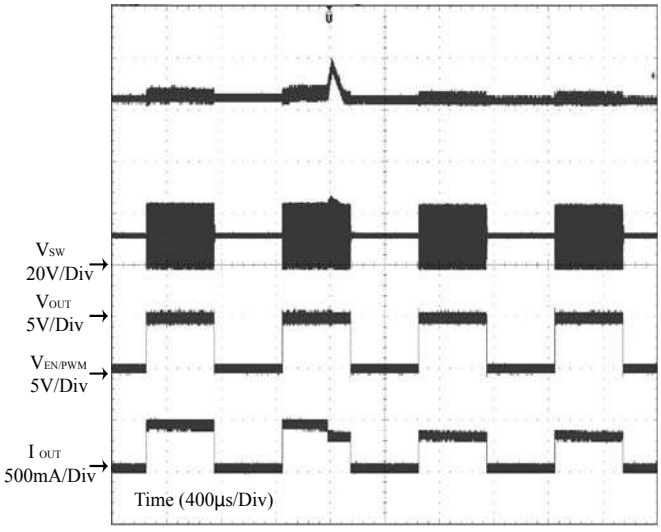


Figure 35 OVP Protection With Open LED String

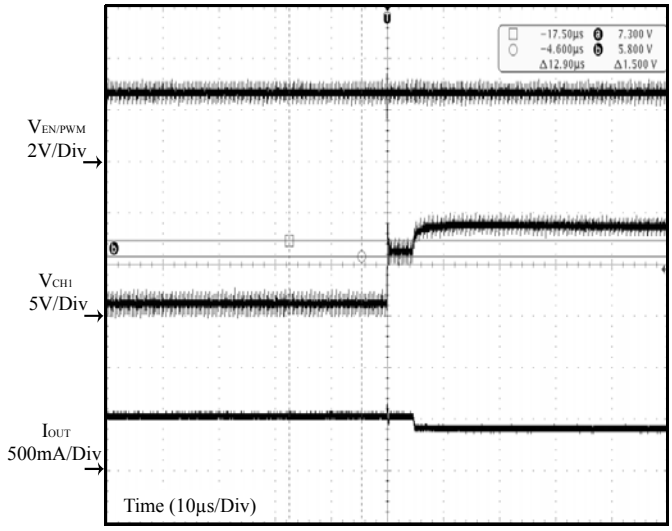


Figure 36 Disabling Of An LED String

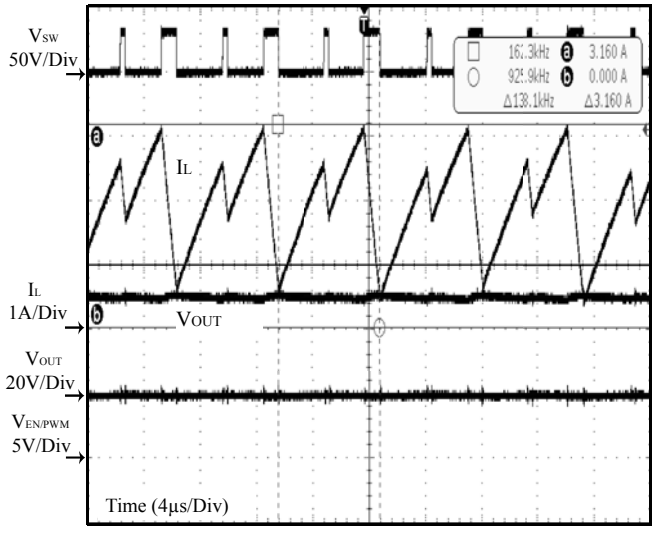


Figure 37 Cycle-By-Cycle Current Limiting

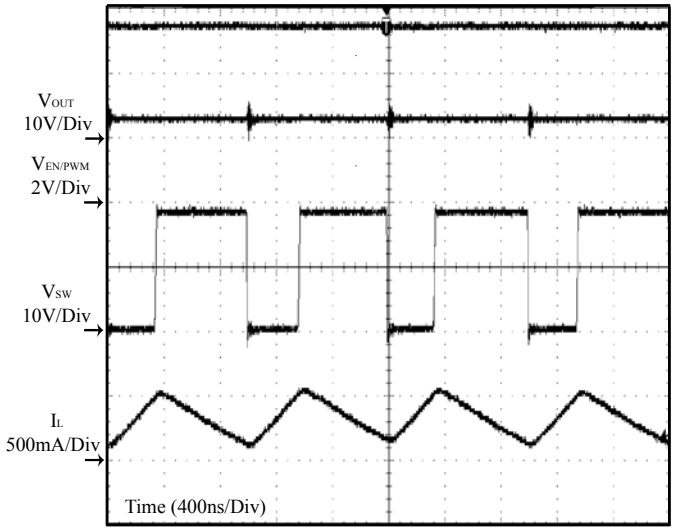
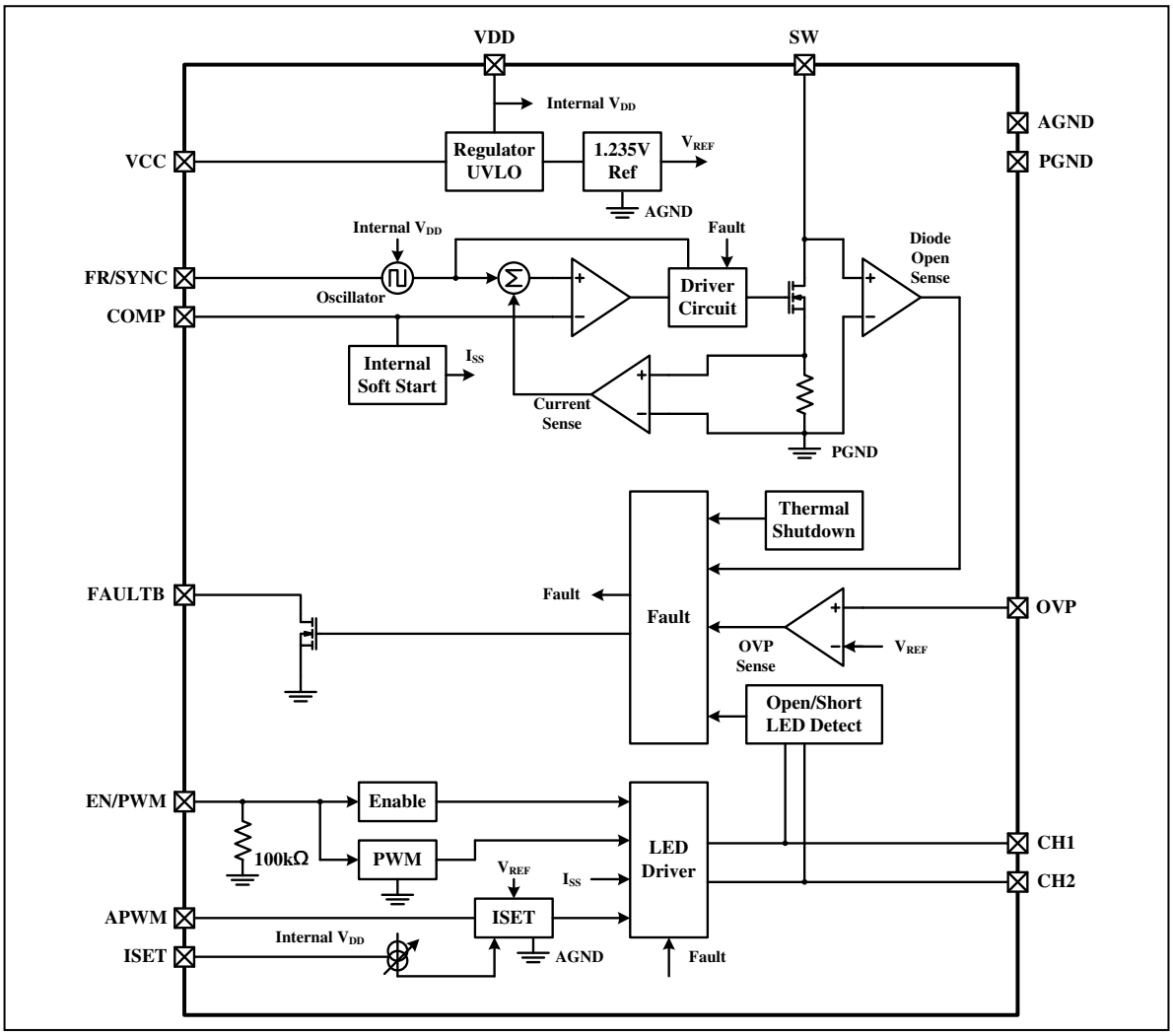


Figure 38 Normal Operation

FUNCTIONAL BLOCK DIAGRAM



APPLICATION INFORMATION

The IS31BL3555 is a highly integrated current-mode boost HBLED driver with integrated switching FET and two LED current sinks. It is designed to drive two LED strings of up to 12 white LEDs in series, with current up to 200mA per string. An adaptive headroom control feature automatically adjusts the output boost stage to the minimum voltage (V_{OUT}) required to power the LED strings (V_{STRx}). This is expressed by the following Equation (1):

$$V_{OUT} = Max(V_{STR1}, V_{STR2}) + V_{CH} \quad (1)$$

Where V_{STRx} is the voltage drop across LED strings 1 through 2, and V_{CH} is the headroom (regulation) voltage of the LED current sinks (typically 0.72V at the maximum LED current). The dynamic headroom control will adjust the VOUT to equal the sum of the highest LED string voltage plus the IS31BL3555 operating headroom voltage.

INITIAL POWER UP SEQUENCE

The power-up sequence is shown in Figure 18. The IS31BL3555 integrates a UVLO/Regulator function which monitors the supply voltage level at the VCC input pin. The IS31BL3555 will power up only when the supply voltage is above the internal UVLO threshold level of 4.35V (max) and the EN/PWM pin is pulled high. During the power up sequence, the IS31BL3555 will check if any CHx pins are shorted to ground and/or are not used as shown in Figure 39.

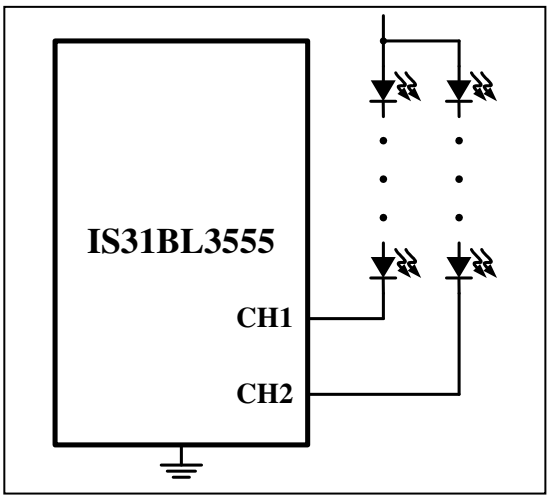
Once any of the CHx pin voltage rises above 120mV, a delay of between 3000 and 4000 clock cycles must pass before pin status detection is enabled. Therefore the LED detection period will vary depending on the switching frequency, as shown in the following table:

Switching Frequency (MHz)	Detection Time (ms)
1	3 ~ 4
0.800	3.75 ~ 5.0
0.600	5.0 ~ 6.7

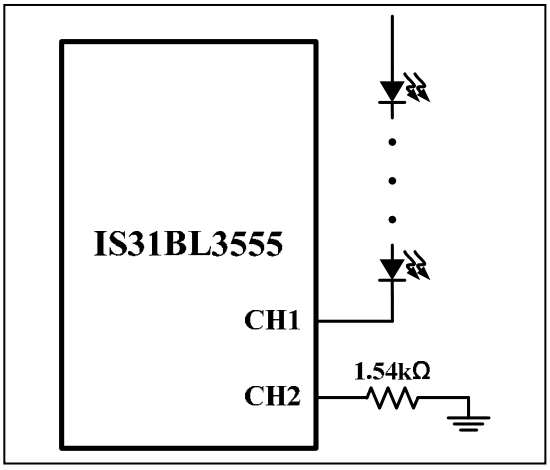
The CHx pin voltage thresholds used in detecting short/open LED conditions are as follows:

CHx	LED Pin Status	Action
<35mV	Short to ground	Power-up is halted
<220mV	Not used	LED removed from operation
>220mV	LED pin in use	None

As shown in Figure 39, any unused CHx pins should be connected with a 1.54kΩ resistor to ground. The CHx pin with a pull-down resistor will be ignored and will not be used for adaptive headroom control in Equation (1).



(A)



(B)

Figure 39 Channel Select Setup: (A) Using All Two Channels And (B) Using Only CH1.

If any CHx short to ground (V_{CHx}<35mV) is detected, the IS31BL3555 will not soft start until the short condition is removed. This protects the LED strings from an uncontrolled amount of current at power up due to shorted CHx pins.

SOFT START

When in soft start mode, the CHx pins will initially sink the soft start current (I_{CH_SS}). As the CHx pin voltage rises above 220mV, the IS31BL3555 will set the boost switch current limit to the I_{SW_LIM1} level and proceed to increase the LED current to the level set by the I_{SET} resistor value. This is shown in Figure 27

ENABLING THE IC

The IS31BL3555 will turn on when a logic high (> t_{PWM_ON}) on EN/PWM pin and the VCC voltage rises above 4.35V to clear the UVLO (V_{UVLO_R}) threshold.

A logic low on the EN/PWM pin will completely shut down the IS31BL3555. It will not power-up if the FR/SYNC pin is pulled low.

SWITCHING FREQUENCY SELECTION

A resistor connected to the FR/SYNC pin is used to set the boost regulator's switching frequency from 200kHz to 1MHz. Figure 11 shows the typical switching frequencies, in MHz, for resistor values, in kΩ.

$$R_{FSET} = 15 / f_{SW}$$

The FR/SYNC pin is clamped to a maximum switching frequency of 3.5MHz if a fault occurs during operation. It will shut down when the FR/SYNC pin is shorted to GND.

SYNCHRONIZE

The FR/SYNC pin can be used as a synchronization input, allowing the IS31BL3555 to operate with an external clock in the range of 580kHz to 1MHz as long as it satisfies the 150ns requirements of t_{SY_ON} and t_{SY_OFF}. When an external synchronization clock is applied to the FR/SYNC pin, the internal oscillator is over-driven so that each switching cycle begins at the rising edge of external clock. The IS31BL3555 will not be enabled if the FR/SYNC pin is held low during power-up. Only when the FR/SYNC pin is tri-stated to allow the pin to rise, to about 1V, or when a synchronization clock is detected, will the IS31BL3555 try to power-up.

Figure 40 shows the timing for a synchronization clock into the IS31BL3555 at 1MHz. Thus any pulse with a duty cycle of 15% to 85% at 1MHz can be used to synchronize the IC.

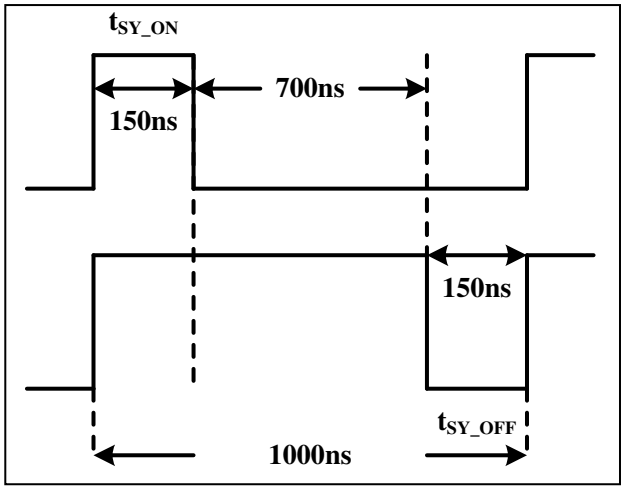


Figure 40 SYNC Pulse On And Off Time Requirements

The SYNC pulse duty cycle ranges for selected switching frequencies are:

SYNC Pulse Frequency(MHz)	Duty Cycle Range(%)
1	15 ~ 85
0.800	12 ~ 88
0.600	9 ~ 91

If the clock is lost, the IC will revert to the preset switching frequency set by the R_{FSET} resistor. The IC will stop switching during this period for a maximum period of about 7μs to allow the sync detection circuitry to switch over to the resistor preset switching frequency. Figure 28 shows the synchronized normal operation of the external sync signal and switching frequency. Figure 29 shows the switching frequency locking to the external sync signal. LED current does vary during the frequency changeover.

Keeping the FR/SYNC pin lower than 0.4V for greater than 7μs will effectively shut down the IS31BL3555. If the FR/SYNC pin is held low during power-up, the IC will not power-up. Normal operation is resumed when the FR/SYNC pin is released and rises above 1V which starts the soft-start sequence. The IC can be placed into a low-power mode by keeping the EN pin low for 32,750 clock cycles.

SETTING LED CURRENT

The I_{SET} pin is used to set the I_{LED} channel current from 40mA up to a maximum of 200mA. To adjust the I_{LED} current, the resistor, R_{ISET}, is selected according to the following Formula (2):

$$R_{ISET} = (1.000 \times 2000) / I_{LED} \qquad (2)$$

Where I_{LED} is in Amps and R_{ISET} is in Ω. This sets the maximum channel current, referred to as the peak current.

Sample standard R_{ISET} values with the corresponding I_{LED} current are as follows:

Standard Closest Resistor, R_{ISET} (kΩ)	LED Current, I_{LED} (mA)
10.0	200
25	80
33.4	60

PWM DIMMING

A PWM signal in the range of 200Hz ~ 1kHz applied to the EN/PWM pin will adjust the average LED current for all enabled channels. The PWM duty cycle sets the average LED current by turning on and off the current sinks. During the "high level" period of the PWM signal, the current sinks are turned ON at peak current level. During the "low level" period the current sinks are turned OFF and only critical internal circuits are kept active resulting in minimal power consumption. Figures 22 to 25 provide examples of PWM switching behavior.

PWM signal to LED current delay is less than 1μs typically, which allows greater accuracy at low PWM dimming duty cycles, as shown in Figure 14.

APWM PIN

As shown in Figure 41, the APWM pin is used to trim the LED peak current set by the R_{ISET} resistor. The duty cycle of this 20kHz to 1MHz digital signal will adjust the internally I_{SET} current. The duty cycle of this signal is inversely proportional to the percentage of current that is delivered to the LEDs (Shown in Figure 15). There is a several millisecond propagation delay between applying an APWM signal and the change in LED current peak current. This effect is shown in Figures 30~32.

The APWM pin should be connected to ground if it is not used.

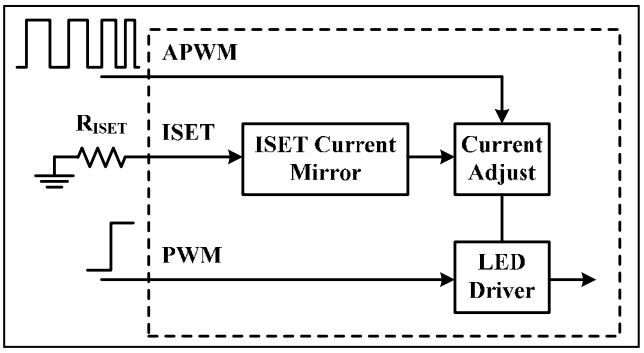


Figure 41 Simplified Block Diagram Of The APWM And ISET Circuit

When using the APWM input to trim the LED current, the R_{ISET} should selected for an LED current at least 5% higher than the desired peak current. The LED current is then trimmed down to the desired value. The trim down percentage corresponds to the APWM duty cycle. Therefore duty cycles between 30% and 60% will result in LED current trim from 30% and 60%. (Shown in Figure 16, I_{CH}=200mA).

For example, a peak LED current of 80mA (set by R_{ISET}) would deliver 60mA of current per LED sink if an APWM signal is applied with a duty cycle of 25% (Figures 30 and 31).

Although the order in which APWM and the PWM signal are enabled does not matter, the APWM signal should be enable before the PWM signal when actively adjusting the IS31BL3555 to output a lower current. This is to prevent the light intensity from changing during power up of the IC. Figure 20 shows the sequence of applying APWM before the PWM signal during power-up to prevent inadvertent light intensity changes.

For the best APWM dimming accuracy it is recommended to use frequency ranges between 50 and 500kHz.

ANALOG DIMMING

The LED current can also be dimmed by using an external DAC or another voltage source applied either directly to the ground side of the R_{ISET} resistor or through an external resistor to the ISET pin (Figure 42). For this type of dimming the I_{SET} range 20μA ~ 100μA will set the dimming limits.

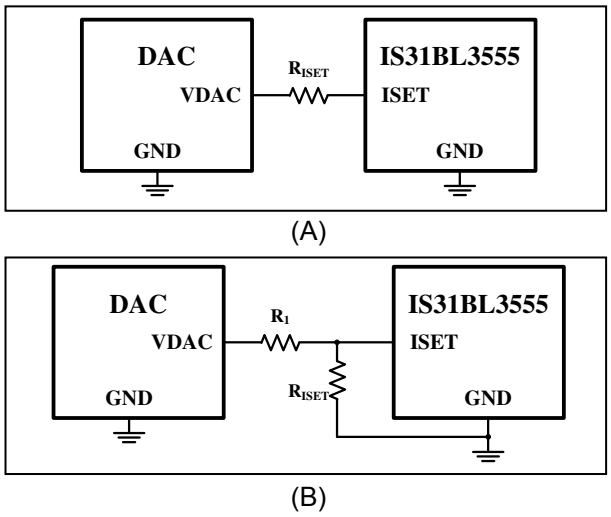


Figure 42 Simplified diagrams of voltage control of I_{LED}: typical applications using a DAC to control I_{LED} using a single resistor (upper), and dual resistors (lower).

• For Figure 42A, the I_{SET} current is calculated by the following Formula (3). The LED can only be decreased from the peak current set by R_{ISET}.

$$I_{SET} = \frac{V_{SET} - V_{DAC}}{R_{ISET}} \qquad (3)$$

Where V_{SET} is the I_{SET} pin voltage (1V typ) and V_{DAC} is the DAC output voltage. The LED current is maximum value when the DAC voltage is 0V. Select R_{ISET} resistor so the I_{SET} current is in the range of 20μA ~ 100μA to maintain stability of the internal gain amplifier.

• For the dual-resistor configuration (Figure 42B), the I_{SET} current is calculated by the following Formula (4). The LED current can be increased or decreased.

$$I_{SET} = \frac{V_{SET}}{R_{ISET}} - \frac{V_{DAC} - V_{SET}}{R_1} \qquad (4)$$

For this resistor circuit the LED current can be increased or decreased.by adjusting the DAC voltage higher or lower. The LED current can be made higher or lower than the current set by the R_{ISET} resistor:

- V_{DAC}= 1.000V; R_{ISET} controls current output
- V_{DAC}> 1.000V; the LED current is reduced
- V_{DAC}< 1.000V; the LED current is increased

LED SHORT DETECT

The IS31BL3555 integrates an LED short-circuit protection circuit. If the voltage at any of the two channel pins exceeds a threshold of approximately V_{CH_S} during normal operation, the corresponding string is turned off and is latched off (Figure 36). This is to prevent the IC from dissipating too much power by having a large voltage present on a CHx pin.

To prevent false tripping of an LED short event, the IS31BL3555 rechecks the disabled LED string every time the PWM signal goes high. This enables self-correction for an intermittent LED pin short.

OVERVOLTAGE PROTECTION

The IS31BL3555 integrates an OVP circuit and open Schottky diode protection to prevent system damage should the output voltage become excessive. The OVP protection default level is 8.1V and can be increased to 53V by connecting a resistor R_{OVP} from the OVP pin to VOUT. When the current into the OVP pin exceeds 199μA (typical), the OVP comparator goes low and stops the switching.

The following Equation (5) can be used to determine the resistance for setting the OVP level:

$$R_{OVP} = \frac{V_{OVP\_OUT} - V_{OVP1}}{I_{OVPS}} \qquad (5)$$

Where: V_{OVP_OUT} is the target overvoltage level, R_{OVP} is the value of the external resistor, in Ω, V_{OVP1} is the pin OVP threshold found in the Electrical Characteristics Table, and I_{OVPS} is the sense current into the OVP pin.

The two most common reasons for an OVP condition are: a disconnected output, and an open LED string. Examples of these are provided in Figures 34 and 35.

Figure 34 shows when the output of the IS31BL3555 is disconnected from the load during normal operation. The output voltage V_{OUT} immediately increases to the OVP voltage level which then stops the switching to prevent damage to the IC. Switching will resume once V_{OUT} discharges to below the OVP threshold and will stop if V_{OUT} increases above the OVP threshold.

Figure 35 displays a typical OVP event caused by an open LED string. After the OVP condition is detected, the IS31BL3555 stops switching, the open LED string is disabled and V_{OUT} begins to drop. The switching will resume and the IS31BL3555 continues with normal operation.

IS31BL3555 also has secondary overvoltage protection for the internal switch (SW pin). In the event of an open schottky diode the voltage on the SW pin (V_{SW}) may exceed 60V, which is above the device safe operating voltage rating. Under this condition the secondary overvoltage protection will disable the IS31BL3555 and remain in a latched off condition. To clear the latch and resume operation, the IS31BL3555 must be shut down by either lowering the supply voltage below the UVLO threshold or by driving the EN/PWM pin as shown in Figure 21.

If the IS31BL3555 is enabled with an open diode condition, it will go through all its initial LED detection procedure and then try to enable the switcher, at which time the open diode is detected the device shuts down as shown in Figure 33.

INPUT UVLO

The IS31BL3555 will be enabled when V_{CC} and V_{SENSE} rise above the V_{UVLO_R} threshold. It will be disabled when V_{CC} falls below the V_{UVLO_F} threshold for more than 50μs. This small delay is used to avoid shutting down because of momentary glitches in the input power supply. It will shut down if V_{CC} falls below 4.35V, (see Figure 17).

VDD

The IS31BL3555 has an internal LDO to support internal circuits and provide a pull-up voltage (3.5V typ) for the FAULTB pin. The current is limited to <2mA and a capacitor C_{VDD} (≥1μF) should be connected to the VDD pin.

SHUTDOWN

The IS31BL3555 enters a shutdown mode and clears all internal fault registers when the EN/PWM pin is pulled low for more than t_{PWM_OFF} (32,750 clock cycles). With a 1MHz clock frequency, it will take approximately 33ms to shut down (Figure 26). When the IS31BL3555 is shut down, all current sources are disabled. A high level on the EN/PWM will remove the shutdown condition. For a faster shutdown, the FR/SYNC pin can be pulled low.

FAULT PROTECTION DURING OPERATION

The IS31BL3555 constantly monitors the state of the system in order to determine whether there is any fault condition. The response to a triggered fault condition is summarized in the Fault Mode Table 1.

The device can detect these fault conditions:

- Open/short LED string
- FSET or ISET pins shorted to ground
- Open boost schottky diode
- Over temperature (OTP)

TABLE 1 FAULT MODE

Fault Name	Type	Active	Flag	Description	Boost	Sink Driver
Primary switch overcurrent protection (Cycle-by-cycle current limit)	Auto-restart	Always	No	This fault condition is triggered by the cycle-by-cycle current limit, I_{SW_LIM1}	Off for a single cycle	On
Secondary OVP	Latched	Always	Yes	Secondary overvoltage protection is used for open diode detection. When diode D1 opens, the SW pin voltage will increase until V_{OVP2} is reached. This fault latches the IC and the fault flag is set. To re-enable the part the EN/PWM pin must be pulled low for 32,750 clock cycles.	Off	Off
LED pin short protection	Auto-restart	Startup	No	This fault prevents the device from starting-up if either of the CHx pins are shorted. The device stops soft-start from starting while either of the CHx pins are determined to be shorted. After the short is removed, soft-start is allowed to start.	Off	Off
LED pin open	Auto-restart	Normal Operation	No	When a CHx pin is open the device will determine which LED pin is open by increasing the output voltage until OVP is reached. Any LED string not in regulation will be turned off. The device will then go back to normal operation by reducing the output voltage to the appropriate voltage level.	On	Off for open pins. On for all others.
ISET short protection	Auto-restart	Always	No	This fault occurs when the ISET current goes above 150% of the maximum current. The boost will stop switching and the IC will disable the LED sinks until the fault is removed. When the fault is removed the IC will try to regulate to the preset LED current.	Off	Off
FR/SYNC short protection	Auto-restart	Always	Yes	Fault occurs when the FR/SYNC current goes above the protection threshold, about 256μA. The boost will stop switching and the IC will disable the LED sinks until the fault is removed. When the fault is removed the IC will try to restart with soft-start.	Off	Off
Overvoltage protection	Auto-restart	Always	No	Fault occurs when OVP pin exceeds V_{OVPS} threshold. The IC will immediately stop switching to try to reduce the output voltage. If the output voltage decreases then the IC will restart switching to regulate the output voltage.	Stop during OVP event	On
LED short protection	Auto-restart	Always	No	Fault occurs when the LED pin voltage exceeds V_{CH_S}. When the LED short protection is detected the LED string that is above the threshold will be removed from operation.	On	Off for shorted pins. On for all others.
Over temperature protection	Auto-restart	Always	No	Fault occurs when the die temperature exceeds the over temperature threshold, 165°C.	Off	Off
VCC UVLO	Auto-restart	Always	No	Fault occurs when V_{CC} drops below V_{UVLO}, 3.9V maximum. This fault resets all latched faults.	Off	Off

CLASSIFICATION REFLOW PROFILES

Profile Feature	Pb-Free Assembly
Preheat & Soak Temperature min (Tsmin) Temperature max (Tsmax) Time (Tsmin to Tsmax) (ts)	150°C 200°C 60-120 seconds
Average ramp-up rate (Tsmax to Tp)	3°C/second max.
Liquidous temperature (TL) Time at liquidous (tL)	217°C 60-150 seconds
Peak package body temperature (Tp)*	Max 260°C
Time (tp)** within 5°C of the specified classification temperature (Tc)	Max 30 seconds
Average ramp-down rate (Tp to Tsmax)	6°C/second max.
Time 25°C to peak temperature	8 minutes max.

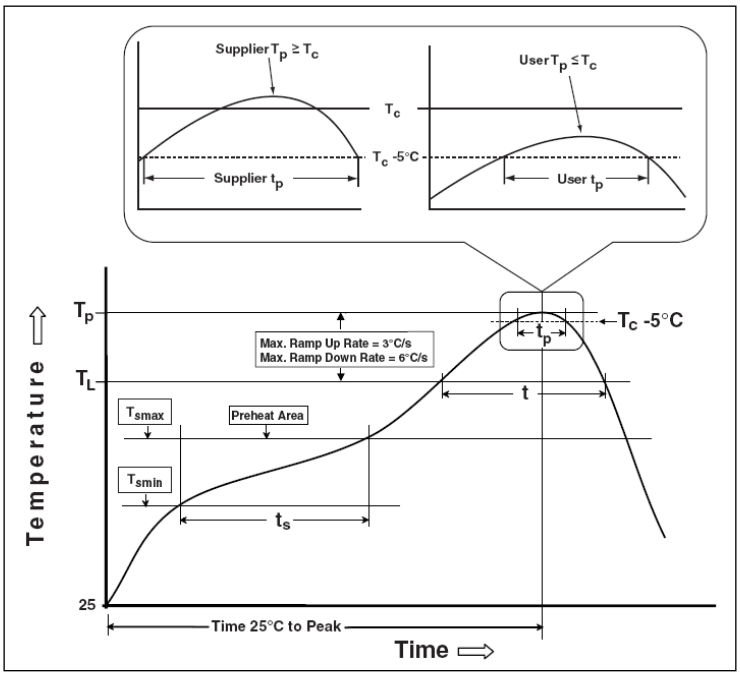
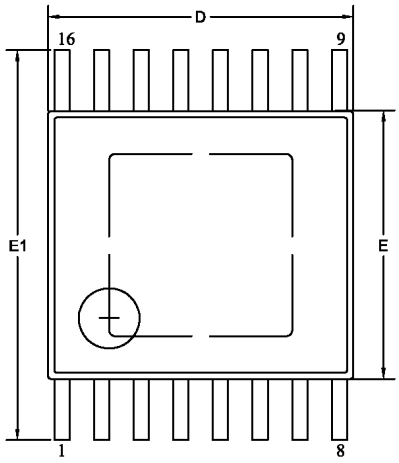


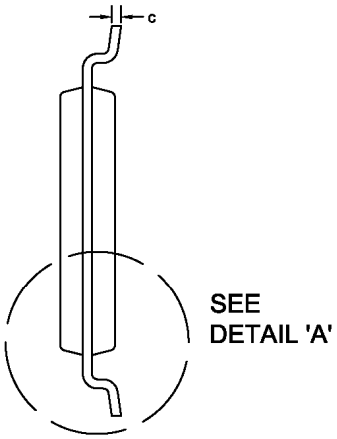
Figure 43 Classification Profile

PACKAGE INFORMATION

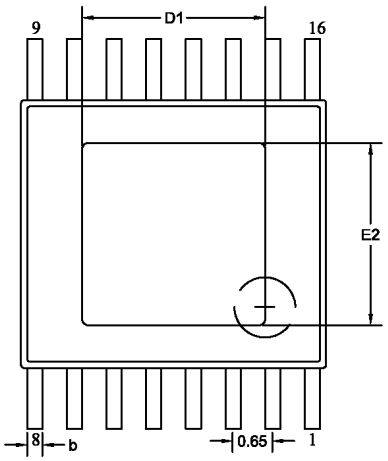
eTSSOP-16



TOP VIEW

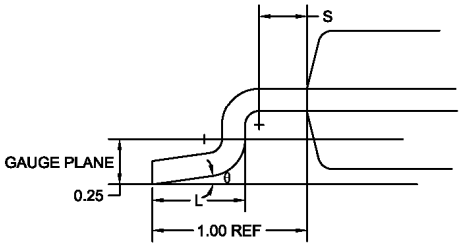


END VIEW

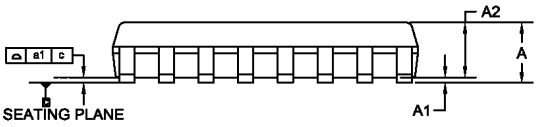


BOTTOM VIEW

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	—	—	1.20
A1	0.00	—	0.15
A2	0.80	0.90	1.05
D	4.90	5.00	5.10
D1	1.70		3.10
E	4.30	4.40	4.50
E1	6.40BSC		
E2	1.50		3.10
L	0.45	0.60	0.75
b	0.19	—	0.30
S	0.20		
c	0.09	—	0.20
θ	0°		8°
a1	0.10		



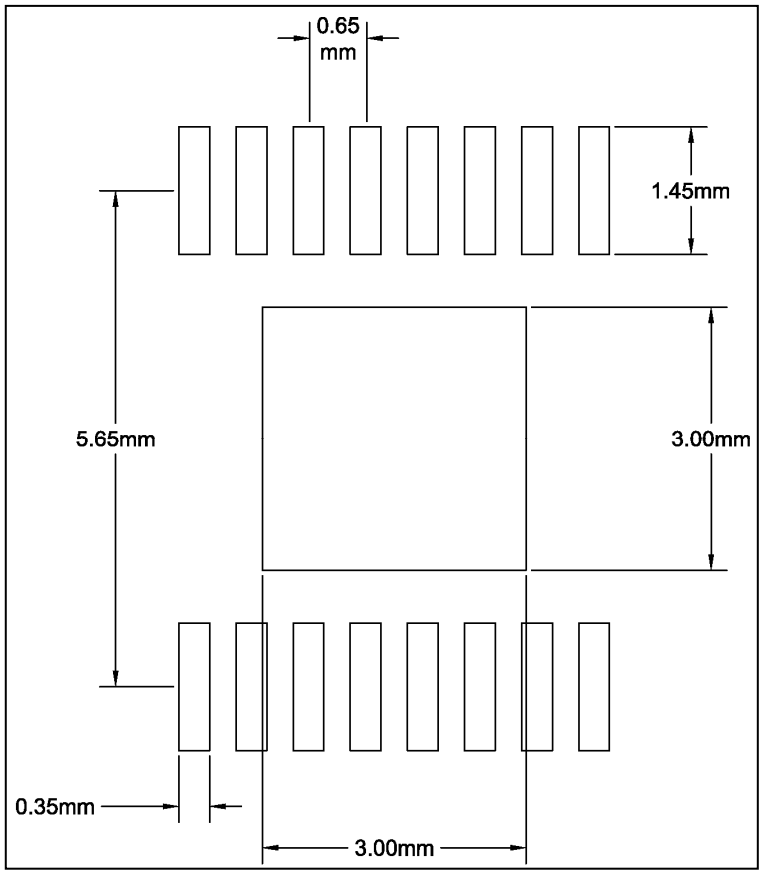
DETAIL 'A'



SIDE VIEW

NOTES:
The thermal pad shows different shape among different factories.

RECOMMENDED LAND PATTERN



Note:

1. Land pattern complies to IPC-7351.
2. All dimensions in MM.
3. This document (including dimensions, notes & specs) is a recommendation based on typical circuit board manufacturing parameters. Since land pattern design depends on many factors unknown (eg. User's board manufacturing specs), user must determine suitability for use.

REVISION HISTORY

Revision	Detail Information	Date
0A	Initial release	2017.09.08