LVDS CLOCK MULTIPLIER FOR VIDEO APPLICATIONS

ICS874S336

General Description

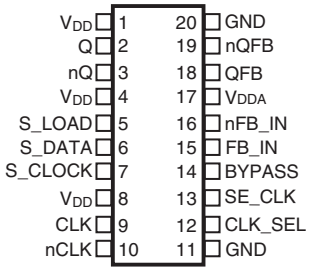
The ICS874S336 is a high performance, 1-to-1, Differential-to-LVDS Clock Multiplier and is a member of the HiPerClocksS™family of High Performance Clock Solutions from IDT. The CLK/ nCLK input pair can accept most standard differential input levels. The ICS874S336 has a fully integrated PLL along with frequency configurable outputs. An external feedback output regenerates clocks with “zero delay”.

The ICS874S336 has multiple divide combinations designed to work with the most common video rates used in professional video systems.

Features

- One LVDS differential output pair, plus one LVDS feedback output pair
- One differential clock input pair CLK/nCLK can accept the following differential input levels: LVPECL, LVDS, LVHSTL, HCSL, SSTL
- Input Frequency Range: 14MHz to 17MHz
- Maximum Output Frequency: 204MHz
- VCO range: 1.2GHz – 2GHz
- Cycle-to-cycle jitter: TBD
- 3.3V operating supply voltage
- Low PLL bandwidth allows for better jitter attenuation
- 0°C to 70°C ambient operating temperature
- Available in both standard (RoHS 5) and lead-free (RoHS 6) packages

Pin Assignment

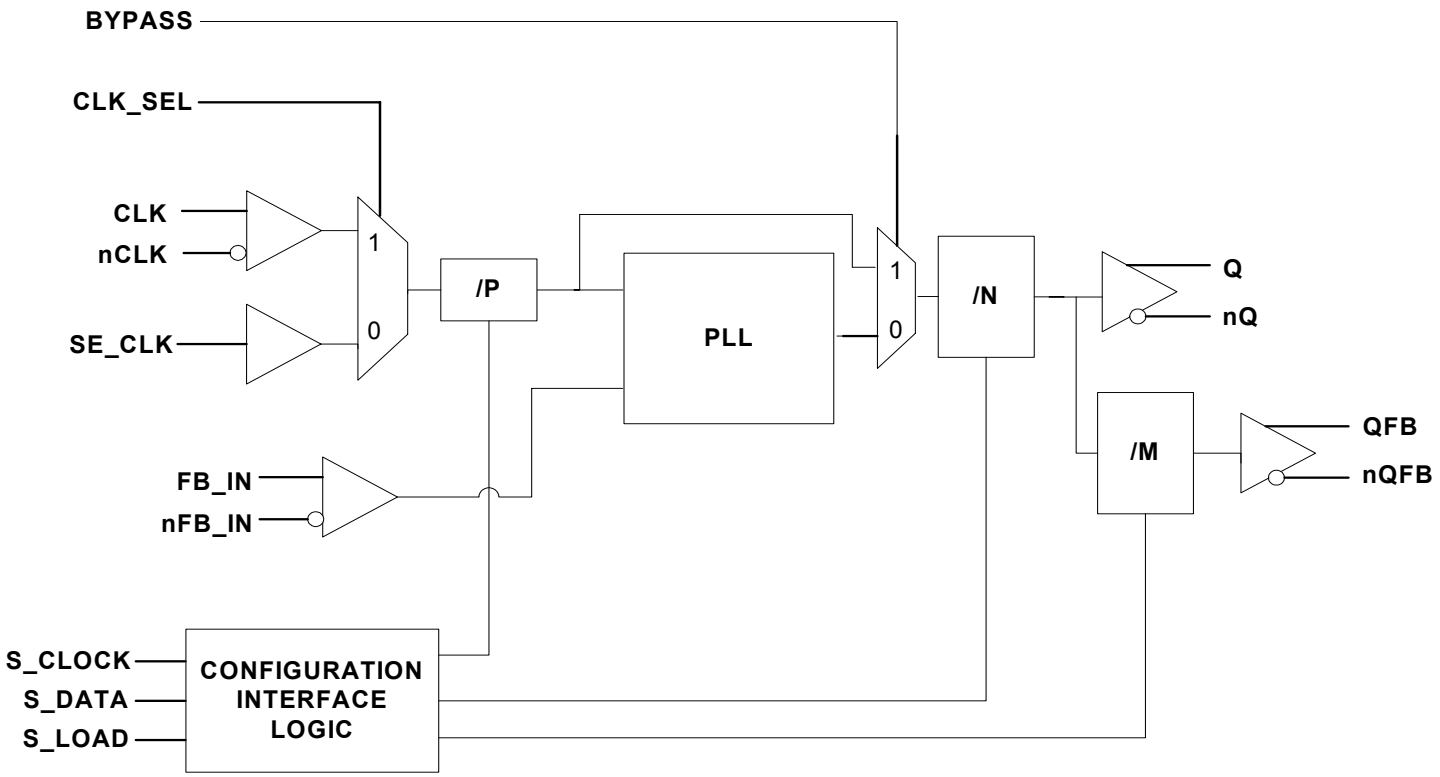


ICS874S336I
20-Lead TSSOP
6.5mm x 4.4mm x 0.925mm
package body

G Package
Top View

The Preliminary Information presented herein represents a product in pre-production. The noted characteristics are based on initial product characterization and/or qualification. Integrated Device Technology, Incorporated (IDT) reserves the right to change any circuitry or specifications without notice.

Block Diagram



Functional Description

The ICS874S336 features a fully integrated PLL and therefore requires no external components for setting the loop bandwidth. The VCO of the PLL operates over a range of 1.2GHz to 2GHz. The output of the M divider is also applied to the phase detector.

The phase detector and the M divider force the VCO output frequency to be M times the reference frequency by adjusting the VCO control voltage. Note that for some values of M (either too high or too low), the PLL will not achieve lock. The output of the VCO is scaled by a divider prior to being sent to each of the LVPECL output buffers. The divider provides a 50% output duty cycle.

The relationship between the VCO frequency, the input frequency and the M divider is defined as follows:

$$fVCO = \frac{fIN \times M \times N}{P} \times 2$$

The M, N, and P values used to obtain the proper video frequencies are found in Table 3B, *Programmable VCO Frequency Function Table.* The actual data bits can be found in Tables 3C, 3D and 3E.

Serial operation occurs when S_LOAD is LOW. The shift register is loaded by sampling the S_DATA bits with the rising edge of S_CLOCK. The contents of the shift register are loaded into the M, N and P dividers when S_LOAD transitions from LOW-to-HIGH. The divide values are latched on the HIGH-to-LOW transition of S_LOAD. If S_LOAD is held HIGH, data at the S_DATA input is passed directly to the dividers on each rising edge of S_CLOCK. The serial mode can be used to program the M, N and P bits.

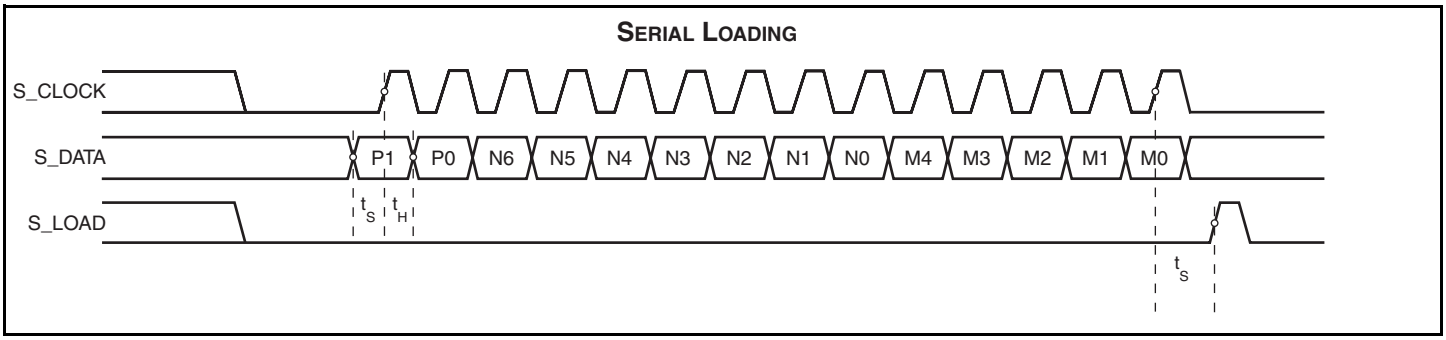


Figure 1. Serial Load Operation

Table 1. Pin Descriptions

Number	Name	Type		Description
1, 4, 8	V_{DD}	Power		Core supply pins.
2, 3	Q, nQ	Output		Differential output pair. LVDS interface levels.
5	S_LOAD	Input	Pulldown	Controls transition of data from shift register into the dividers. LVCMOS/LVTTL interface levels.
6	S_DATA	Input	Pulldown	Shift register serial input. Data sampled on the rising edge of S_CLOCK. LVCMOS/LVTTL interface levels.
7	S_CLOCK	Input	Pulldown	Clocks in serial data present at S_DATA input into the shift register on the rising edge of S_CLOCK. LVCMOS/LVTTL interface levels.
9	CLK	Input	Pulldown	Non-inverting differential clock input.
10	nCLK	Input	Pullup/Pulldown	Inverting differential clock input. $V_{DD}/2$ default when left floating.
11, 20	GND	Power		Negative supply pin.
12	CLK_SEL	Input	Pullup	Selects the reference clock. When LOW selects SE_CLK as the clock source. When HIGH selects CLK, nCLK as the clock source. LVCMOS/LVTTL interface levels.
13	SE_CLK	Input	Pulldown	Single-ended clock input. LVCMOS/LVTTL interface levels.
14	BYPASS	Input	Pulldown	Selects between the PLL and reference clock as the input to the dividers.When LOW, selects PLL. When HIGH, selects reference clock. LVCMOS/LVTTL interface levels.
15	FB_IN	Input	Pulldown	Non-inverting differential clock input.
16	nFB_IN	Input	Pullup/Pulldown	Inverting differential clock input. $V_{DD}/2$ default when left floating.
17	V_{DDA}	Power		Analog supply pin.
18, 19	QFB, nQFB	Output		Differential output pair. LVDS interface levels.

NOTE: *Pullup and Pulldown* refer to internal input resistors. See Table 2, *Pin Characteristics,* for typical values.

Table 2. Pin Characteristics

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance			4		pF
R_{PULLUP}	Input Pullup Resistor			51		kΩ
$R_{PULLDOWN}$	Input Pulldown Resistor			51		kΩ

Function Tables

Table 3A. Parallel and Serial Mode Function Table

Inputs			
S_LOAD	**S_CLOCK**	**S_DATA**	**Conditions**
L	X	X	Data is latched into input registers and remains loaded until next LOW transition or until a serial event occurs.
L	↑	Data	Shift register is loaded with data on S_DATA on each rising edge of S_CLOCK.
↑	L	Data	Contents of the shift register are passed to the M, N and P dividers.
↓	L	Data	M, N and P divider values are latched.
L	X	X	Serial input do not affect shift registers.
H	↑	Data	S_DATA passed directly to M, N and P dividers as it is clocked.

NOTE: L = LOW
H = HIGH
X = Don't care
↑ = Rising edge transition
↓ = Falling edge transition

Table 3B. Device Configuration Table

Input Frequency (MHz)		P Divide Value	N Divide Value	M Divide Value	Output Frequency (MHz)	
Min	**Max**				**Min**	**Max**
14	17	1	10	12	168	204
14	17	1	10	10	140	170
14	17	2	12	17	119	144.5
14	17	4	14	28	98	119
14	17	4	16	24	84	102
14	17	4	20	20	70	85
14	17	4	22	17	59.5	72.25
14	17	4	28	14	49	59.5
14	17	4	32	12	42	51
14	17	8	38	20	35	42.5
14	17	8	46	17	29.75	36.125
14	17	8	56	14	24.5	29.75
14	17	8	64	12	21	25.5
14	17	8	80	10	17.5	21.25
14	17	8	100	8	14	17
14	17	8	110	7	12.25	14.875
14	17	8	130	6	10.5	12.75
14	17	8	160	5	8.75	10.6

Table 3C. Pre-Divider (P) Configuration Table

P Divide	P1	P0
1	0	0
2	0	1
4	1	0
8	1	1

Table 3D. Output Divider (N) Configuration Table

N Divide	N6	N5	N4	N3	N2	N1	N0
10	0	0	0	0	1	0	1
12	0	0	0	0	1	1	0
14	0	0	0	0	1	1	1
16	0	0	0	1	0	0	0
20	0	0	0	1	0	1	0
22	0	0	0	1	0	1	1
28	0	0	0	1	1	1	0
32	0	0	1	0	0	0	0
38	0	0	1	0	0	1	1
46	0	0	1	0	1	1	1
56	0	0	1	1	1	0	0
64	0	1	0	0	0	0	0
80	0	1	0	1	0	0	0
100	0	1	1	0	0	1	0
110	0	1	1	0	1	1	1
130	1	0	0	0	0	0	1
160	1	0	1	0	0	0	0

Table 3E. Feedback Divider (M) Configuration Table

M Divide	M4	M3	M2	M1	M0
5	0	0	1	0	1
6	0	0	1	1	0
7	0	0	1	1	1
8	0	1	0	0	0
10	0	1	0	1	0
12	0	1	1	0	0
14	0	1	1	1	0
17	1	0	0	0	1
20	1	0	1	0	0
24	1	1	0	0	0
28	1	1	1	0	0

Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics or AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Item	Rating
Supply Voltage, V_{DD}	4.6V
Inputs, V_I	-0.5V to V_{DD} + 0.5V
Outputs, I_O (LVDS) Continuos Current Surge Current Outputs, I_O (LVDS) Continuos Current Surge Current	 10mA 15mA 50mA 100mA
Package Thermal Impedance, θ_{JA}	87.2°C/W (0 mps)
Storage Temperature, T_{STG}	-65°C to 150°C

DC Electrical Characteristics

Table 4A. LVDS Power Supply DC Characteristics, V_{DD} = 3.3V ± 5%, T_A = 0°C to 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Positive Supply Voltage		3.135	3.3	3.465	V
V_{DDA}	Analog Supply Voltage		V_{DD} – 0.15	3.3	V_{DD}	V
I_{DD}	Power Supply Current			115		mA
I_{DDA}	Analog Supply Current			15		mA

Table 4B. LVCMOS/LVTTL DC Characteristics, V_{DD} = 3.3V ± 5%, T_A = 0°C to 70°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage			2		V_{DD} + 0.3	V
V_{IL}	Input Low Voltage			-0.3		0.8	V
I_{IH}	Input High Current	SE_CLK, BYPASS, S_CLOCK, S_DATA, S_LOAD	V_{DD} = V_{IN} = 3.465V			150	µA
		CLK_SEL	V_{DD} = V_{IN} = 3.465V			5	µA
I_{IL}	Input Low Current	SE_CLK, BYPASS, S_CLOCK, S_DATA, S_LOAD	V_{DD} = 3.465V, V_{IN} = 0V	-5			µA
		CLK_SEL	V_{DD} = 3.465V, V_{IN} = 0V	-150			µA

Table 4C. Differential DC Characteristics, V_{DD} = 3.3V ± 5%, T_A = 0°C to 70°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
I_{IH}	Input High Current	CLK/nCLK, FB_IN/nFB_IN	$V_{DD} = V_{IN}$ = 3.465V			150	µA
I_{IL}	Input Low Current	CLK, FB_IN	V_{DD} = 3.465V, V_{IN} = 0V	-5			µA
		nCLK, nFB_IN	V_{DD} = 3.465V, V_{IN} = 0V	-150			µA
V_{PP}	Peak-to-Peak Voltage; NOTE 1			0.15		1.3	V
V_{CMR}	Common Mode Input Voltage; NOTE 1, 2			GND + 0.5		V_{DD} – 0.85	V

NOTE 1: V_{IL} should not be less than -0.3V.
NOTE 2: Common mode input voltage is defined as V_{IH}.

Table 4D. LVDS DC Characteristics, V_{DD} = 3.3V ± 5%, T_A = 0°C to 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OD}	Differential Output Voltage			370		mV
ΔV_{OD}	V_{OD} Magnitude Change			50		mV
V_{OS}	Offset Voltage			1.22		V
ΔV_{OS}	V_{OS} Magnitude Change			50		mV

Table 5. Input Frequency Characteristics, V_{DD} = 3.3V ± 5%, T_A = 0°C to 70°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
f_{IN}	Input Frequency	CLK/nCLK, SE_CLK; NOTE 1		14		17	MHz
		S_CLOCK				10	MHz

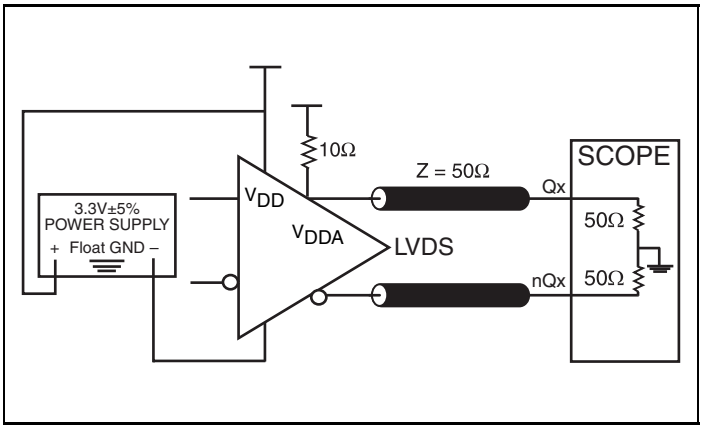
NOTE 1: For the CLK/nCLK and SE_CLK frequency range, the M value must be set for the VCO to operate within the TBD MHz to TBD MHz range.

Table 6. AC Characteristics, V_{DD} = 3.3V ± 5%, T_A = 0°C to 70°C

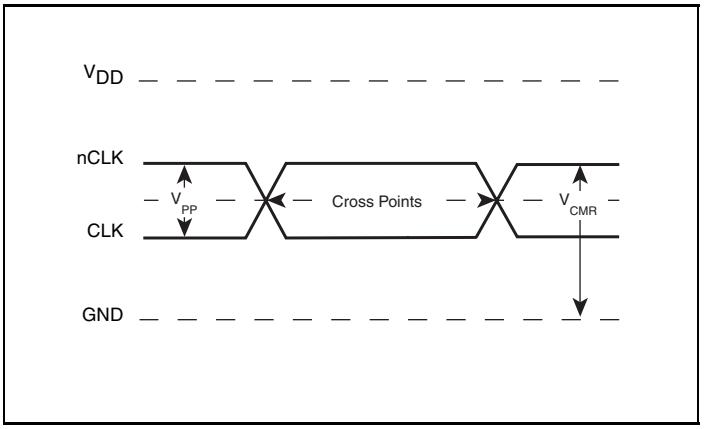
Parameter	Symbol	Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency		8.75		204	MHz
*t*jit(cc)	Cycle-to-Cycle Jitter; NOTE 1			TBD		ps
t(Ø)	Static Phase Offset; NOTE 1			TBD		ps
*t*jit(per)	Period Jitter, RMS; NOTE 1			TBD		ps
t_R / t_F	Output Rise/Fall Time	20% to 80%		270		ps
odc	Output Duty Cycle			50		%

NOTE 1: This parameter is defined in accordance with JEDEC Standard 65.

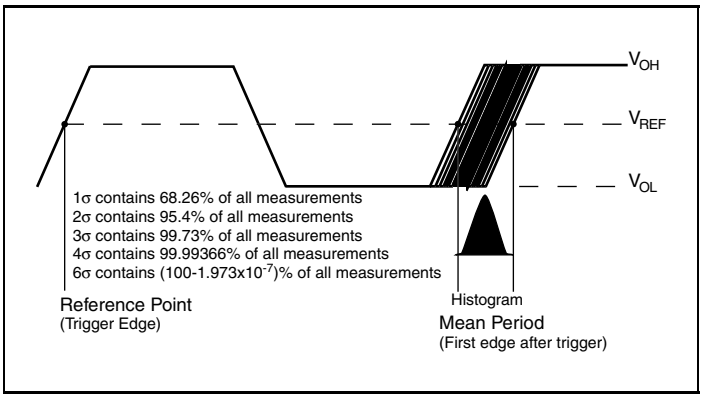
Parameter Measurement Information



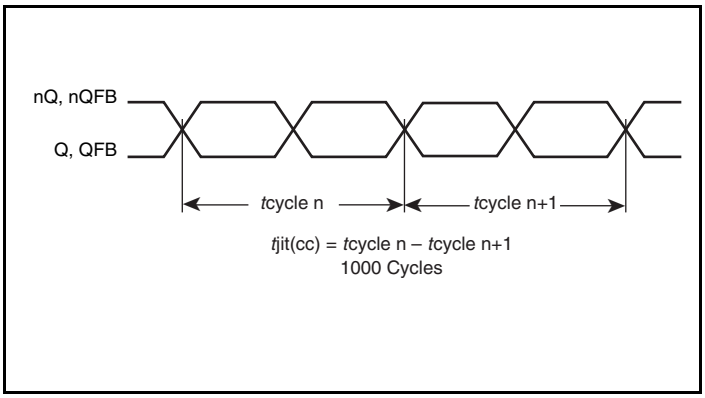
3.3V LVDS Output Load AC Test Circuit



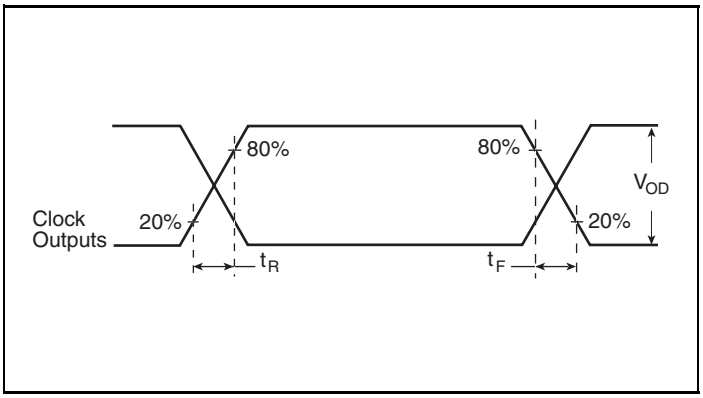
Differential Input Level



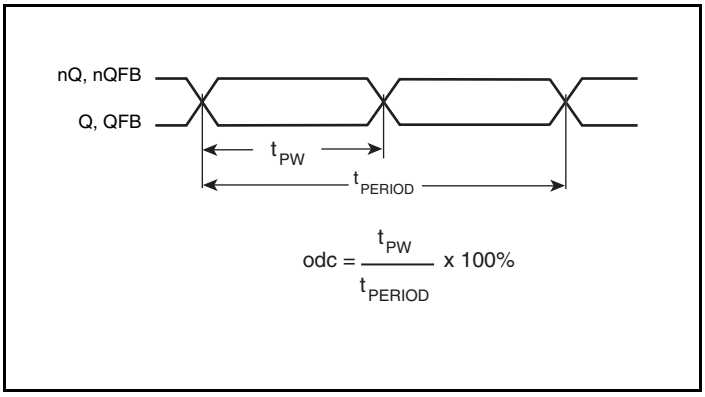
Period Jitter, RMS



Cycle-to-Cycle Jitter

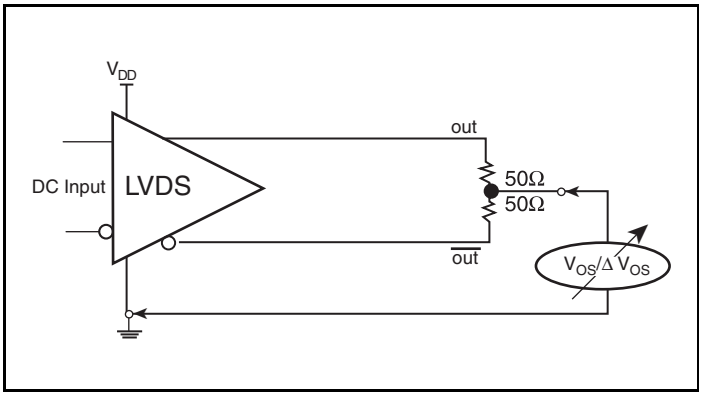


Output Rise/Fall Time

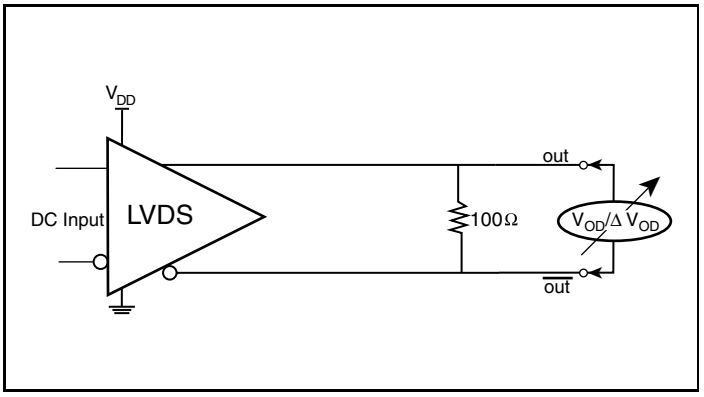


Output Duty Cycle/Pulse Width/Period

Parameter Measurement Information, continued



Offset Voltage Setup



Differential Output Voltage Setup

Application Information

Wiring the Differential Input to Accept Single-Ended Levels

Figure 2 shows how the differential input can be wired to accept single-ended levels. The reference voltage V_REF = V_{DD}/2 is generated by the bias resistors R1, R2 and C1. This bias circuit should be located as close as possible to the input pin. The ratio of R1 and R2 might need to be adjusted to position the V_REF in the center of the input voltage swing. For example, if the input clock swing is only 2.5V and V_{DD} = 3.3V, V_REF should be 1.25V and R2/R1 = 0.609.

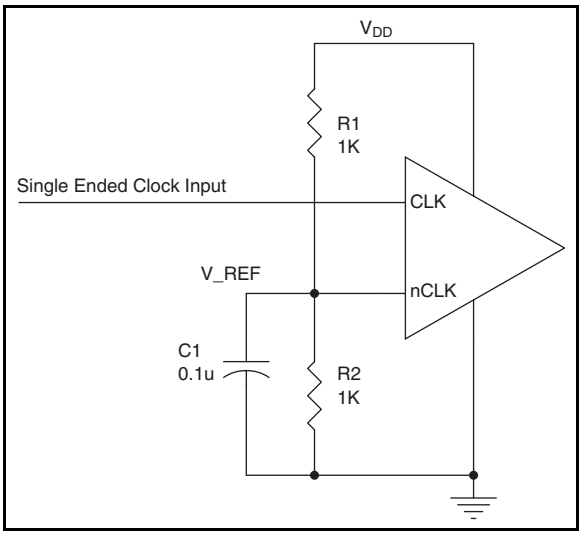


Figure 2. Single-Ended Signal Driving Differential Input

Differential Clock Input Interface

The CLK /nCLK accepts LVDS, LVPECL, LVHSTL, SSTL, HCSL and other differential signals. Both V_{SWING} and V_{OH} must meet the V_{PP} and V_{CMR} input requirements. *Figures 3A to 3F* show interface examples for the HiPerClockS CLK/nCLK input driven by the most common driver types. The input interfaces suggested here are examples only. Please consult with the vendor of the driver component to confirm the driver termination requirements. For example, in Figure 3A, the input termination applies for IDT HiPerClockS open emitter LVHSTL drivers. If you are using an LVHSTL driver from another vendor, use their termination recommendation.

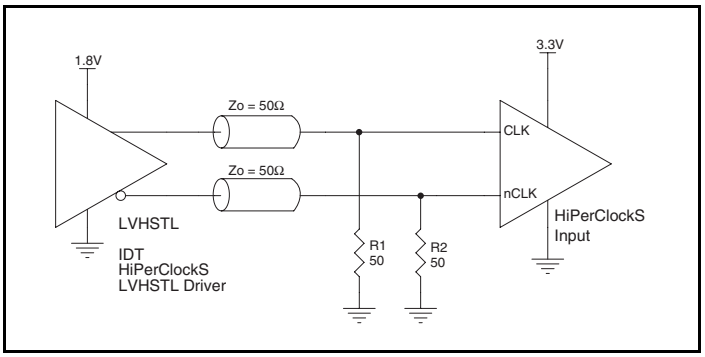


Figure 3A. HiPerClockS CLK/nCLK Input Driven by an IDT Open Emitter HiPerClockS LVHSTL Driver

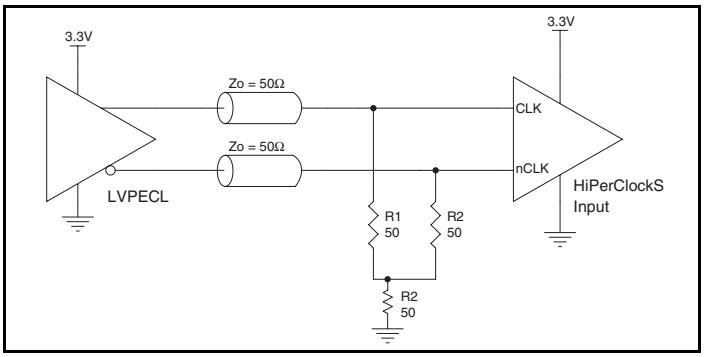


Figure 3B. HiPerClockS CLK/nCLK Input Driven by a 3.3V LVPECL Driver

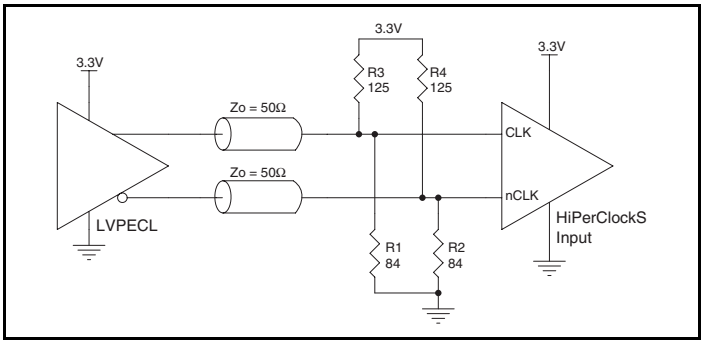


Figure 3C. HiPerClockS CLK/nCLK Input Driven by a 3.3V LVPECL Driver

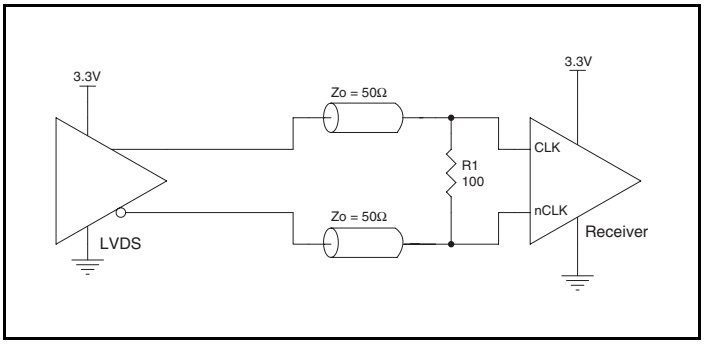


Figure 3D. HiPerClockS CLK/nCLK Input Driven by a 3.3V LVDS Driver

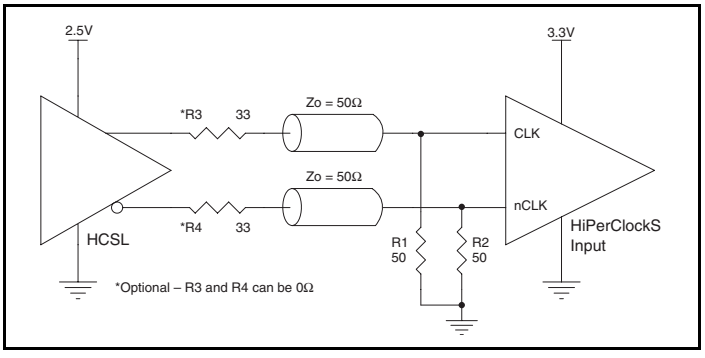


Figure 3E. HiPerClockS CLK/nCLK Input Driven by a 3.3V HCSL Driver

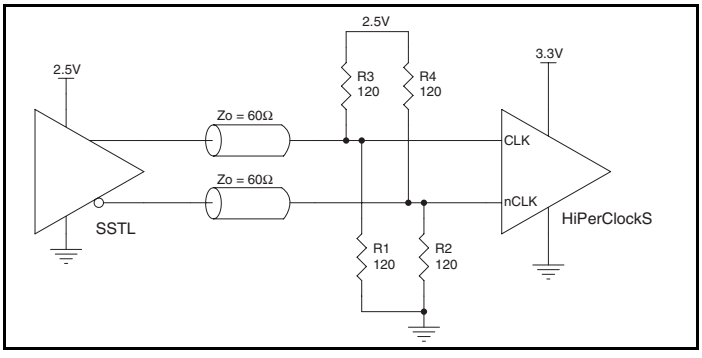


Figure 3F. HiPerClockS CLK/nCLK Input Driven by a 2.5V SSTL Driver

Power Supply Filtering Technique

As in any high speed analog circuitry, the power supply pins are vulnerable to random noise. The ICS874S336 provides separate power supplies to isolate any high switching noise from the outputs to the internal PLL. V_{DD} and V_{DDA} should be individually connected to the power supply plane through vias, and bypass capacitors should be used for each pin. To achieve optimum jitter performance, power supply isolation is required. *Figure 4* illustrates how a 10Ω resistor along with a 10μF and a 0.01μF bypass capacitor should be connected to each V_{DDA} pin.

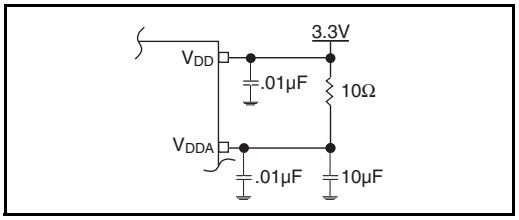


Figure 4. Power Supply Filtering

Recommendations for Unused Input and Output Pins

Inputs:

CLK/nCLK Inputs

For applications not requiring the use of the differential input, both CLK and nCLK can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from CLK to ground.

SE_CLK Input

For applications not requiring the use of a clock input, it can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from the SE_CLK input to ground.

LVCMOS Control Pins

All control pins have internal pull-ups or pull-downs; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

Outputs:

LVDS Outputs

All unused LVDS output pairs can be either left floating or terminated with 100Ω across. If they are left floating, there should be no trace attached.

3.3V LVDS Driver Termination

A general LVDS interface is shown in *Figure 5.* In a 100Ω differential transmission line environment, LVDS drivers require a matched load termination of 100Ω across near the receiver input.

For a multiple LVDS outputs buffer, if only partial outputs are used, it is recommended to terminate the unused outputs.

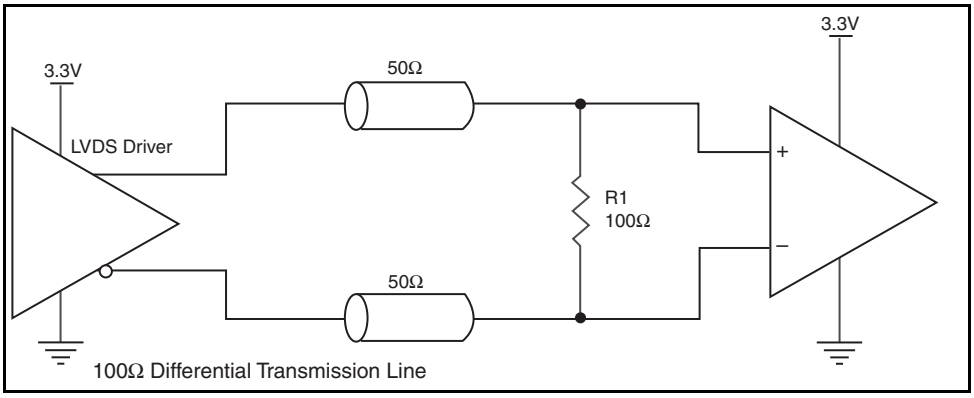


Figure 5. Typical LVDS Driver Termination

Schematic Example

Figure 6 shows an example of ICS874S336 application schematic. In this example, the device is operated at V_{DD} = 3.3V. The decoupling capacitors should be located as close as possible to the power pin. Two examples of LVDS terminations are shown in this schematic. The input is driven either by a 3.3V LVPECL driver or a 3.3V LVCMOS. .

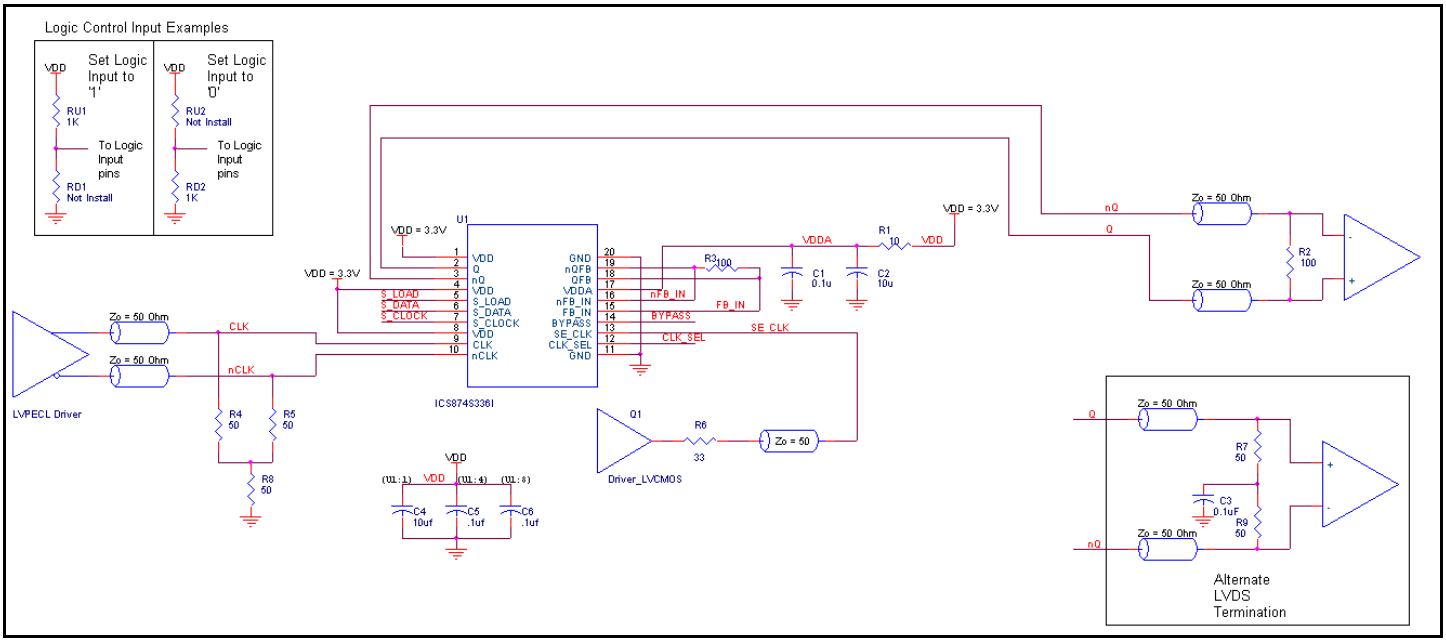


Figure 6. ICS874S336 Schematic Example

Power Considerations

This section provides information on power dissipation and junction temperature for the ICS874S336.
Equations and example calculations are also provided.

1. Power Dissipation.

The total power dissipation for the ICS74S336 is the sum of the core power plus the power dissipated in the load(s).
The following is the power dissipation for V_{DD} = 3.3V + 5% = 3.465V, which gives worst case results.

- Power (core)$_{MAX}$ = V_{DD_MAX} * (I_{DD_MAX} + I_{DDA_MAX}) = 3.465V * (115mA + 15mA) = **450.45mW**

2. Junction Temperature.

Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad and directly affects the reliability of the device. The maximum recommended junction temperature for HiPerClockS devices is 125°C.

The equation for Tj is as follows: Tj = θ_{JA} * Pd_total + T_A

Tj = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming no air flow and a multi-layer board, the appropriate value is 87.2°C/W per Table 7 below.

Therefore, Tj for an ambient temperature of 70°C with all outputs switching is:

70°C + 0.450W * 87.2°C/W = 109.2°C. This is well below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (single layer or multi-layer).

Table 7. Thermal Resistance θ_{JA} for 20 Lead TSSOP, Forced Convection

θ_{JA} **by Velocity**			
Meters per Second	**0**	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	87.2°C/W	82.9°C/W	80.7°C/W

Reliability Information

Table 8. θ_{JA} vs. Air Flow Table for a 20 Lead TSSOP

θ_{JA} by Velocity			
Meters per Second	**0**	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	87.2°C/W	82.9°C/W	80.7°C/W

Transistor Count

The transistor count for ICS874S336 is: 2434

Package Outline and Package Dimension

Package Outline - G Suffix for 20 Lead TSSOP

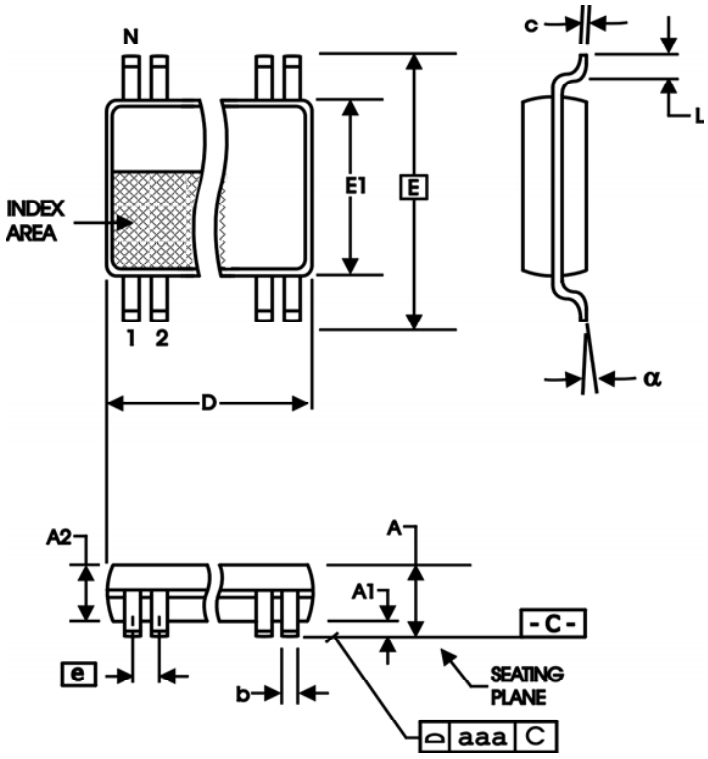


Table 9. Package Dimensions

All Dimensions in Millimeters		
Symbol	**Minimum**	**Maximum**
N	20	
A		1.20
A1	0.05	0.15
A2	0.80	1.05
b	0.19	0.30
c	0.09	0.20
D	6.40	6.60
E	6.40 Basic	
E1	4.30	4.50
e	0.65 Basic	
L	0.45	0.75
α	0°	8°
aaa		0.10

Reference Document: JEDEC Publication 95, MO-153

Ordering Information

Table 9. Ordering Information

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
874S336AG	TBD	20 Lead TSSOP	Tube	0°C to 70°C
874S336AGT	TBD	20 Lead TSSOP	2500 Tape & Reel	0°C to 70°C
874S336AGLF	ICS874S336AL	“Lead-Free” 20 Lead TSSOP	Tube	0°C to 70°C
874S336AGLFT	ICS874S336AL	“Lead-Free” 20 Lead TSSOP	2500 Tape & Reel	0°C to 70°C

NOTE: Parts that are ordered with an "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

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