MPQ7235

36V, 3A, Synchronous Buck Automotive IR LED Driver, AEC-Q100 Qualified

DESCRIPTION

The MPQ7235 is a high-frequency, synchronous, rectified, step-down, switch-mode LED driver with integrated power MOSFETs. It offers a very compact solution to achieve 1.5A of continuous output current (I_{LED}) and 3A of peak LED current (I_{PEAK}), with excellent load and line regulation across a wide input supply range. The MPQ7235 also offers synchronous mode operation to achieve high efficiency.

The MPQ7235 supports low pulse-width modulation (PWM) dimming frequencies at small dimming duty cycles. The device can support PWM dimming frequencies as low as 10Hz to adjust infrared radiation (IR) LED driver applications. It is compatible with 30fps, 60fps, and 120fps dimming.

Current-mode operation provides fast transient response and eases loop stabilization.

Full protection features include over-current protection (OCP) and thermal shutdown.

The MPQ7235 requires a minimal number of readily available, standard external components. It is available in a space-saving QFN-13 (2.5mmx3mm) package, and is AEC-Q100 qualified.

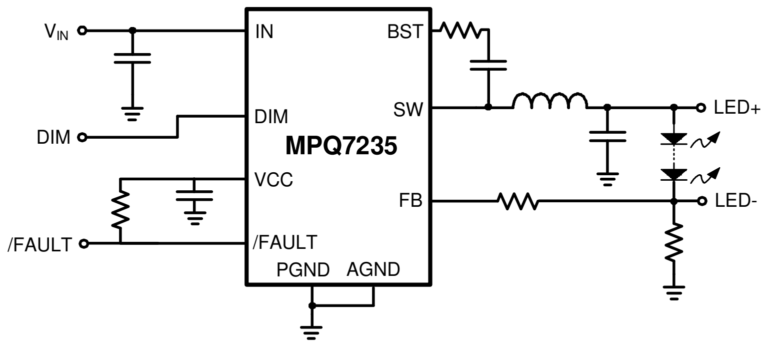
FEATURES

- **Built for a Wide Range of IR LED Applications:**
  - Wide 4V to 36V Operating Input Voltage (V_{IN}) Range
  - Up to 1.5A of Continuous LED Current (I_{LED})
  - Up to 3A of Peak LED Current (I_{PEAK}) with Low Dimming Frequencies at Small Duty Cycles
  - PWM Dimming Frequency: 10Hz to 2kHz
  - Compatible with 30fps, 60fps, and 120fps Dimming
- **High Performance for Improved Thermals:**
  - 85mΩ/50mΩ Low $R_{DS(ON)}$ Internal Power MOSFETs
  - 0.2V Reference Voltage (V_{REF})
  - High-Efficiency Synchronous Mode Operation
- **Optimized for EMC and EMI:**
  - Default 2.2MHz Switching Frequency (f_{SW})
  - EMI Reduction Techniques
- **Full Protection Features:**
  - LED Short and Open Fault Indication
  - OCP with Valley Current Detection
  - Thermal Shutdown
- **Additional Features:**
  - FCCM
  - Internal Soft Start (SS)
  - Available in a QFN-13 (2.5mmx3mm) Package
  - Available in a Wettable Flank Package
  - CISPR25 Class 5 Compliant
  - Available in AEC-Q100 Grade 1

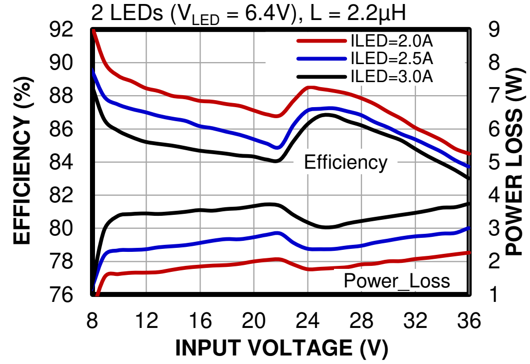
APPLICATIONS

- Infrared (IR) LED Drivers for Driver Monitoring Systems (DMS)
- IR Illumination for Automotive Cameras
- Surveillance Systems

TYPICAL APPLICATION



Efficiency vs. Input Voltage vs. Power Loss
2 LEDs (V_{LED} = 6.4V), L = 2.2µH



ORDERING INFORMATION

Part Number*	Package	Top Marking	MSL Rating**
MPQ7235GQBE-AEC1***	QFN-13 (2.5mmx3mm)	*See Below*	1

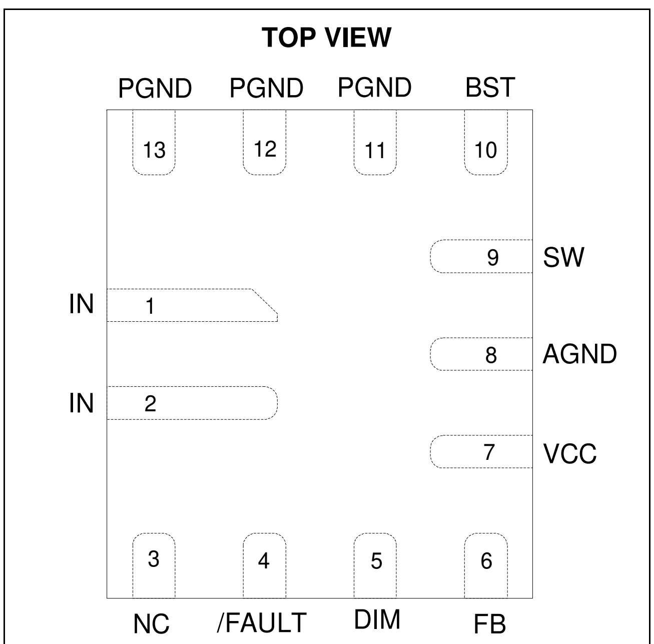
* For Tape & Reel, add suffix -Z (e.g. MPQ7235GQBE-AEC1-Z).
** Moisture Sensitivity Level Rating
*** Wettable Flank

TOP MARKING

BRE
YWW
LLL

BRE: Product code
Y: Year code
WW: Week code
LLL: Lot number

PACKAGE REFERENCE



QFN-13 (2.5mmx3mm)

PIN FUNCTIONS

Pin #	Name	Description
1, 2	IN	**Supply voltage.** The MPQ7235 operates from a 4V to 36V input rail. An input capacitor (C_{IN}) is required to decouple the input rail. Connect VIN to the input rail using a wide PCB trace.
3	NC	**Not connected.**
4	/FAULT	**Fault indicator.** /FAULT is an open-drain output. Pull /FAULT to VCC or an external source with a resistor to indicate a fault condition. Pull this pin low if any of the following occurs: an LED short, open fault, or thermal shutdown.
5	DIM	**Dimming control.** Apply a 10Hz to 2kHz external clock to the DIM pin for pulse-width modulation (PWM) dimming. Pull DIM low with an internal resistor; dimming is off if the pin is floating.
6	FB	**LED current feedback input.**
7	VCC	**Internal bias supply.** Decouple VCC with a 0.1µF to 0.22µF capacitor. The capacitance should not exceed 0.22µF.
8	AGND	**Analog ground.** AGND is the logic circuit's reference ground. Connect AGND to PGND internally. An external connection on board between AGND and PGND is not required, but is recommended for better ground connection.
9	SW	**Switch output.** Connect SW using a wide PCB trace.
10	BST	**Bootstrap.** Connect a capacitor between the SW and BST pins to form a floating supply across the high-side MOSFET (HS-FET) driver. A 20Ω resistor placed between SW and the BST capacitor (C_{BST}) is strongly recommended to reduce the SW spike voltage.
11, 12, 13	PGND	**Power ground.** PGND is the power device's reference ground, and requires careful consideration during PCB layout. For the best results, connect PGND with copper pours and vias.

ABSOLUTE MAXIMUM RATINGS (1)

Supply voltage (V_{IN}) ....-0.3V to +40V
Switch voltage (V_{SW}) ....-0.3V to V_{IN} + 0.3V
BST voltage (V_{BST}) .... V_{SW} + 6V
All other pins ....-0.3V to +6V (2)
Continuous power dissipation (T_A = 25°C) (3) (8)
QFN-13 (2.5mmx3mm)............................ 2.98W
Junction temperature ....150°C
Lead temperature ....260°C
Storage temperature................ -65°C to +150°C

ESD Ratings

Human body model (HBM) ....Class 2 (4)
Charged device model (CDM) .... Class C2b (5)

Recommended Operating Conditions

Supply voltage (V_{IN}) ....4V to 36V
Continuous LED current (I_{LED})............Up to 1.5A
LED peak current (I_{PEAK}) ....Up to 3A
Operating junction temp (T_J) ....
....-40°C to +125°C (6)

Thermal Resistance

Thermal Resistance	θ_{JA}	θ_{JC}	
QFN-13 (2.5mmx3mm)			
JESD51-7 (7)	60	13	°C/W
EVQ7235-QB-00A (8)	42	2.5	°C/W

Notes:

1) Absolute maximum ratings are rated under room temperature unless otherwise noted. Exceeding these ratings may damage the device.
2) See the PWM Dimming section on page 22 for details about the DIM pin's absolute maximum rating.
3) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation can generate an excessive die temperature, which causes the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
4) Per AEC-Q100-002.
5) Per AEC-Q100-011.
6) Operating devices at junction temperature up to 150°C is possible. Contact MPS for details.
7) Measured on JESD51-7, 4-layer PCB. The value of θ_{JA} given in this table is only valid for comparison with other packages and cannot be used for design purposes. These values were calculated in accordance with JESD51-7 and simulated on a specified JEDEC board. They do not represent the performance obtain in an actual application.
8) Measured on MPS's standard EVB for the MPQ7235: a 4-layer, 2-oz PCB (83mmx83mm).

ELECTRICAL CHARACTERISTICS

V_{IN} = 12V, V_{DIM} = 2V, T_J = -40°C to +125°C, typical values are at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Quiescent supply current	I_Q	V_{DIM} = 2V, V_{FB} = 1V, no switching		0.6	0.8	mA
High-side MOSFET (HS-FET) on resistance	$HS_{RDS\text{-}ON}$	$V_{BST\text{-}SW}$ = 5V		85	150	mΩ
Low-side MOSFET (LS-FET) on resistance	$LS_{RDS\text{-}ON}$	V_{CC} = 5V		50	105	mΩ
Switch leakage	SW_{LKG}	V_{DIM} = 0V, V_{SW} = 12V			1	µA
Current limit (9)	I_{LIMIT}	Below 40% duty cycle	4.5	6	8	A
Reverse current limit	$I_{LIMIT\_REVERSE}$			1.2		A
Switching frequency	f_{SW}	V_{FB} = 100mV	1800	2200	2600	kHz
Maximum duty cycle	D_{MAX}	V_{FB} = 100mV	80	87		%
Minimum on time (9)	t_{ON_MIN}			46		ns
Feedback (FB) voltage	V_{FB}	T_J = 25°C	192	200	208	mV
		T_J = -40°C to +125°C	184	200	216	
FB current	I_{FB}	V_{FB} = 250mV		30	100	nA
DIM rising threshold	V_{DIM_RISING}		0.65	0.98	1.35	V
DIM falling threshold	$V_{DIM\_FALLING}$		0.5	0.8	1.1	V
DIM threshold hysteresis	V_{DIM_HYS}			175		mV
DIM input current	I_{DIM}	V_{DIM} = 2V		4	6	µA
		V_{DIM} = 0		0.9	1.5	µA
DIM to first SW delay after soft start	$t_{DIM\text{-}SW}$	I_{VCC} = 10mA		1.3		µs
V_{IN} under-voltage lockout (UVLO) rising threshold	$INUV_{VTH\_R}$		3.2	3.5	3.8	V
V_{IN} UVLO falling threshold	$INUV_{VTH\_F}$		2.8	3.1	3.5	V
V_{IN} UVLO hysteresis threshold	$INUV_{HYS}$			400		mV
Over-voltage (OV) detection (/FAULT pulled low)	$FT_{VTH\text{-}HI}$			140%		V_{FB}
OV detection hysteresis				20%		V_{FB}
/FAULT delay	$t_{FT\text{-}TD}$			10		µs
/FAULT sink current capability	V_{FT}	Sink 4mA			0.4	V
/FAULT leakage current	$I_{FT\text{-}LEAK}$				100	nA
VCC regulator	V_{CC}	I_{CC} = 0mA	4.6	4.9	5.2	V
VCC load regulation		I_{CC} = 10mA		1.5	8	%
VCC source current ability		V_{CC} = V_{CC_UVLO} + 100mV, switching		10		mA
Soft-start time (9)	t_{SS}	I_{LED} = 3A, L = 2.2µH, V_{LED} = 6.4V, I_{LED} from 10% to 90%		2		ms

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{DIM} = 2V, T_J = -40°C to +125°C, typical values are at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Thermal shutdown (9)	T_{SD}	Rising temperature	150	170		°C
Thermal hysteresis (9)	T_{SD_HYS}			30		°C

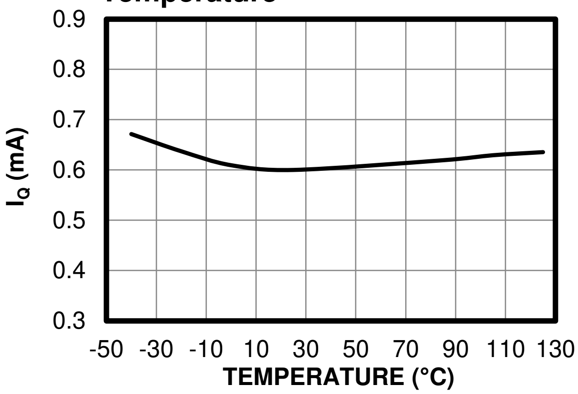
Note:

9) Guaranteed by bench characterization. Not tested in production.

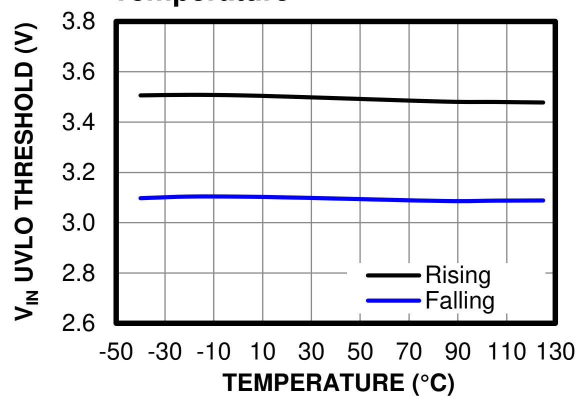
TYPICAL CHARACTERISTICS

V_{IN} = 12V, T_J = -40°C to +125°C, unless otherwise noted.

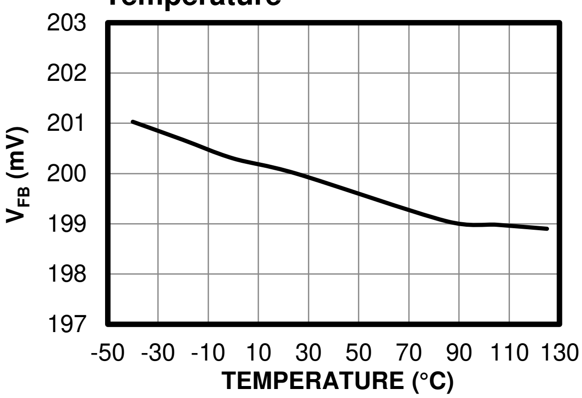
Quiescent Current vs. Temperature



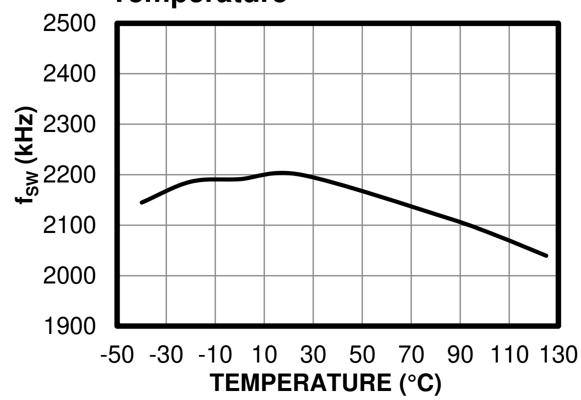
V_{IN} UVLO Threshold vs. Temperature



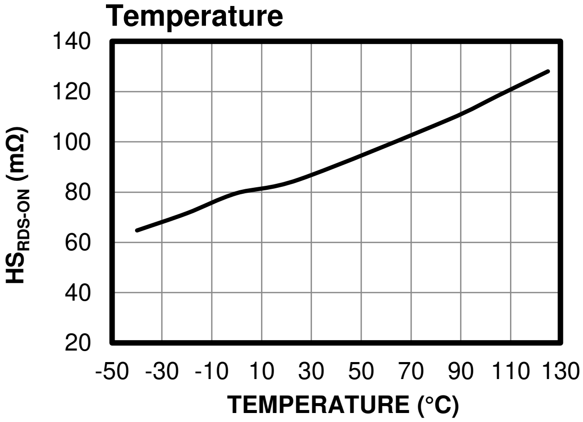
Feedback Voltage vs. Temperature



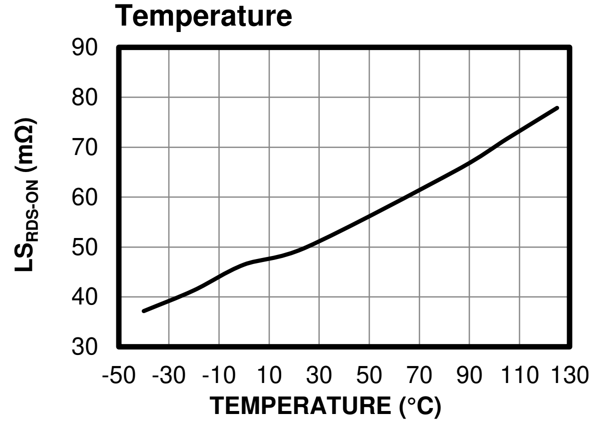
Switching Frequency vs. Temperature



HS-FET On Resistance vs. Temperature

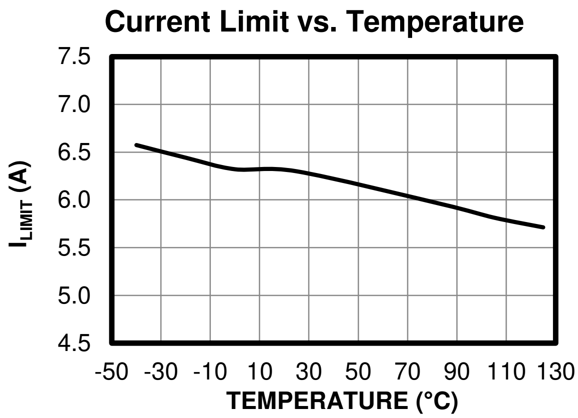


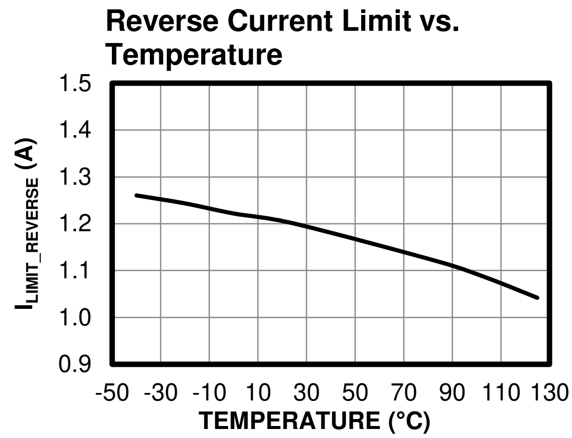
LS-FET On Resistance vs. Temperature



TYPICAL CHARACTERISTICS *(continued)*

V_{IN} = 12V, T_J = -40°C to +125°C, unless otherwise noted.



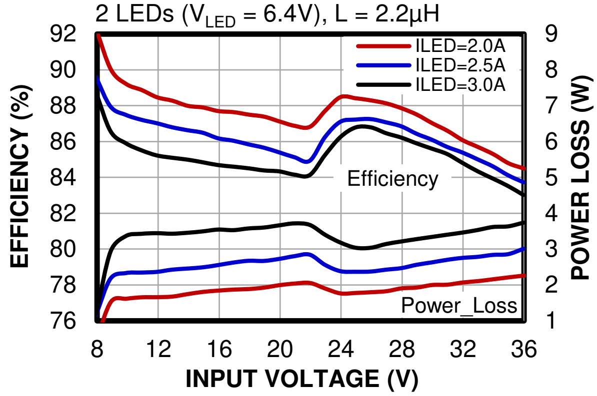


TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 12V, V_{LED+} - V_{LED-} = 2 x 3.2V at I_{LED} = 1.5A, L = 2.2µH, f_{SW} = 2.2MHz, T_A = 25°C, unless otherwise noted. (10)

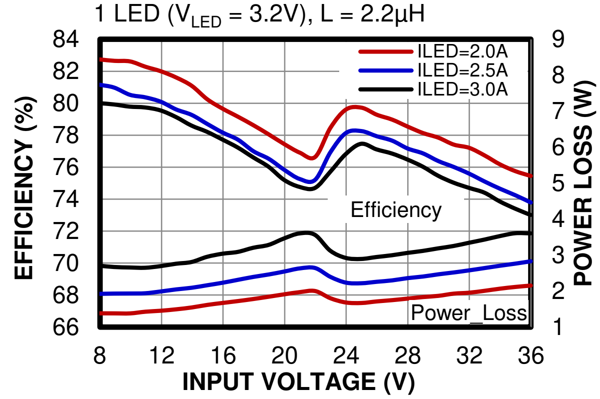
Efficiency vs. Input Voltage vs. Power Loss

2 LEDs (V_{LED} = 6.4V), L = 2.2µH



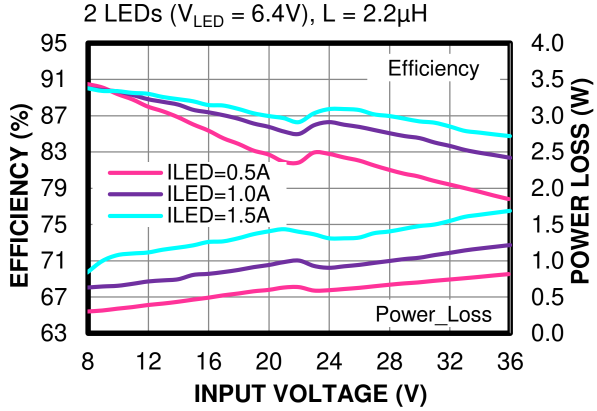
Efficiency vs. Input Voltage vs. Power Loss

1 LED (V_{LED} = 3.2V), L = 2.2µH



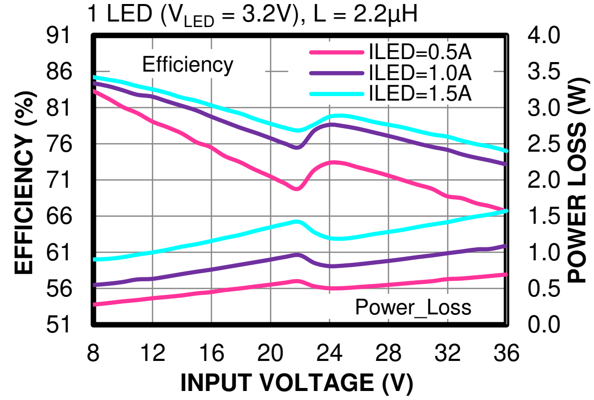
Efficiency vs. Input Voltage vs. Power Loss

2 LEDs (V_{LED} = 6.4V), L = 2.2µH



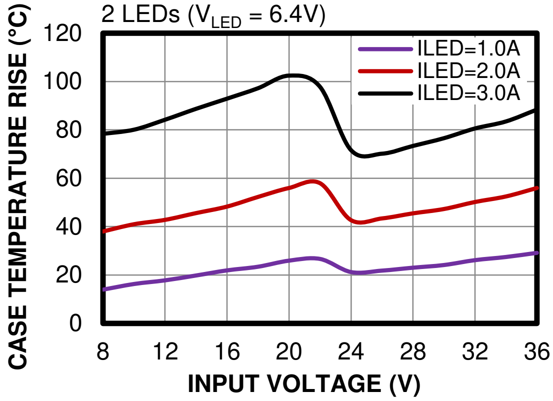
Efficiency vs. Input Voltage vs. Power Loss

1 LED (V_{LED} = 3.2V), L = 2.2µH



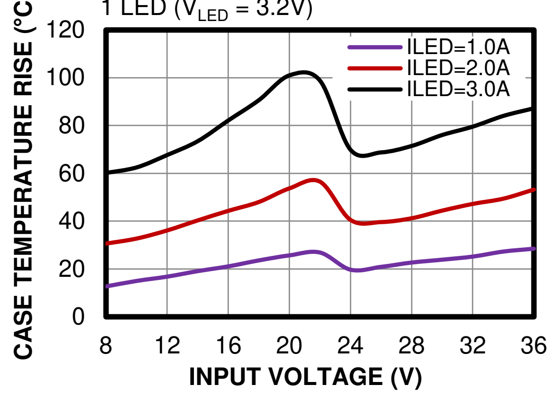
Case Temperature Rise vs. Input Voltage

2 LEDs (V_{LED} = 6.4V)



Case Temperature Rise vs. Input Voltage

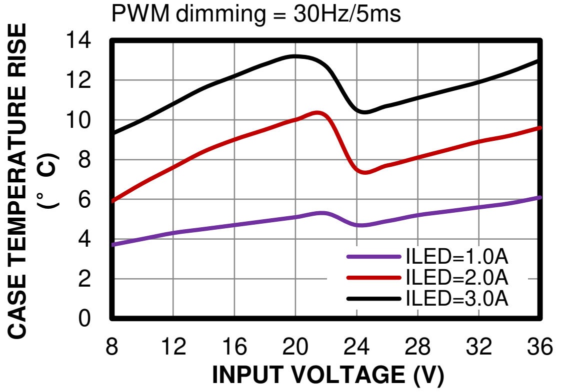
1 LED (V_{LED} = 3.2V)



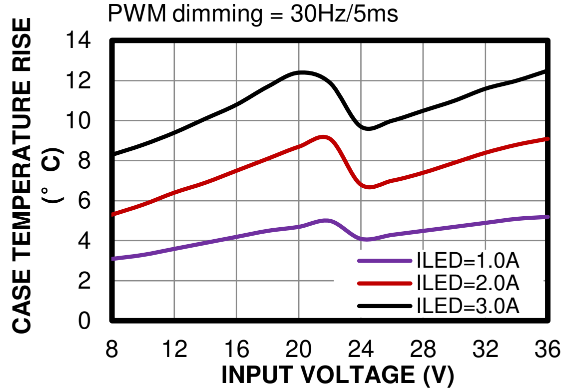
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{LED+} - V_{LED-} = 2 x 3.2V at I_{LED} = 1.5A, L = 2.2µH, f_{SW} = 2.2MHz, T_A = 25°C, unless otherwise noted. (10)

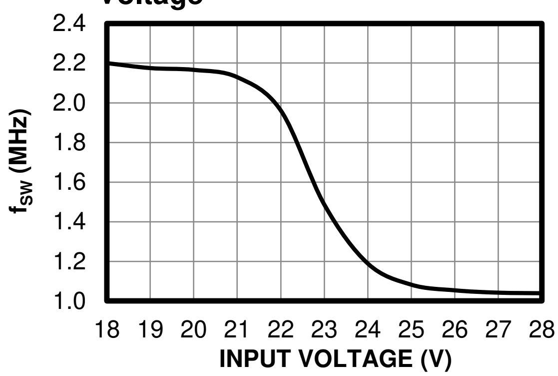
Case Temp Rise vs. V_{IN}
2 LEDs (V_{LED} = 6.4V),
PWM dimming = 30Hz/5ms



Case Temp Rise vs. V_{IN}
1 LED (V_{LED} = 3.2V),
PWM dimming = 30Hz/5ms



Switching Frequency vs. Input Voltage



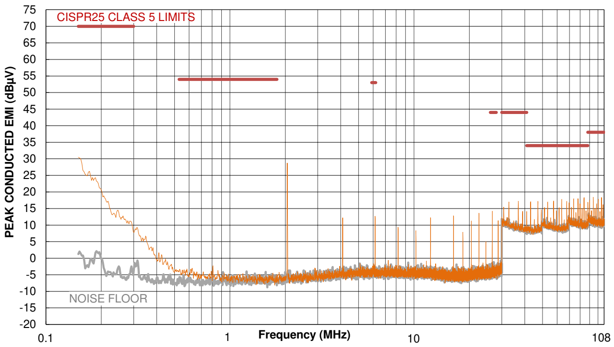
Note:

10) The efficiency and thermal curves are based on Figure 8 on page 28 when R_{BST} = 0Ω, and the output and input filters have been removed. L = 2.2µH (VCHA042A-2R2MS6).

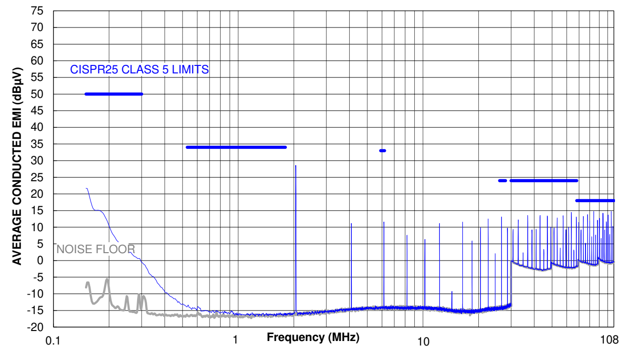
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{LED+} - V_{LED-} = 2 x 3.2V at I_{LED} = 3A, L = 2.2µH, f_{SW} = 2.2MHz, with EMI filters, T_A = 25°C, unless otherwise noted. [11]

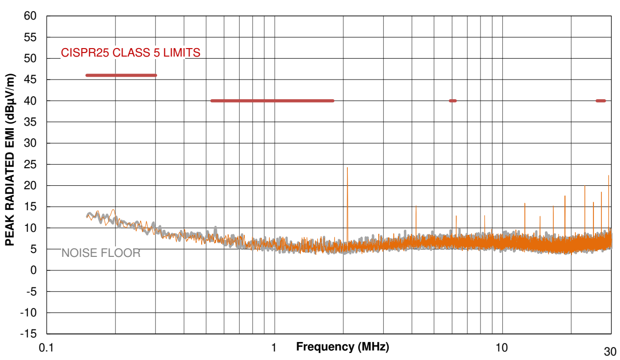
CISPR25 Class 5 Peak Conducted Emissions
150kHz to 108MHz



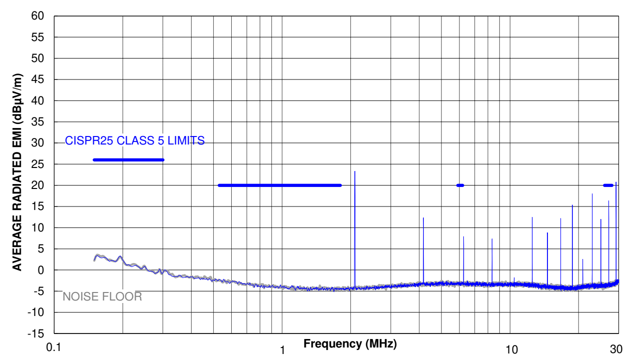
CISPR25 Class 5 Average Conducted Emissions
150kHz to 108MHz



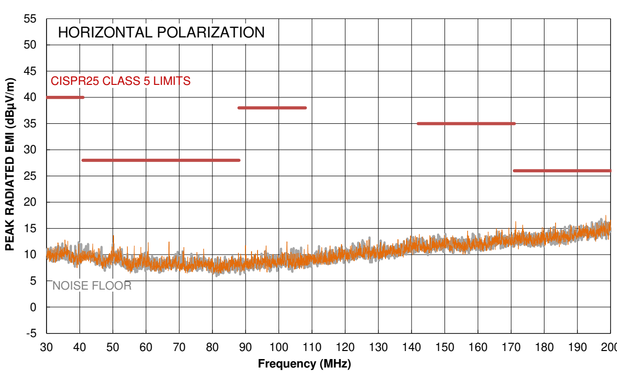
CISPR25 Class 5 Peak Radiated Emissions
150kHz to 30MHz



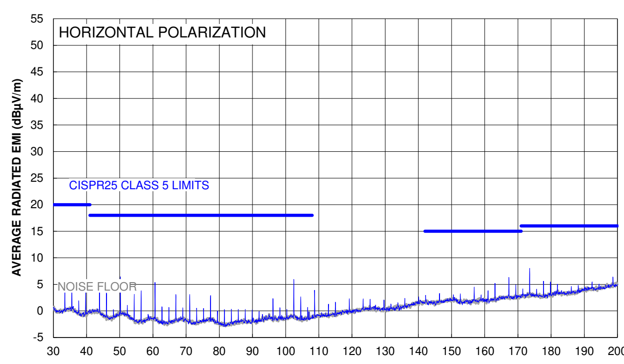
CISPR25 Class 5 Average Radiated Emissions
150kHz to 30MHz



CISPR25 Class 5 Peak Radiated Emissions
Horizontal, 30MHz to 200MHz



CISPR25 Class 5 Average Radiated Emissions
Horizontal, 30MHz to 200MHz

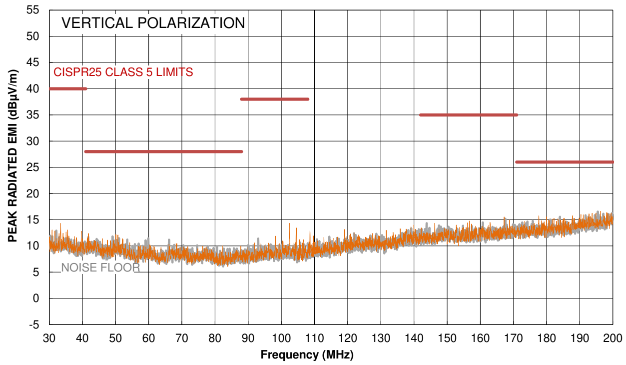


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{LED+} - V_{LED-} = 2 x 3.2V at I_{LED} = 3A, L = 2.2µH, f_{SW} = 2.2MHz, with EMI filters, T_A = 25°C, unless otherwise noted. [11]

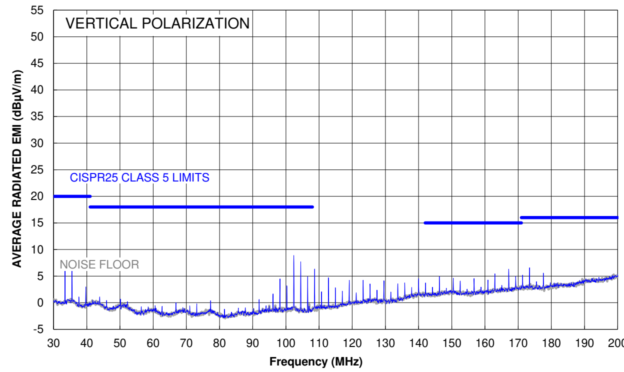
CISPR25 Class 5 Peak Radiated Emissions

Vertical, 30MHz to 200MHz



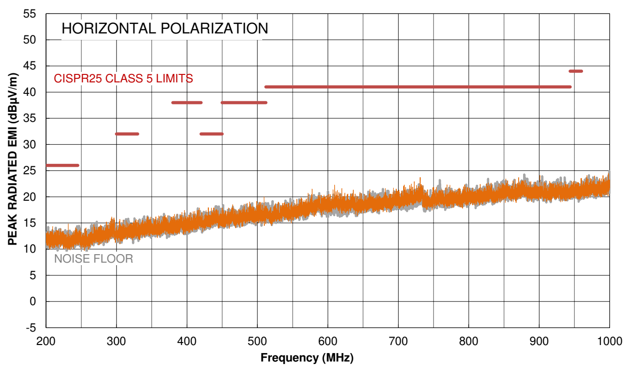
CISPR25 Class 5 Average Radiated Emissions

Vertical, 30MHz to 200MHz



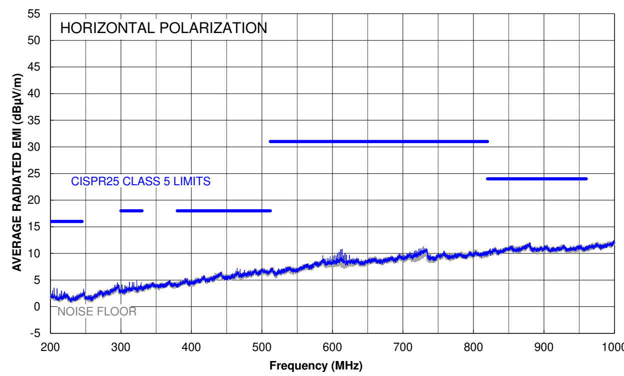
CISPR25 Class 5 Peak Radiated Emissions

Horizontal, 200MHz to 1GHz



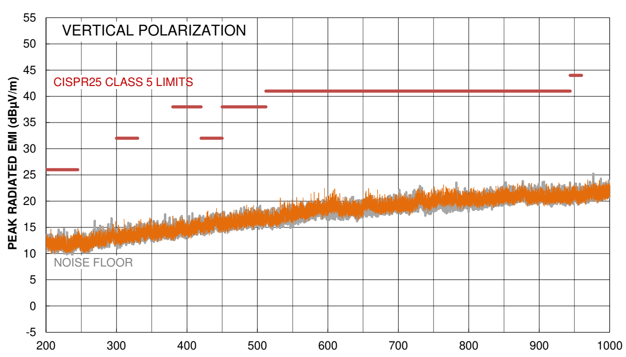
CISPR25 Class 5 Average Radiated Emissions

Horizontal, 200MHz to 1GHz



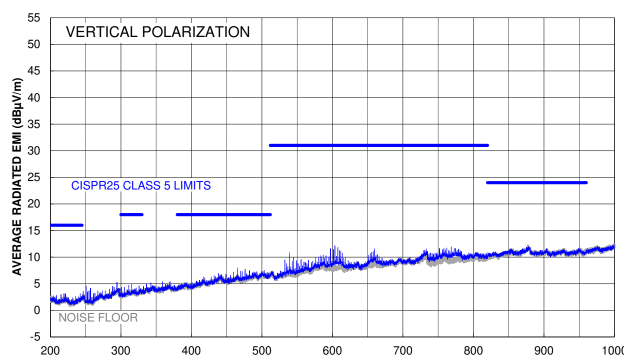
CISPR25 Class 5 Peak Radiated Emissions

Vertical, 200MHz to 1GHz



CISPR25 Class 5 Average Radiated Emissions

Vertical, 200MHz to 1GHz



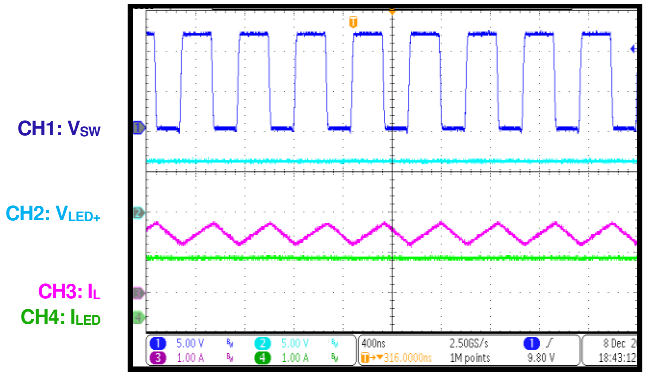
Note:

11) The MPQ7235 EMI test results are based on the typical application circuit with EMI filters (see Figure 9 on page 28).

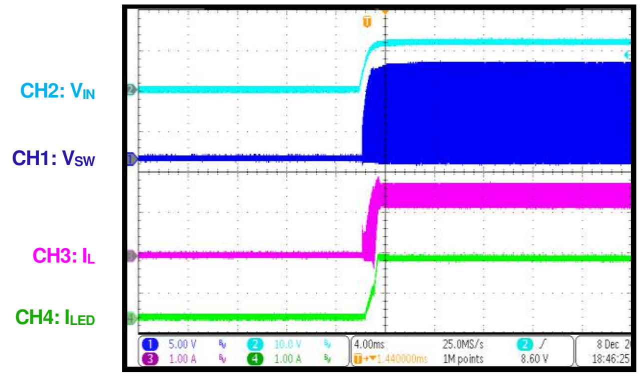
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{LED+} - V_{LED-} = 2 x 3.2V at I_{LED} = 1.5A, L = 2.2µH, f_{SW} = 2.2MHz, T_A = 25°C, unless otherwise noted.

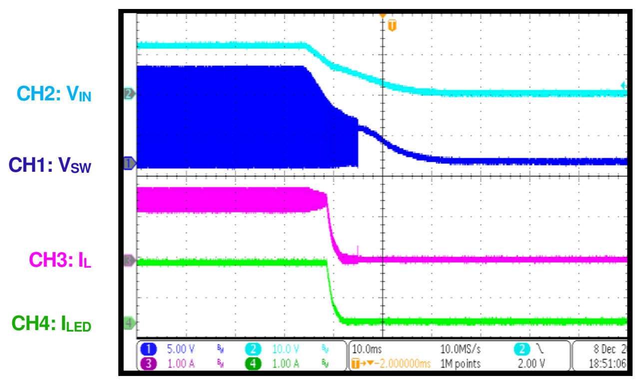
Steady State
I_{LED} = 1.5A



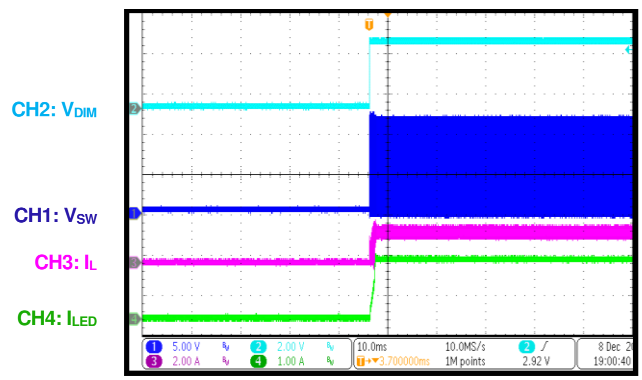
Start-Up through VIN
I_{LED} = 1.5A



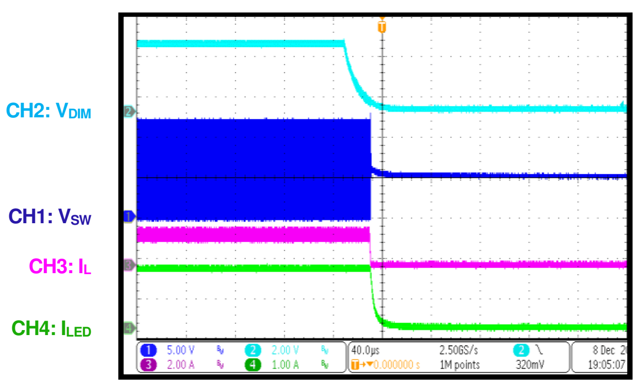
Shutdown through VIN
I_{LED} = 1.5A



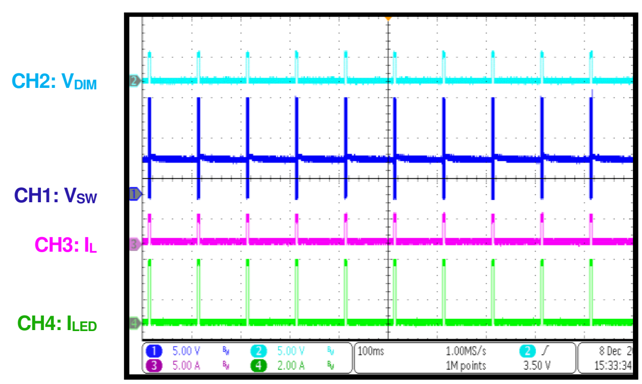
Start-Up through DIM
I_{LED} = 1.5A



Shutdown through DIM
I_{LED} = 1.5A



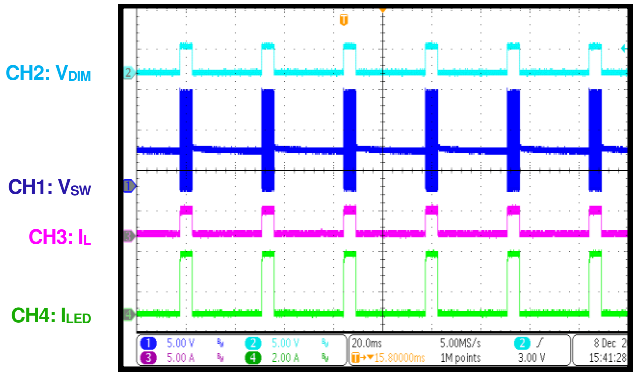
PWM Dimming Steady State
Dimming frequency = 10Hz/5ms, I_{PEAK} = 3A



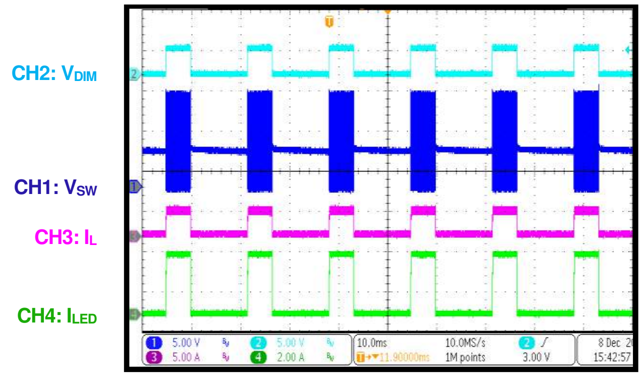
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{LED+} - V_{LED-} = 2 x 3.2V at I_{LED} = 1.5A, L = 2.2µH, f_{SW} = 2.2MHz, T_A = 25°C, unless otherwise noted.

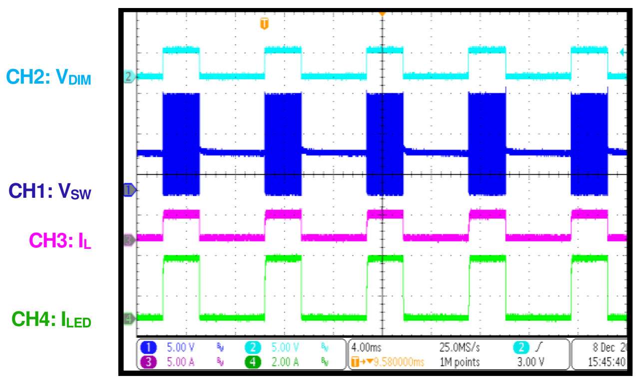
PWM Dimming Steady State
Dimming frequency = 30Hz/5ms, I_{PEAK} = 3A



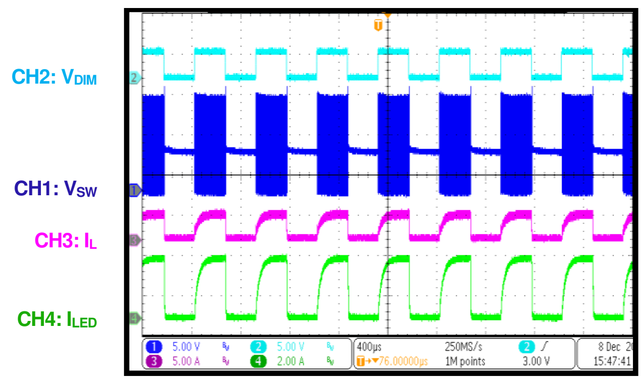
PWM Dimming Steady State
Dimming frequency = 60Hz/5ms, I_{PEAK} = 3A



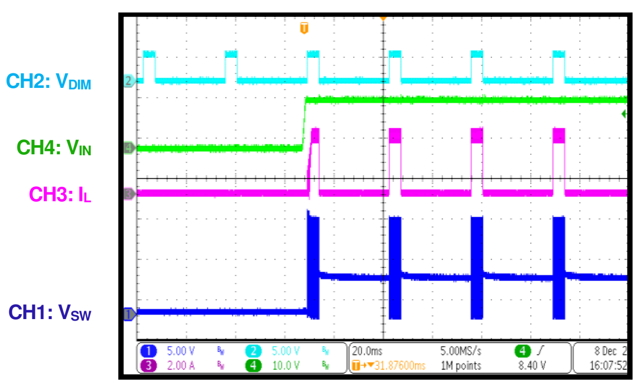
PWM Dimming Steady State
Dimming frequency = 120Hz/3ms, I_{PEAK} = 3A



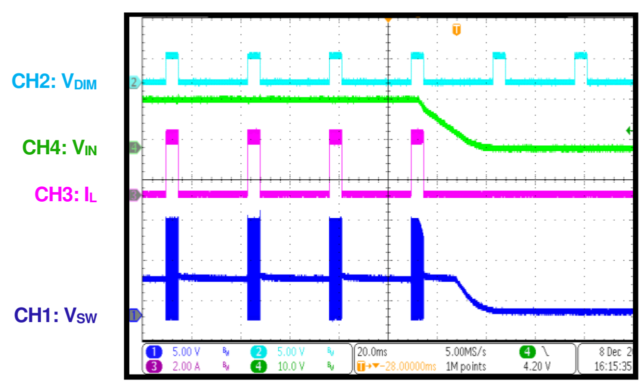
PWM Dimming Steady State
Dimming frequency = 2kHz/50%, I_{PEAK} = 3A



PWM Dimming
Start-up through VIN, I_{PEAK} = 3A



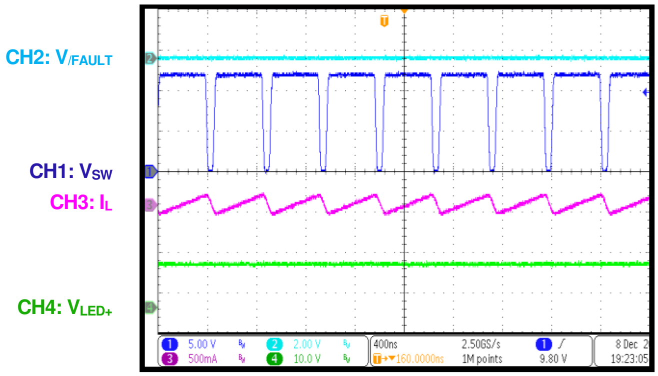
PWM Dimming
Shutdown through VIN, I_{PEAK} = 3A



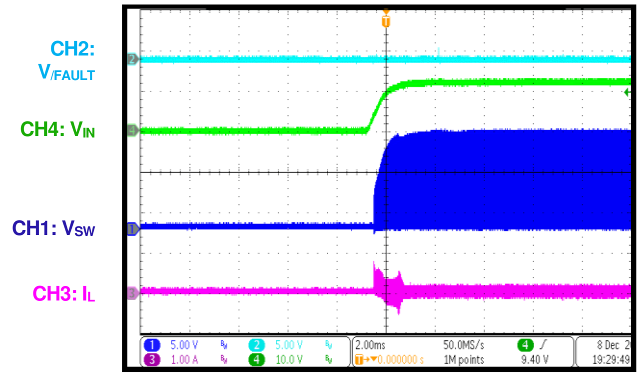
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{LED+} - V_{LED-} = 2 x 3.2V at I_{LED} = 1.5A, L = 2.2µH, f_{SW} = 2.2MHz, T_A = 25°C, unless otherwise noted.

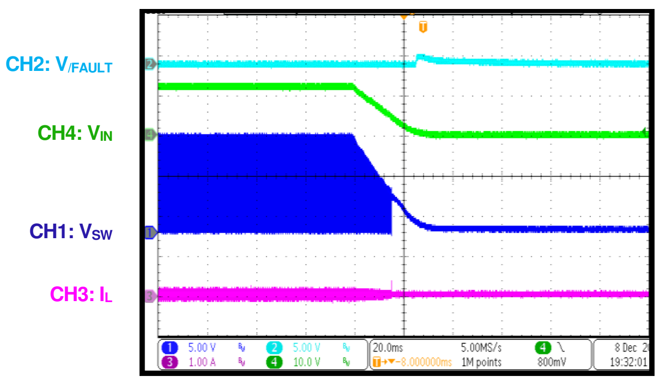
LED Open Steady State



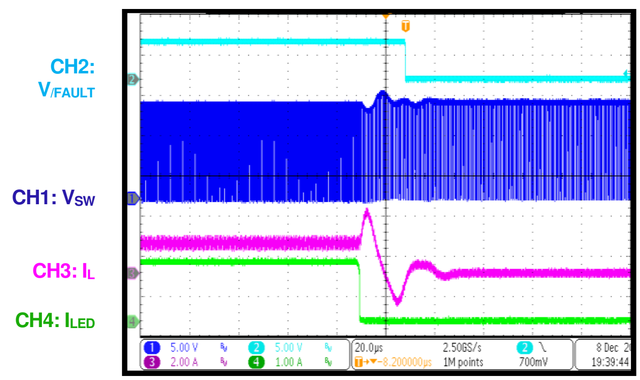
LED Open Input Start-Up



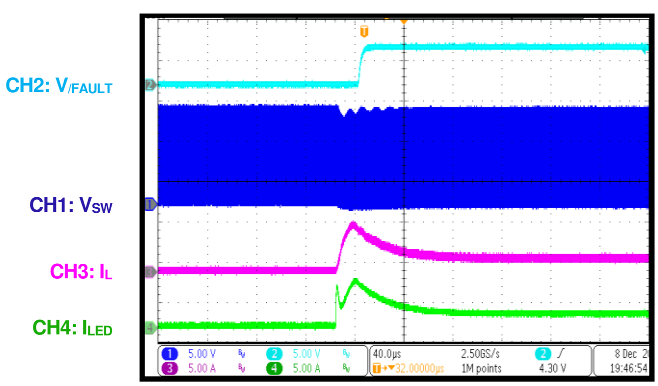
LED Open Input Shutdown



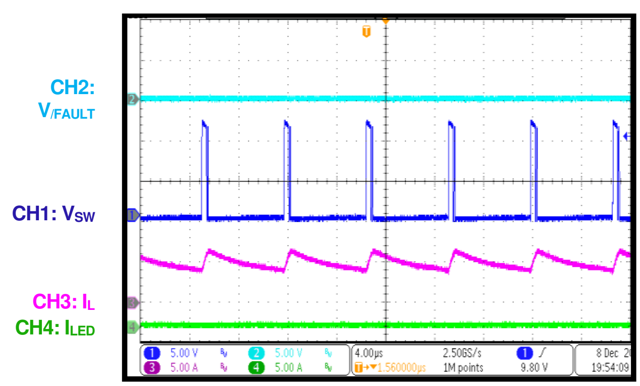
LED Open Entry



LED Open Recovery



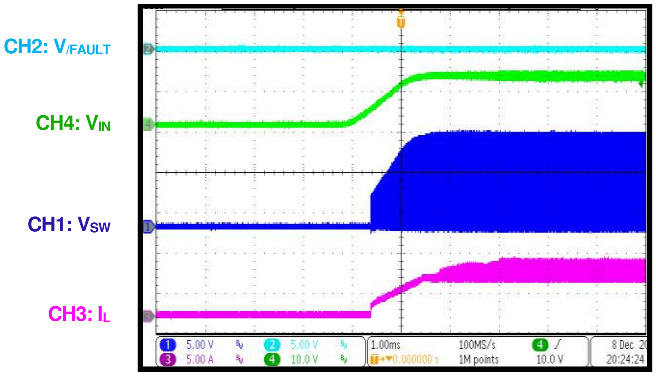
LED+ Short to GND Steady State



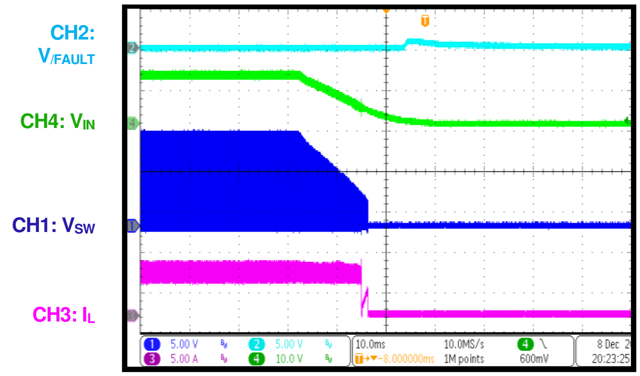
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{LED+} - V_{LED-} = 2 x 3.2V at I_{LED} = 1.5A, L = 2.2μH, f_{SW} = 2.2MHz, T_A = 25°C, unless otherwise noted.

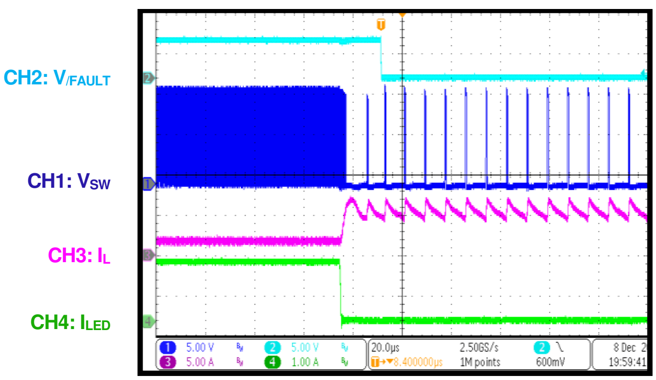
LED+ Short to GND Input Start-Up



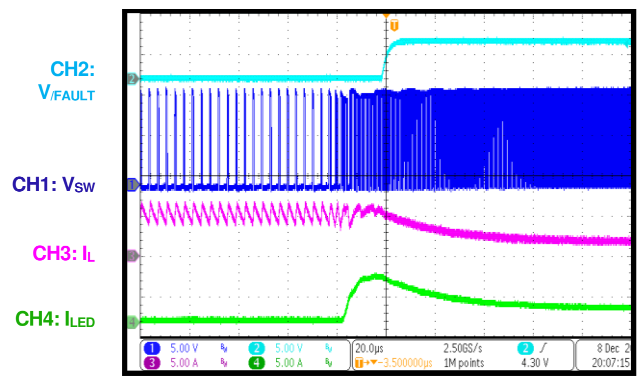
LED+ Short to GND Input Shutdown



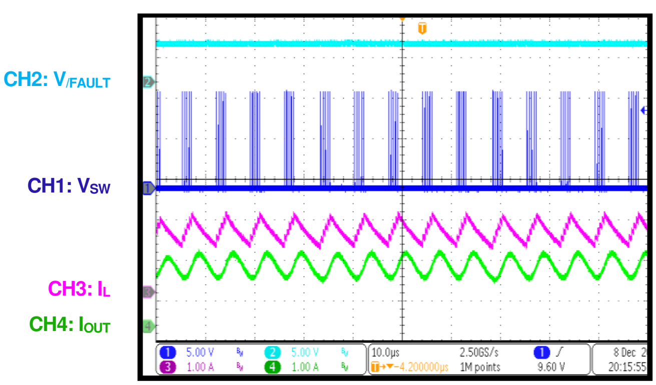
LED+ Short to GND Entry



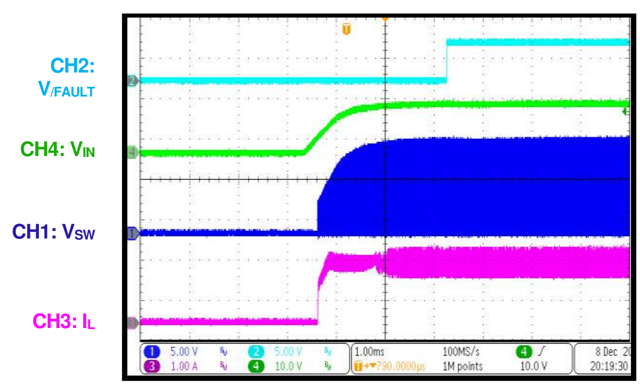
LED+ Short to GND Recovery



LED+ Short to LED- Steady State



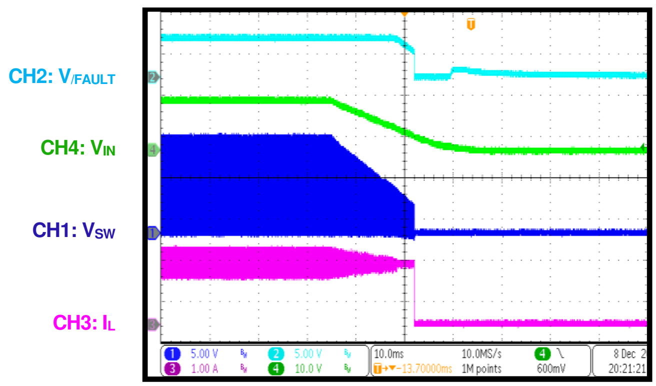
LED+ Short to LED- Input Start-Up



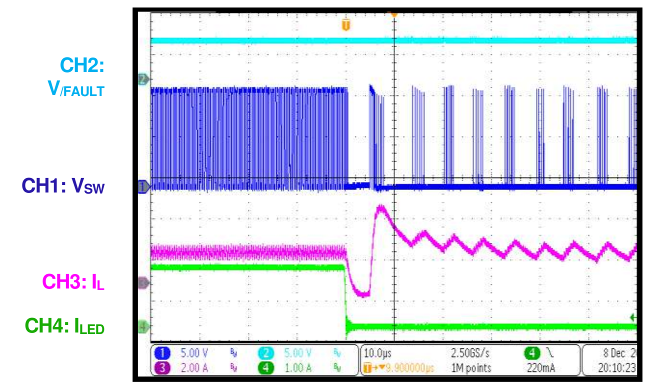
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{LED+} - V_{LED-} = 2 x 3.2V at I_{LED} = 1.5A, L = 2.2μH, f_{SW} = 2.2MHz, T_A = 25°C, unless otherwise noted.

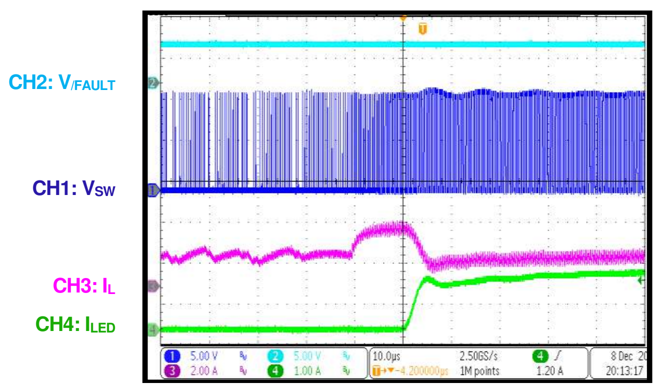
LED+ Short to LED- Input Shutdown



LED+ Short to LED- Entry

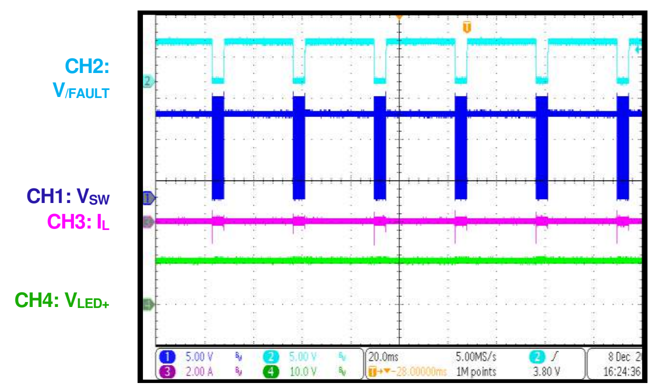


LED+ Short to LED- Recovery



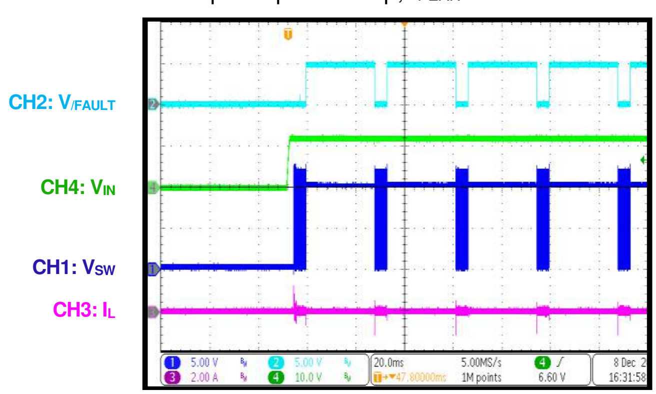
PWM Dimming

LED open steady state, I_{PEAK} = 3A



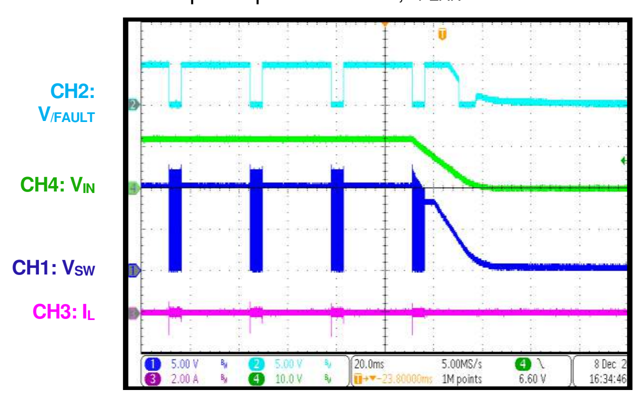
PWM Dimming

LED open input start-up, I_{PEAK} = 3A



PWM Dimming

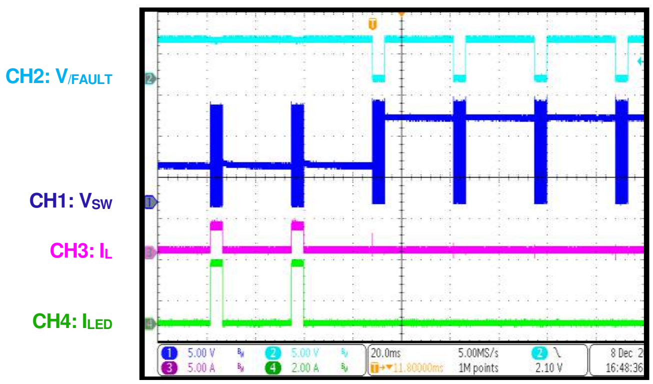
LED open input shutdown, I_{PEAK} = 3A



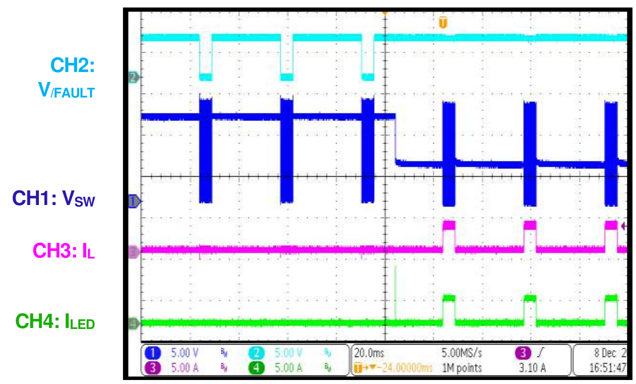
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{LED+} - V_{LED-} = 2 x 3.2V at I_{LED} = 1.5A, L = 2.2µH, f_{SW} = 2.2MHz, T_A = 25°C, unless otherwise noted.

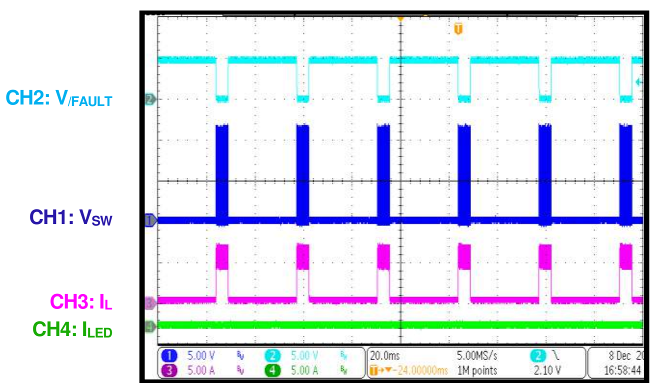
PWM Dimming
LED open entry, I_{PEAK} = 3A



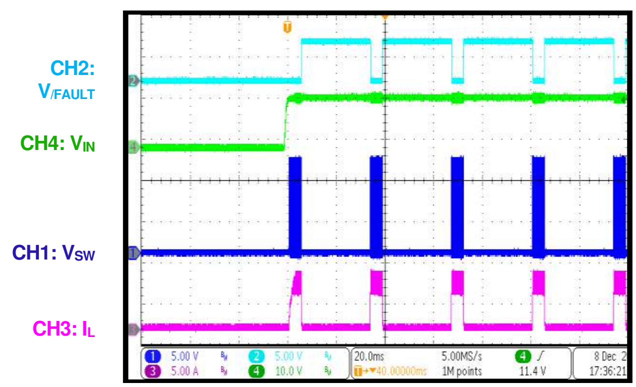
PWM Dimming
LED open recovery, I_{PEAK} = 3A



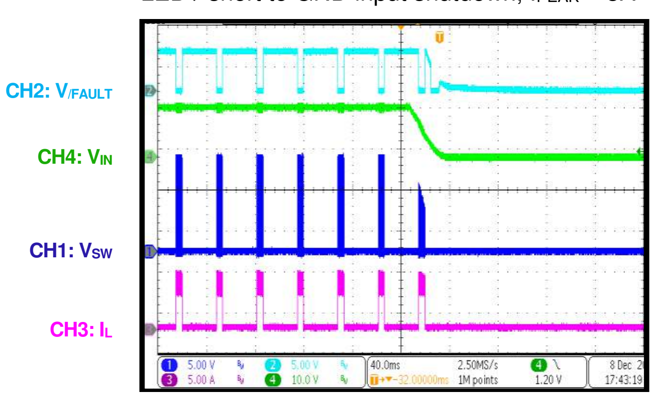
PWM Dimming
LED+ short to GND steady state, I_{PEAK} = 3A



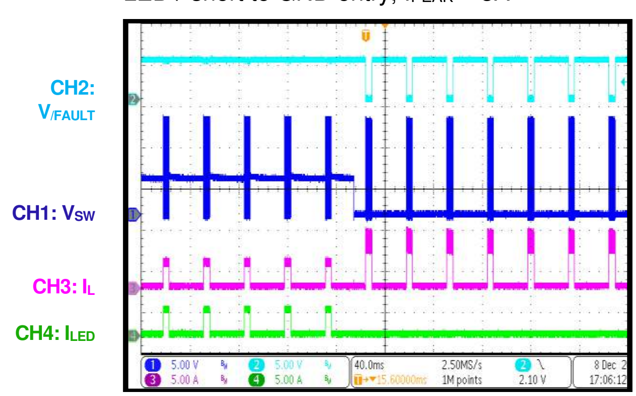
PWM Dimming
LED+ short to GND input start-up, I_{PEAK} = 3A



PWM Dimming
LED+ short to GND input shutdown, I_{PEAK} = 3A



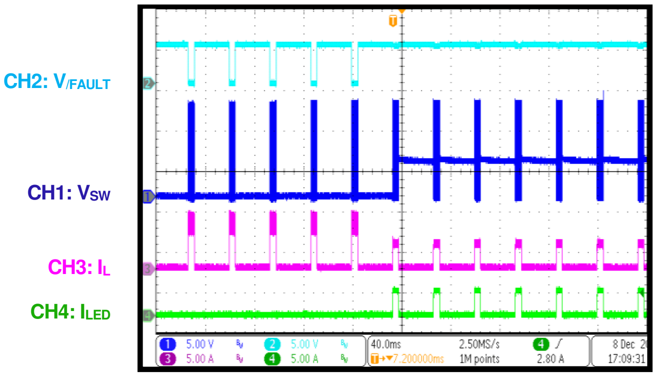
PWM Dimming
LED+ short to GND entry, I_{PEAK} = 3A



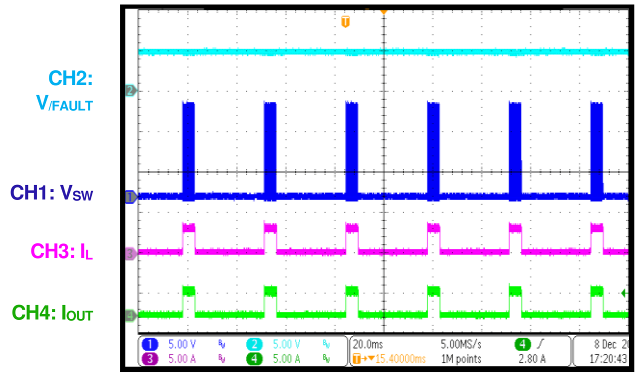
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{LED+} - V_{LED-} = 2 x 3.2V at I_{LED} = 1.5A, L = 2.2µH, f_{SW} = 2.2MHz, T_A = 25°C, unless otherwise noted.

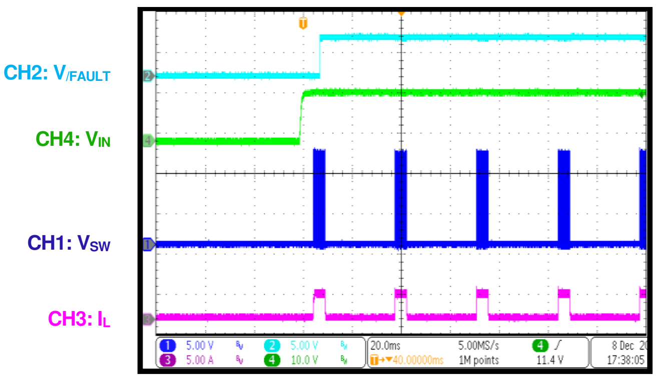
PWM Dimming
LED+ short to GND recovery, I_{PEAK} = 3A



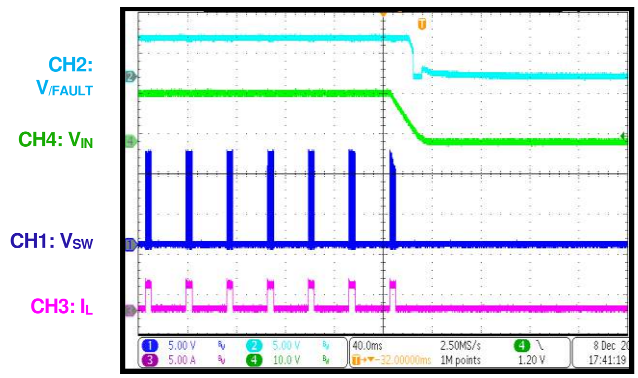
PWM Dimming
LED+ short to LED- steady state, I_{PEAK} = 3A



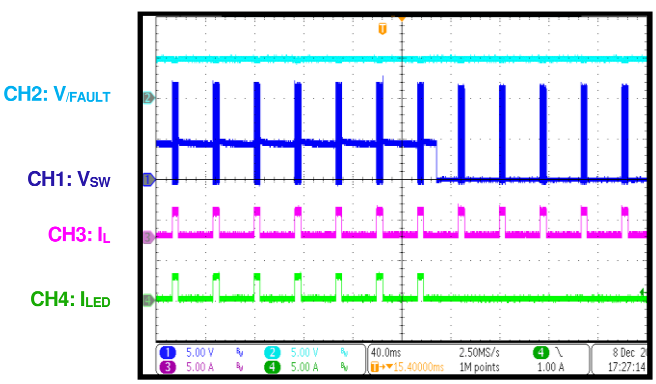
PWM Dimming
LED+ short to LED- input start-up, I_{PEAK} = 3A



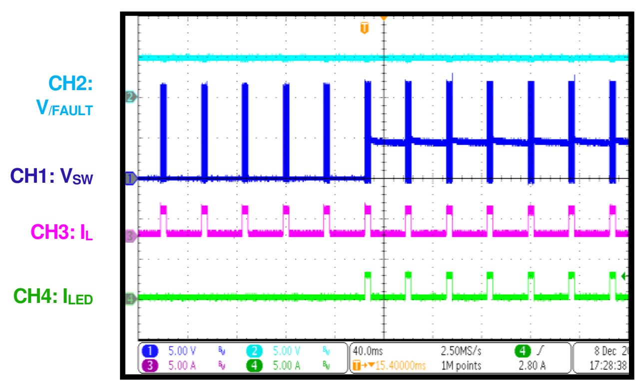
PWM Dimming
LED+ short to LED- input shutdown, I_{PEAK} = 3A



PWM Dimming
LED+ short to LED- entry, I_{PEAK} = 3A



PWM Dimming
LED+ short to LED- recovery, I_{PEAK} = 3A



FUNCTIONAL BLOCK DIAGRAM

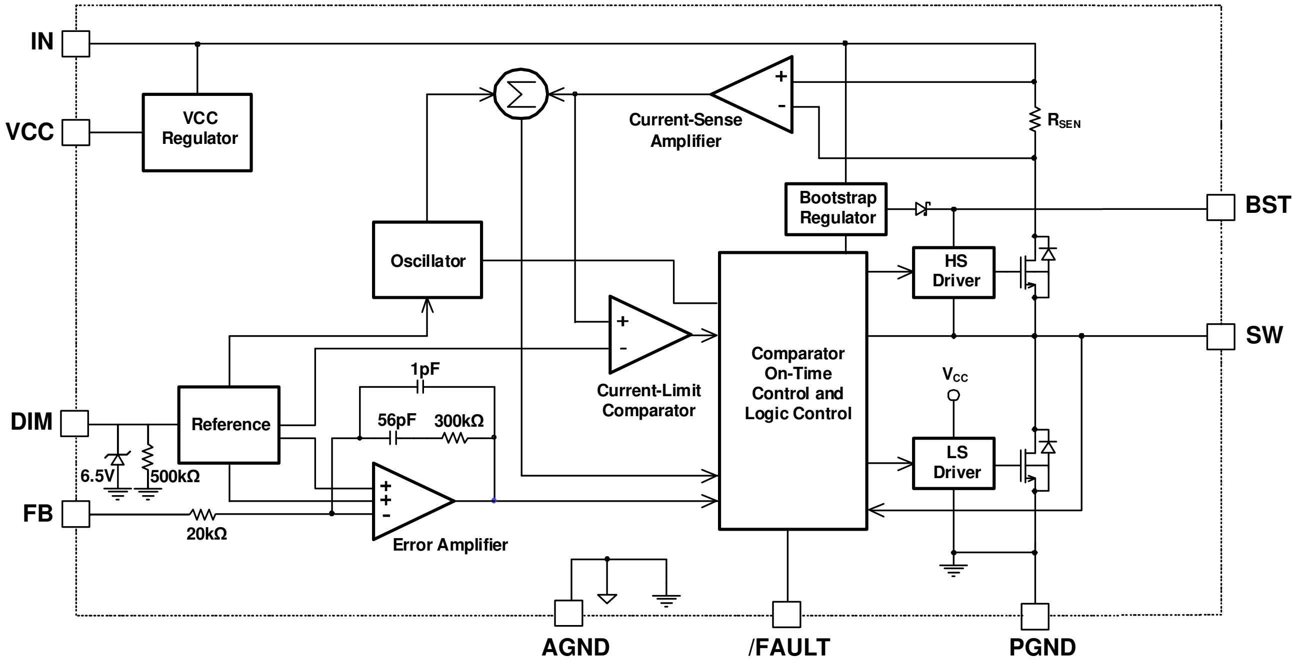


Figure 1: Functional Block Diagram

OPERATION

The MPQ7235 is a high-frequency, synchronous, rectified, step-down, switch-mode LED driver with integrated power MOSFETs. It offers a very compact solution to achieve 1.5A of continuous output current (I_{LED}) and 3A of peak LED current (I_{PEAK}), with excellent load and line regulation across a 4V to 36V input supply range. The MPQ7235 supports low pulse-width modulation (PWM) dimming frequencies at small dimming duty cycles.

The MPQ7235 operates in a fixed-frequency, peak current control mode to regulate I_{LED}. An internal clock initiates a PWM cycle. The integrated high-side MOSFET (HS-FET) turns on and remains on until its current reaches the value set by the COMP voltage (V_{COMP}). When the HS-FET is off, it remains off until the next clock cycle starts. If the HS-FET current does not reach the current value set by V_{COMP} within 87% of one PWM period, the HS-FET is forced off.

Internal Regulator

The 4.9V internal regulator (VCC) powers most of the internal circuitries. VCC uses the input voltage (V_{IN}) and operates in the full V_{IN} range. When V_{IN} exceeds 4.9V, the regulator output is fully regulated; when V_{IN} falls below 4.9V, the output decreases following V_{IN}. A 0.1µF decoupling ceramic capacitor is required at the pin.

The 4.9V VCC can also bias other circuitries up to a 10mA load.

Forced Continuous Conduction Mode (CCM) Operation

The MPQ7235 uses forced continuous conduction mode (FCCM) to ensure that the part works with a fixed frequency across a no load to full-load range. The advantages of FCCM are its controllable frequency and lower output ripple under light loads.

Frequency Foldback

The MPQ7235 enters frequency foldback when V_{IN} exceeds about 21V. The frequency decreases to half of the nominal value and changes to 1.1MHz.

Frequency foldback also occurs during soft start (SS) and short-circuit protection (SCP).

Error Amplifier (EA)

The error amplifier (EA) compares the FB voltage (V_{FB}) to the internal 0.2V reference voltage (V_{REF}), and outputs a current proportional to the difference between the two. This I_{LED} then charges or discharges the internal compensation network to form V_{COMP}, which controls the power MOSFET current. The optimized internal compensation network minimizes the required external components and simplifies control loop design.

PWM Dimming

An external 10Hz to 2kHz PWM waveform can be applied to the DIM pin to implement PWM dimming. The average LED current is proportional to the PWM duty. The minimum amplitude of the PWM signal is 1.35V. If the dimming signal is applied before start-up, the first dimming signal's on time must exceed 5ms to ensure SS finishes, which generates I_{LED}. After the first pulse, the dimming on time can be shorter (see Figure 2). If the dimming signal is applied after SS finishes, the 5ms limit is not required.

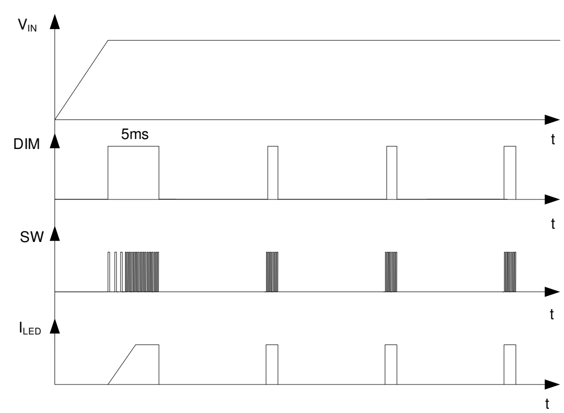


Figure 2: Timing with Active PWM Dimming

DIM is clamped internally using a 6.5V series Zener diode (see Figure 3 on page 23). Connect the DIM input through a pull-up resistor to the voltage on V_{IN}, which limits the DIM input current below 100µA. For example, with 36V connected to V_{IN}, $R_{PULL-UP} \geq (36V - 6.5V) / 100\mu A = 295k\Omega$.

To directly connect DIM to a voltage source without a pull-up resistor, the voltage source amplitude must be limited to ≤6V to prevent damage to the Zener diode.

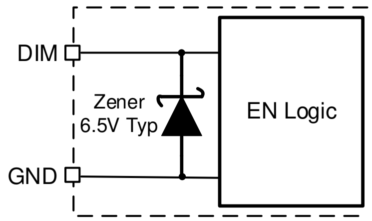


Figure 3: 6.5V Zener Diode Connection

Under-Voltage Lockout (UVLO)

Under-voltage lockout (UVLO) protects the chip from operating at an insufficient supply voltage. The UVLO comparator monitors VCC's output voltage (V_{OUT}).

Internal Soft Start (SS)

Soft start (SS) prevents the converter's V_{OUT} from overshooting during start-up. When SS begins, the internal circuitry generates a soft-start voltage (V_{SS}). If V_{SS} is below the internal V_{REF}, then V_{SS} overrides V_{REF} and the EA uses V_{SS} as the reference. If V_{SS} exceeds V_{REF}, then the EA uses V_{REF} as the reference.

During SS, the part has no fault detection, which means the /FAULT pin is pulled low.

Fault Indicator

The MPQ7235 provides fault indication. The /FAULT pin is the open drain of a MOSFET. /FAULT should be connected to VCC or another voltage source through a resistor (e.g. 100kΩ). Pull /FAULT low when the part is disabled or during thermal shutdown.

When the DIM pin remains high (no dimming), to indicate a fault status, pull /FAULT high during normal operation; pull it low during LED short/open.

For PWM dimming single input (PWM dimming), pull /FAULT high during normal operation. During LED short/open, pull /FAULT low when DIM is high; pull it high when DIM is low.

Over-Current Protection (OCP)

The MPQ7235 supports cycle-by-cycle peak current-limit protection with valley current detection. The inductor current (I_L) is monitored while the HS-FET is on. If I_L exceeds the peak current limit value (typically 6A) set by the COMP high-clamp voltage, the HS-FET turns off immediately. Then the low-side MOSFET (LS-FET) turns on to discharge the energy and I_L decreases. The HS-FET remains off unless the inductor valley current falls below a certain current threshold (typically 3.5A), even though the internal clock pulses high. If I_L does not drop below the valley current limit when the internal clock pulses high, then the HS-FET misses the clock and the switching frequency (f_{SW}) decreases to half of the nominal value. Both the peak and valley current limits help prevent I_L from running away during an overload or short-circuit condition.

Reverse Current Protection

The MPQ7235 has a 1.2A reverse current limit. Once I_L reaches the reverse current limit, the LS-FET immediately turns off and the HS-FET turns on. The current limit prevents the negative current from dropping too low and damaging the components.

Thermal Shutdown

Thermal shutdown prevents the chip from operating at exceedingly high temperatures. If the die temperature exceeds 170°C, the entire chip shuts down. Once the temperature drops below its lower threshold (typically 140°C), the chip is enabled again and resumes normal operation.

Floating Driver and Bootstrap Charging

An external bootstrap (BST) capacitor (C_{BST}) powers the floating power MOSFET driver. This floating driver has its own UVLO protection, with a rising threshold of 2.2V and hysteresis of 150mV. The C_{BST} voltage is regulated internally by V_{IN} through D1, M1, C3, L1, and C4 (see Figure 4 on page 24). If (V_{IN} - V_{SW}) exceeds 5V, then U1 regulates M1 to maintain a 5V BST voltage (V_{BST}) across C4. As long as V_{IN} sufficiently exceeds SW, C_{BST} can be charged. When the HS-FET is on, $V_{IN} \approx V_{SW}$ and C_{BST} cannot be charged. When the LS-FET is on, V_{IN} - V_{SW} reaches its maximum for fast charging. When there is no inductor current, $V_{SW} = V_{OUT}$ and the difference between V_{IN} and V_{OUT} charges C_{BST}. A 20Ω resistor placed between SW and C_{BST} is strongly recommended to reduce SW spike voltage.

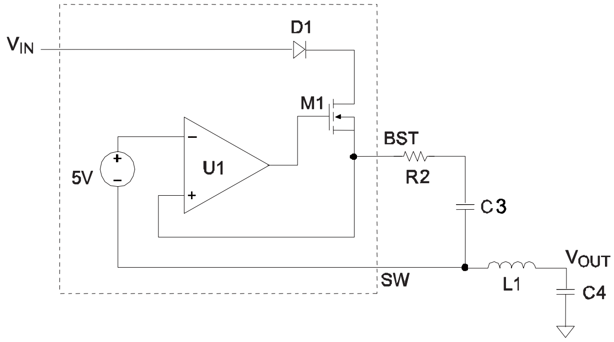


Figure 4: Internal Bootstrap Charging Circuit

Start-Up and Shutdown

If V_{IN} exceeds its appropriate threshold, the chip starts up and VCC is enabled, which provides a stable supply for the internal circuitries. Once the first DIM pulse is high, the reference block starts, followed by SS. Once SS finishes, DIM low cannot shut down the part, including the VCC regulator, and a ~380µA current flows into the part.

Two events can shut down the chip: V_{IN} low and thermal shutdown. During the shutdown procedure, the signaling path is blocked to avoid any fault triggering. V_{COMP} and the internal supply rail are then pulled down. The floating driver is not subject to this shutdown command.

APPLICATION INFORMATION

Setting the Output Current

The output current (I_{LED}) is set by the external resistor R_{FB} (see Figure 5). I_{LED} can be calculated using Equation (1):

$$I_{LED} = \frac{0.2V}{R_{FB}} \quad (1)$$

Where the feedback reference voltage is 0.2V.

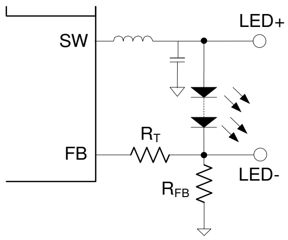


Figure 5: Feedback Network

R_T sets the loop bandwidth. A lower R_T means a higher bandwidth. However, high bandwidth may cause insufficient phase margin, resulting in loop instability. A proper R_T value must make a tradeoff between bandwidth and phase margin. Table 1 shows the recommended feedback resistor and R_T values for common output currents with 1 or 2 series LEDs.

Table 1: Resistor Selection for Common Output Currents

I_{LED} (A)	R_{FB} (mΩ)	R_T (kΩ)
0.5	400 (1%)	200
1	200 (1%)	150
1.5	133 (1%)	100
3	66.5 (1%)	100

Selecting the Input Capacitor

The step-down converter has a discontinuous input current, and requires a capacitor to supply AC current to the converter while maintaining the DC V_{IN}. For the best performance, use low-ESR capacitors. Ceramic capacitors with X5R or X7R dielectrics are highly recommended because of their low ESR and small temperature coefficients.

For most applications, use a 4.7µF to 10µF capacitor. It is strongly recommended to use another, lower-value capacitor (e.g. 0.1µF) with a small package size (0603) to absorb high-frequency switching noise. Place the small-size capacitor as close to the IN and GND pins as possible.

Since the input capacitor (C_{IN}) absorbs the input switching current, it requires an adequate ripple current rating. C_{IN}'s RMS current (I_{CIN}) can be estimated using Equation (2):

$$I_{CIN} = I_{LED} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)} \quad (2)$$

The worst-case condition occurs at V_{IN} = 2 x V_{OUT}. I_{CIN} can be calculated using Equation (3):

$$I_{CIN} = \frac{I_{LED}}{2} \quad (3)$$

For simplification, choose an input capacitor with an RMS current rating that exceeds half of the maximum load current.

The input capacitor can be electrolytic, tantalum, or ceramic. When using electrolytic or tantalum capacitors, add a small, high-quality ceramic capacitor (e.g. 0.1µF) as close to the IC as possible. When using ceramic capacitors, ensure that they have enough capacitance to provide a sufficient charge, which prevents excessive voltage ripple at input. The input voltage ripple (ΔV_{IN}) caused by the capacitance can be estimated using Equation (4):

$$\Delta V_{IN} = \frac{I_{LED}}{f_{SW} \times C_{IN}} \times \frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (4)$$

Selecting the Output Capacitor

The output capacitor (C_{OUT}) maintains the DC V_{OUT}. Use ceramic, tantalum, or low-ESR electrolytic capacitors. For the best results, use low-ESR capacitors to keep the output voltage ripple (ΔV_{OUT}) low. ΔV_{OUT} can be estimated using Equation (5):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times \left(R_{ESR} + \frac{1}{8 \times f_{SW} \times C_{OUT}}\right) \quad (5)$$

Where L is the inductance, and R_{ESR} is the equivalent series resistance (ESR) value of C_{OUT}.

For ceramic capacitors, the capacitance dominates the impedance at f_{SW} and causes the majority of ΔV_{OUT}. For simplification, ΔV_{OUT} can be estimated using Equation (6):

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times f_{SW}^{2} \times L \times C_{OUT}} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (6)$$

For tantalum or electrolytic capacitors, the ESR dominates the impedance at f_{SW}. For simplification, ΔV_{OUT} can be estimated using Equation (7):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \times R_{ESR} \quad (7)$$

The C_{OUT} characteristics also affect the stability of the regulation system. The MPQ7235 can be optimized for a wide range of capacitances and ESR values.

Selecting the Inductor

A 1µH to 10µH inductor with a DC current rating at least 25% above the maximum load current is recommended for most applications. For higher efficiency, choose an inductor with lower DC resistance. A larger-value inductor results in reduced ripple current and a lower ΔV_{OUT}; however, it also has a larger physical size, higher series resistance, and lower saturation current. A good rule for determining the inductance is to allow the inductor ripple current to be approximately 30% of the maximum load current. The inductance (L) can then be calculated using Equation (8):

$$L = \frac{V_{OUT}}{f_{SW} \times \Delta I_L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (8)$$

Where ΔI_L is the peak-to-peak inductor ripple current.

Choose the inductor ripple current to be approximately 30% of the maximum load current. The maximum inductor peak current (I_{LP}) can be calculated using Equation (9):

$$I_{LP} = I_{LED} + \frac{V_{OUT}}{2f_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (9)$$

For the typical application circuit design (see Figure 9 on page 28), a 2.2µH inductor is sufficient, and the VCHA042A-2R2MS6-89 is recommended.

Selecting the BST Resistor and External BST Diode

A 20Ω resistor in series with C_{BST} is recommended to reduce the SW spike voltage. Higher resistance is better for reducing the SW spike, with the tradeoff of compromising efficiency.

An external BST diode can enhance the regulator's efficiency when the duty cycle is high (>65%). A power supply between 2.5V and 5V can power the external BST diode, such as VCC or V_{OUT} (see Figure 6).

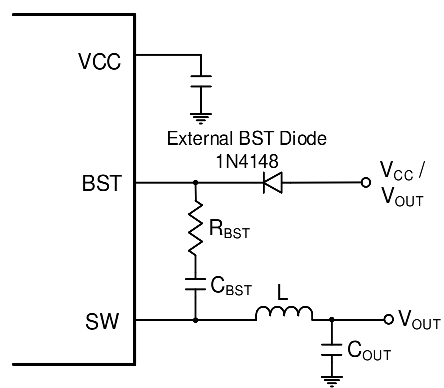


Figure 6: Optional External BST Diode to Enhance Efficiency

The recommended external BST diode is 1N4148, and the recommended C_{BST} range is 0.1µF to 1µF.

Low Dimming Frequency Application

For applications with low PWM dimming frequencies at small dimming duty cycles, the V_{COMP} (the EA's V_{OUT}) may be discharged by the leakage if dimming off time is too long. The minimum dimming frequency should be at least 10Hz.

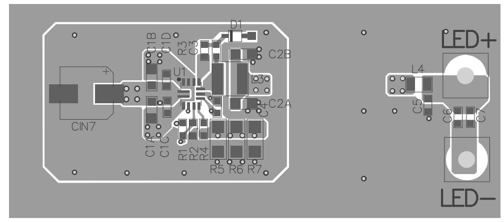
PCB Layout Guidelines [12]

Efficient PCB layout is critical for stable operation. The small board size of the MPQ7235 makes it suitable for IR applications. A 4-layer layout is strongly recommended to improve thermal performance. For the best results, refer to Figure 7 and follow the guidelines below:

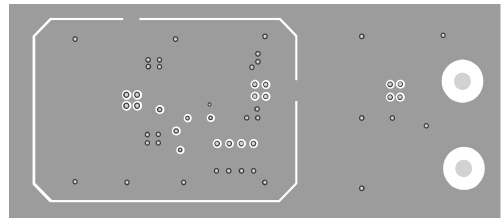
1. Use a large ground plane to connect directly to PGND. If the bottom layer is a ground plane, add vias near PGND.
2. Ensure that the high-current paths at PGND and IN have short, direct, and wide traces.
3. Place the ceramic input capacitor, especially the small package (0603) input bypass capacitor, as close to the IN and PGND pins as possible to minimize high-frequency noise. Keep the connection between the input capacitor and IN as short and wide as possible.
4. Place the VCC capacitor as close to the VCC and GND pins as possible.
5. Route SW and BST away from sensitive analog areas, such as FB.
6. Place the feedback resistors close to the chip to ensure the trace connected to FB is as short as possible.
7. Use multiple vias to connect the power planes to the internal layers.

Note:

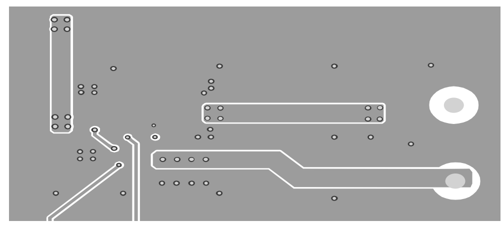
12) The recommended PCB layout is based on the Typical Application Circuit (see Figure 8 on page 28).



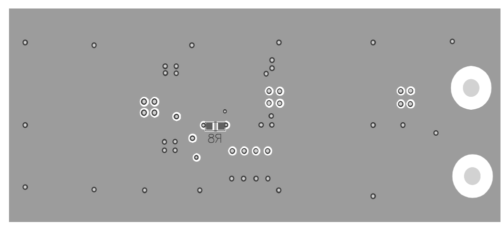
Top Layer



Mid-Layer 1



Mid-Layer 2



Bottom Layer

Figure 7: Recommended PCB Layout [12]

TYPICAL APPLICATION CIRCUITS

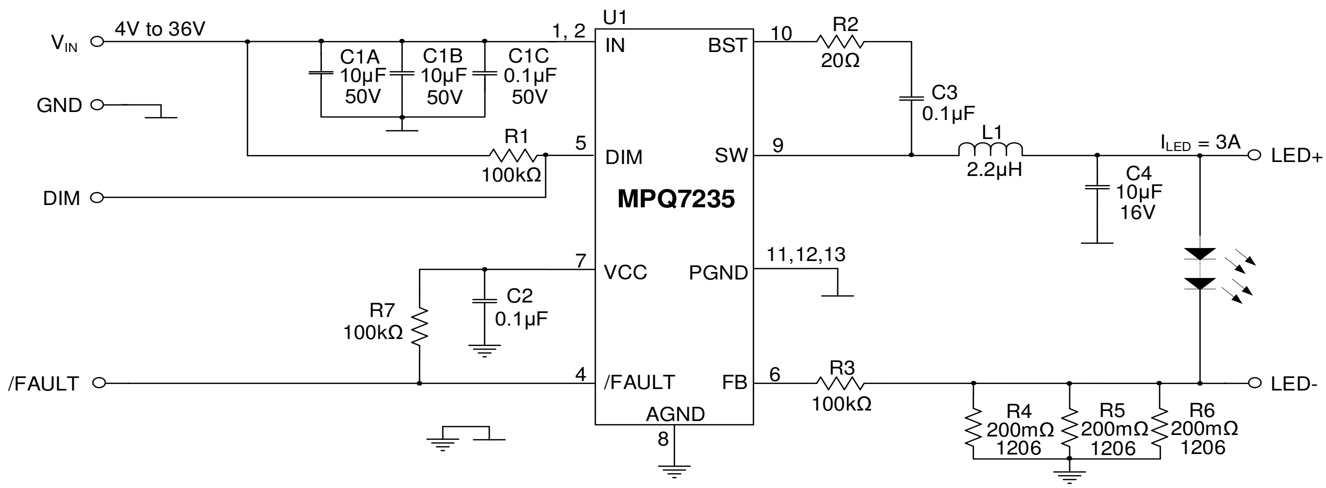


Figure 8: Typical Application Circuit (I_{LED} = 3A)

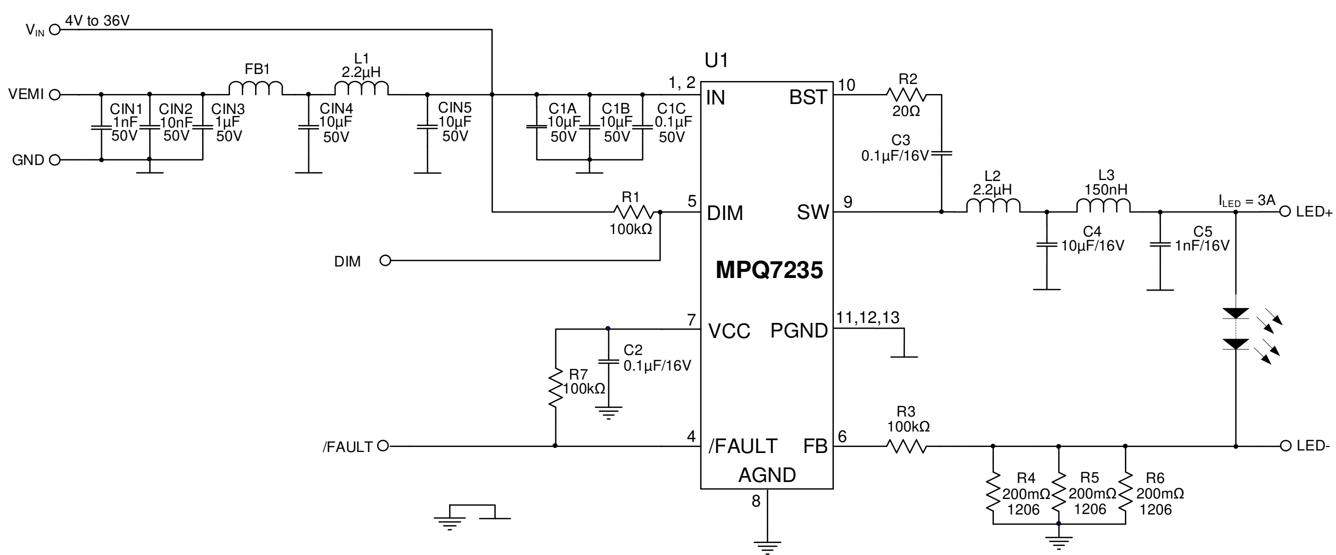
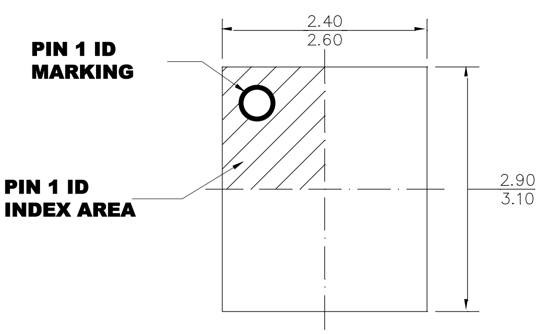


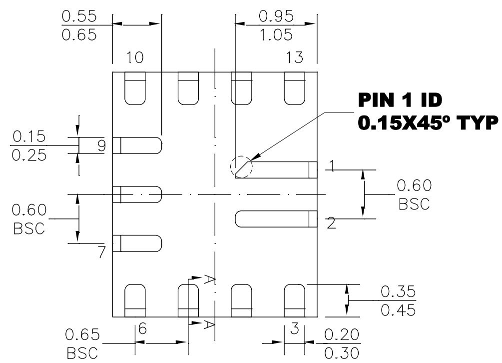
Figure 9: Typical Application Circuit with EMI Filters (I_{LED} = 3A)

PACKAGE INFORMATION

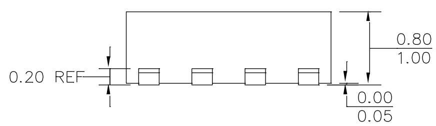
QFN-13 (2.5mmx3mm)
Wettable Flank



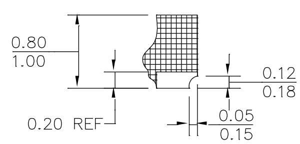
TOP VIEW



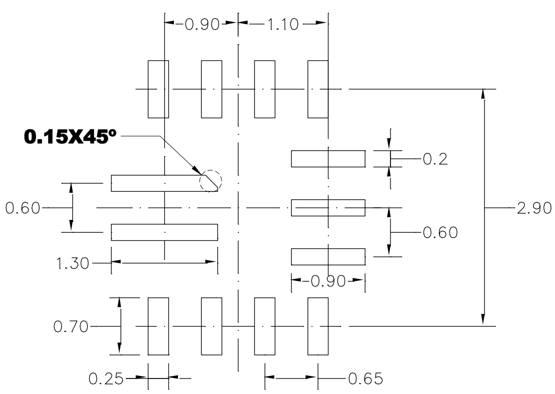
BOTTOM VIEW



SIDE VIEW



SECTION A-A

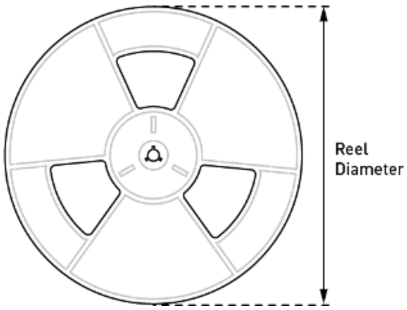


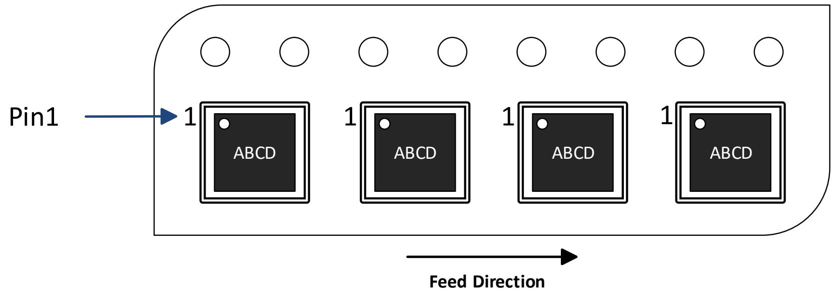
RECOMMENDED LAND PATTERN

NOTE:

1) THE LEAD SIDE IS WETTABLE.
2) ALL DIMENSIONS ARE IN MILLIMETERS.
3) LEAD COPLANARITY SHALL BE 0.08 MILLIMETERS MAX.
4) JEDEC REFERENCE IS MO-220.
5) DRAWING IS NOT TO SCALE.

CARRIER INFORMATION





Part Number	Package Description	Quantity /Reel	Quantity /Tube	Quantity /Tray	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MPQ7235GQBE-AEC1-Z	QFN-13 (2.5mmx3mm)	5000	N/A	N/A	13in	12mm	8mm

REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	12/17/2021	Initial Release	-