TUSB2036 2- or 3-Port Hub for the Universal Serial Bus With Optional Serial EEPROM Interface

1 Features

- Fully Compliant With the USB Specification as a Full-Speed Hub: TID #30220242
- Integrated USB Transceivers
- 3.3-V Low-Power ASIC Logic
- One Upstream Port and 2 or 3 Programmable Downstream Ports
  - Total Number of Ports (2 or 3) Selected by Input Pin
  - Total Number of Permanently Connected Ports Is Selected by 2 Input Pins
- Two Power Source Modes
  - Self-Powered Mode
  - Bus-Powered Mode
- All Downstream Ports Support Full-Speed and Low-Speed Operations
- Power Switching and Overcurrent Reporting Is Provided Ganged or Per Port
- Supports Suspend and Resume Operations
- Suspend Status Pin Available for External Logic Power Down
- Supports Custom Vendor ID and Product ID With External Serial EEPROM
- 3-State EEPROM Interface Allows EEPROM Sharing
- Push-Pull Outputs for $\overline{\text{PWRON}}$ Eliminate the Need for External Pullup Resistors
- Noise Filtering on $\overline{\text{OVRCUR}}$ Provides Immunity to Voltage Spikes
- Supports 6-MHz Operation Through a Crystal Input or a 48-MHz Input Clock
- Output Pin Available to Disable External Pullup Resister on DP0 for 3 ms After Reset or After Change on $\overline{\text{BUSPWR}}$ and Enable Easy Implementation of Onboard Bus/Self-Power Dynamic Switching Circuitry
- No Special Driver Requirements; Works Seamlessly With Any Operating System With USB Stack Support
- Available in 32-Pin HLQFP Package With a 0.8-mm Pin Pitch (JEDEC − S-PQFP-G For Low-Profile Quad Flat Pack)

2 Applications

- Computer Systems
- Docking Stations

3 Description

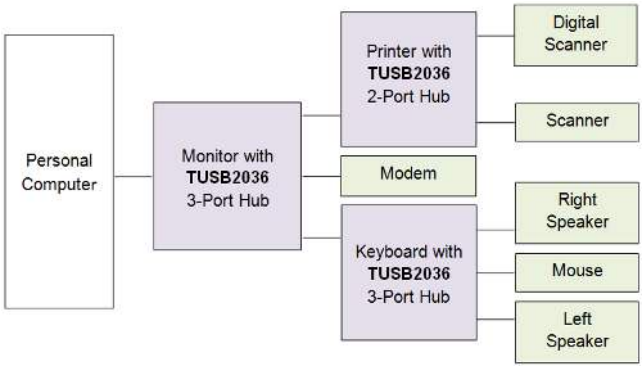
The TUSB2036 hub is a 3.3-V CMOS device that provides up to three downstream ports in compliance with the USB 2.0 specification. Because this device is implemented with a digital state machine instead of a microcontroller, no firmware programming is required. Fully-compliant USB transceivers are integrated into the ASIC for all upstream and downstream ports. The downstream ports support both full-speed and low-speed devices by automatically setting the slew rate according to the speed of the device attached to the ports. The configuration of the $\overline{\text{BUSPWR}}$ pin selects either the bus-powered or the self-powered mode. The introduction of the DP0 pullup resistor disable pin, DP0PUR, makes it much easier to implement an onboard bus/self-power dynamic-switching circuitry. With the new function pin, the end-equipment vendor can reduce the total board cost while adding additional product value.

Device Information[1]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TUSB2036	HLQFP (32)	7.00 mm × 7.00 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

USB-Tiered Configuration Example



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4 Revision History

Changes from Revision H (January 2016) to Revision I — **Page**

- Changed pin $\overline{\text{OVRCUR1}}$, $\overline{\text{OVRCUR2}}$ and $\overline{\text{OVRCUR3}}$ I/O column From: "O" To: "I" in the *Pin Functions* table ... 5
- Changed pin MODE, $\overline{\text{NP3}}$, NPINT1−0 and V_{CC} I/O column From: – To: "I" in the *Pin Functions* table ... 5

Changes from Revision G (May 2015) to Revision H — **Page**

- Changed the description of $f_{(OPRH)}$ From: "high speed mode" To: "full speed mode" in the *Recommended Operating Conditions* ... 6

Changes from Revision F (September 2013) to Revision G — **Page**

- Added *Pin Configuration and Functions* section, *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1

5 Description (Continued)

The $\overline{\text{EXTMEM}}$ (pin 26) enables or disables the optional EEPROM interface. When $\overline{\text{EXTMEM}}$ is high, the vendor and product IDs (VID and PID) use defaults, such that the message displayed during enumeration is General Purpose USB Hub.

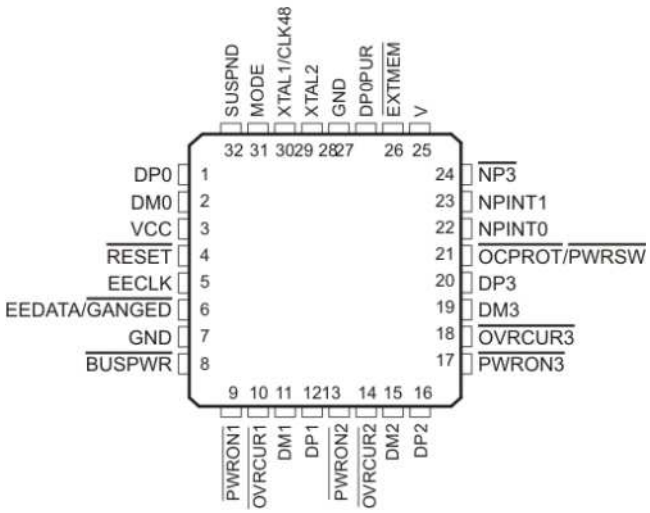
The TUSB2036 supports both bus-powered and self-powered modes. External power-management devices, such as the TPS2044, are required to control the 5-V power source switching (on/off) to the downstream ports and to detect an overcurrent condition from the downstream ports individually or ganged.

An individually port power controlled hub switches power on or off to each downstream port as requested by the USB host. Also when an individually port power controlled hub senses an over-current event, only power to the affected downstream port will be switched off. A ganged hub switches on power to all its downstream ports when power is required to be on for any port. The power to the downstream ports is not switched off unless all ports are in a state that allows power to be removed. Also when a ganged hub senses an over-current event, power to all downstream ports will be switched off.

The logic level of the MODE pin controls the selection of a crystal input to drive an internal oscillator or an external clock source.

6 Pin Configuration and Functions

VF Package
32-PIN HLQFP
(Top View)



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
BUSPWR	8	I	Power source indicator. BUSPWR is an active-low input that indicates whether the downstream ports source their power from the USB cable or a local power supply. For the bus-power mode, this pin must be pulled low, and for the self-powered mode, this pin must be pulled to 3.3 V. Input must not change dynamically during operation.
DM0	2	I/O	Root port USB differential data minus. DM0 paired with DP0 constitutes the upstream USB port.
DM1	11	I/O	USB differential data minus. DM1–DM3 paired with DP1–DP3 support up to four downstream USB ports.
DM2	15		
DM3	19		
DP0	1	I/O	Root port USB differential data plus. DP0 paired with DM0 constitutes the upstream USB port.
DP0PUR	27	O	Pullup resistor connection. When a system reset happens (RESET being driven to low, but not USB reset) or any logic level change on BUSPWR pin, DP0PUR output is inactive (floating) until the internal counter reaches a 15-ms time period. After the counter expires, DP0PUR is driven to the VCC (3.3 V) level thereafter until the next system reset event occurs or there is a BUSPWR logic level change.
DP1	12	I/O	USB differential data plus. DP1–DP3 paired with DM1–DM3 support up to four downstream USB ports.
DP2	16		
DP3	20		
EECLK	5	O	EEPROM serial clock. When EXTMEM is high, the EEPROM interface is disabled. The EECLK pin is disabled and must be left floating (unconnected). When EXTMEM is low, EECLK acts as a 3-state serial clock output to the EEPROM with a 100-μA internal pulldown.
EEDATA/ GANGED	6	I/O	EEPROM serial data/power-management mode indicator. When EXTMEM is high, EEDATA/GANGED selects between ganged or per-port power overcurrent detection for the downstream ports. When EXTMEM is low, EEDATA/GANGED acts as a serial data I/O for the EEPROM and is internally pulled down with a 100-μA pulldown. This standard TTL input must not change dynamically during operation.
EXTMEM	26	I	When EXTMEM is high, the serial EEPROM interface of the device is disabled. When EXTMEM is low, pins 5 and 6 are configured as the clock and data pins of the serial EEPROM interface, respectively.
GND	7, 28		GND pins must be tied to ground for proper operation.

Pin Functions (continued)

PIN		I/O	DESCRIPTION
NAME	NO.		
$\overline{\text{OCPROT}}$/ $\overline{\text{PWRSW}}$	21	I	Overcurrent Protection for bus-powered hub (active low). /Power Switching for self-powered hub (active low). The pin has a different meaning for the bus or self-powered hub. If the pin is logic high the internal pulldown is disabled.(1) (2)
$\overline{\text{OVRCUR1}}$	10	I	Overcurrent input. $\overline{\text{OVRCUR1}}$ – $\overline{\text{OVRCUR3}}$ are active low. For per-port overcurrent detection, one overcurrent input is available for each of the three downstream ports. In the ganged mode, any $\overline{\text{OVRCUR}}$ input may be used and all $\overline{\text{OVRCUR}}$ pins must be tied together. $\overline{\text{OVRCUR}}$ pins are active low inputs with noise filtering logic. Each $\overline{\text{OVRCUR}}$n input is sampled every 2 ms and any input which is valid for two consecutive samples will be passed to the internal logic. $\overline{\text{OVRCUR3}}$ has an internal pull-up that can be enabled for the 2-port operation.
$\overline{\text{OVRCUR2}}$	14		
$\overline{\text{OVRCUR3}}$	18		
$\overline{\text{PWRON1}}$	9	O	Power-on/-off control signals. $\overline{\text{PWRON1}}$–$\overline{\text{PWRON3}}$ are active low, push-pull outputs that enables the external power switch device. Push-pull outputs eliminate the pullup resistors which open-drain outputs require. However, the external power switches that connect to these pins must be able to operate with 3.3-V inputs because these outputs cannot drive 5-V signals.
$\overline{\text{PWRON2}}$	13		
$\overline{\text{PWRON3}}$	17		
$\overline{\text{RESET}}$	4	I	$\overline{\text{RESET}}$ is an active low TTL input with hysteresis and must be asserted at power up. When $\overline{\text{RESET}}$ is asserted, all logic is initialized. Generally, a reset with a pulse width between 100 μs and 1 ms is recommended after 3.3-V V_{CC} reaches its 90%. Clock signal has to be active during the last 60 μs of the reset window.
SUSPND	32	O	Suspend status. SUSPND is an active high output available for external logic power-down operations. During the suspend mode, SUSPND is high. SUSPND is low for normal operation.
MODE	31	I	Mode select. When MODE is low, the APLL output clock is selected as the clock source to drive the internal core of the device and 6-MHz crystal or oscillator can be used. When MODE is high, the clock on XTAL1/CLK48 is selected as the clock source and 48-MHz oscillator or other on-board clock source can be used.
$\overline{\text{NP3}}$	24	I	Number of ports is 3. Active low input. A logic 0 configures the system to use 3 ports. A logic 1 configures the system to use 2 ports.
NPINT0	22	I	Number of ports internal to hub system, which are permanently attached (see Table 1).
NPINT1	23		
V_{CC}	3, 25	I	3.3-V supply voltage
XTAL1/CLK48	30	I	Crystal 1/48-MHz clock input. When MODE is low, XTAL1/CLK48 is a 6-MHz crystal input with 50% duty cycle. An internal APLL generates the 48-MHz and 12-MHz clocks used internally by the ASIC logic. When MODE is high, XTAL1/CLK48 acts as the input of the 48-MHz clock and the internal APLL logic is bypassed.
XTAL2	29	O	Crystal 2. XTAL2 is a 6-MHz crystal output. This pin must be left open when using an oscillator.

(1) If the hub is implemented to be bus-powered (via $\overline{\text{BUSPWR}}$ tying to GND):
  (a) TUSB2036 reports to the host that the hub end-product downstream ports are power-switched (this is required by the USB 2.0 specification). Hub end-product vendor has to ensure the actual end-product implementation meets this specification requirement.
  (b) Pin 21 acts as overcurrent protection ($\overline{\text{OCPROT}}$) implementation indication pin for the bus-powered hub. The overcurrent protection implementation is reported through the wHubCharacteristics. D4 bit in the hub descriptor.
  (c) When $\overline{\text{OCPROT}}$ is low, the TUSB2036 reports to the host that the hub end-product provides overcurrent protection and the wHubCharacteristics. D4 bit is set to 0.
  (d) When $\overline{\text{OCPROT}}$ is high, the TUSB2036 reports to the host that the hub end-product does not provide overcurrent protection and the wHubCharacteristics. D4 bit is set to 1.

(2) If the hub is implemented to be self-powered (via $\overline{\text{BUSPWR}}$ tying to 3.3-V V_{CC}):
  (a) TUSB2036 reports to the host that the hub end-product provides overcurrent protection to the downstream ports (this is required by the USB 2.0 specification). Hub end-product vendor has to ensure the actual end-product implementation meets this specification requirement.
  (b) Pin 21 acts as power switching ($\overline{\text{PWRSW}}$) implementation indication pin for the self-powered hub. The power-switching implementation is reported through the bPwrOn2PwrGood field in the hub descriptor.
  (c) When $\overline{\text{PWRSW}}$ is low, the TUSB2036 reports to the host that the hub end-product has port power switching at the downstream ports and the bPwrOn2PwrGood is set to 50 units (100 ms).
  (d) When $\overline{\text{PWRSW}}$ is high, the TUSB2036 reports to the host that the hub end-product does not have port power switching at the downstream ports and the bPwrOn2PwrGood is set to 0 units (0 ms).

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage(2)		–0.5	3.6	V
V_I	Input voltage		–0.5	V_{CC} + 0.5	V
V_O	Output voltage		–0.5	V_{CC} + 0.5	V
I_{IK}	Input clamp current	V_I < 0 V or V_I < V_{CC}		±20	mA
I_{OK}	Output clamp current	V_O < 0 V or V_O < V_{CC}		±20	mA
T_A	Operating free-air temperature		0	70	°C
T_{stg}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage levels are with respect to GND.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±4000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

	PARAMETER	MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	3	3.3	3.6	V
V_I	Input voltage, TTL/LVCMOS(1)	0		V_{CC}	V
V_O	Output voltage, TTL/LVCMOS(2)	0		V_{CC}	V
$V_{IH(REC)}$	High-level input voltage, signal-ended receiver	2		V_{CC}	V
$V_{IL(REC)}$	Low-level input voltage, signal-ended receiver			0.8	V
$V_{IH(TTL)}$	High-level input voltage, TTL/LVCMOS(1)	2		V_{CC}	V
$V_{IL(TTL)}$	Low-level input voltage, TTL/LVCMOS(1)	0		0.8	V
T_A	Operating free-air temperature	0		70	°C
$R_{(DRV)}$	External series, differential driver resistor	22 (–5%)		22 (+5%)	Ω
$f_{(OPRH)}$	Operating (dc differential driver) full speed mode			12	Mb/s
$f_{(OPRL)}$	Operating (dc differential driver) low speed mode			1.5	Mb/s
V_{ICR}	Common mode, input range, differential receiver	0.8		2.5	V
t_t	Input transition times, TTL/LVCMOS(1)	0		25	ns
T_J	Junction temperature range(3)	0		115	°C

(1) Applies for input and bidirectional buffers.
(2) Applies for output and bidirectional buffers.
(3) These junction temperatures reflect simulated conditions. Absolute maximum junction temperature is 150°C. The customer is responsible for verifying junction temperature.

7.4 Thermal Information

THERMAL METRIC[1]		TUSB2036 VF (HLQFP) 32 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	71.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	32.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	29.4	°C/W
ψ_{JT}	Junction-to-top characterization parameter	2.4	°C/W
ψ_{JB}	Junction-to-board characterization parameter	29.2	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

7.5 Electrical Characteristics

over recommended ranges of operating free-air temperature and supply voltage (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	MAX	UNIT
V_{OH}	High-level output voltage	TTL/LVCMOS	I_{OH} = –4 mA	V_{CC} – 0.5		V
		USB data lines	$R_{(DRV)}$ = 15 kΩ to GND	2.8		
			I_{OH} = –12 mA (without $R_{(DRV)}$)	V_{CC} – 0.5		
V_{OL}	Low-level output voltage	TTL/LVCMOS	I_{OL} = 4 mA		0.5	V
		USB data lines	$R_{(DRV)}$ = 1.5 kΩ to 3.6 V		0.3	
			I_{OL} = 12 mA (without $R_{(DRV)}$)		0.5	
V_{IT+}	Positive input threshold	TTL/LVCMOS			1.8	V
		Single-ended	0.8 V ≤ V_{ICR} ≤ 2.5 V		1.8	
$V_{IT–}$	Negative-input threshold	TTL/LVCMOS		0.8		V
		Single-ended	0.8 V ≤ V_{ICR} ≤ 2.5 V	1		
V_{hys}	Input hysteresis[1] ($V_{T+} – V_{T–}$)	TTL/LVCMOS		0.3	0.7	mV
		Single-ended	0.8 V ≤ V_{ICR} ≤ 2.5 V	300	500	
I_{OZ}	High-impedance output current	TTL/LVCMOS	V = V_{CC} or GND[2]		±10	µA
		USB data lines	0 V ≤ V_O ≤ V_{CC}		±10	
I_{IL}	Low-level input current	TTL/LVCMOS	V_I = GND		–1	µA
I_{IH}	High-level input current	TTL/LVCMOS	V_I = V_{CC}		1	µA
$z_{0(DRV)}$	Driver output impedance	USB data lines	Static V_{OH} or V_{OL}	7.1	19.9	Ω
V_{ID}	Differential input voltage	USB data lines	0.8 V ≤ V_{ICR} ≤ 2.5 V	0.2		V
I_{CC}	Input supply current		Normal operation		40	mA
			Suspend mode		1	µA

(1) Applies for input buffers with hysteresis.
(2) Applies for open drain buffers.

7.6 Differential Driver Switching Characteristics (Full Speed Mode)

over recommended ranges of operating free-air temperature and supply voltage, C_L = 50 pF (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
t_r	Transition rise time for DP or DM	See Figure 1 and Figure 2	4	20	ns
t_f	Transition fall time for DP or DM	See Figure 1 and Figure 2	4	20	ns
$t_{(RFM)}$	Rise/fall time matching[1]	(t_r/t_f) × 100	90%	110%	
$V_{O(CRS)}$	Signal crossover output voltage[1]		1.3	2.0	V

(1) Characterized only. Limits are approved by design and are not production tested.

7.7 Differential Driver Switching Characteristics (Low Speed Mode)

over recommended ranges of operating free-air temperature and supply voltage, C_L = 50 pF (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
t_r	Transition rise time for DP or DM(1)	C_L = 200 pF to 600 pF, See Figure 1 and Figure 2	75	300	ns
t_f	Transition fall time for DP or DM(1)	C_L = 200 pF to 600 pF, See Figure 1 and Figure 2	75	300	ns
$t_{(RFM)}$	Rise/fall time matching(1)	(t_r/t_f) × 100	80%	120%	
$V_{O(CRS)}$	Signal crossover output voltage(1)	C_L = 200 pF to 600 pF	1.3	2.0	V

(1) Characterized only. Limits are approved by design and are not production tested.

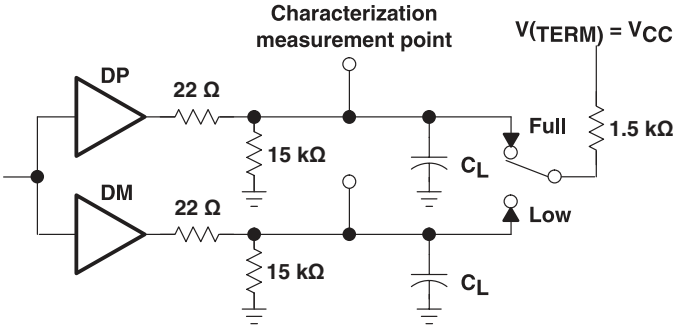
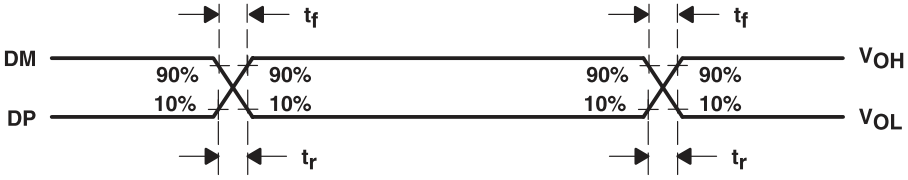


Figure 1. Differential Driver Switching Load



NOTE: The t_r/t_f ratio is measured as $t_{r(DP)}/t_{f(DM)}$ and $t_{r(DM)}/t_{f(DP)}$ at each crossover point.

Figure 2. Differential Driver Timing Waveforms

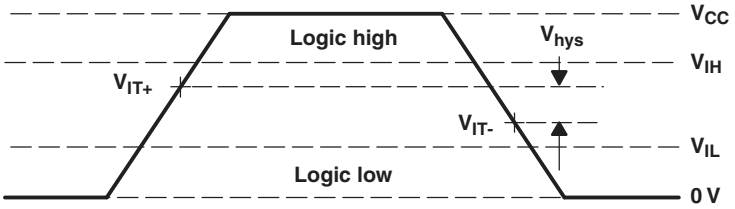


Figure 3. Single-Ended Receiver Input Signal Parameter Definitions

7.8 Typical Characteristics

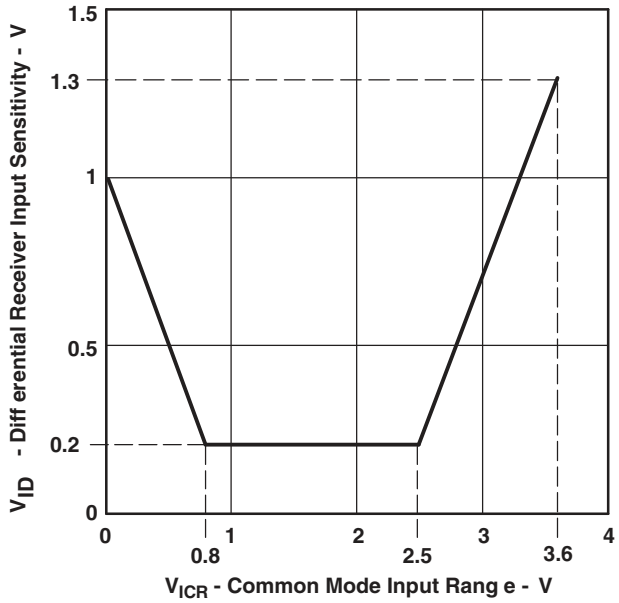


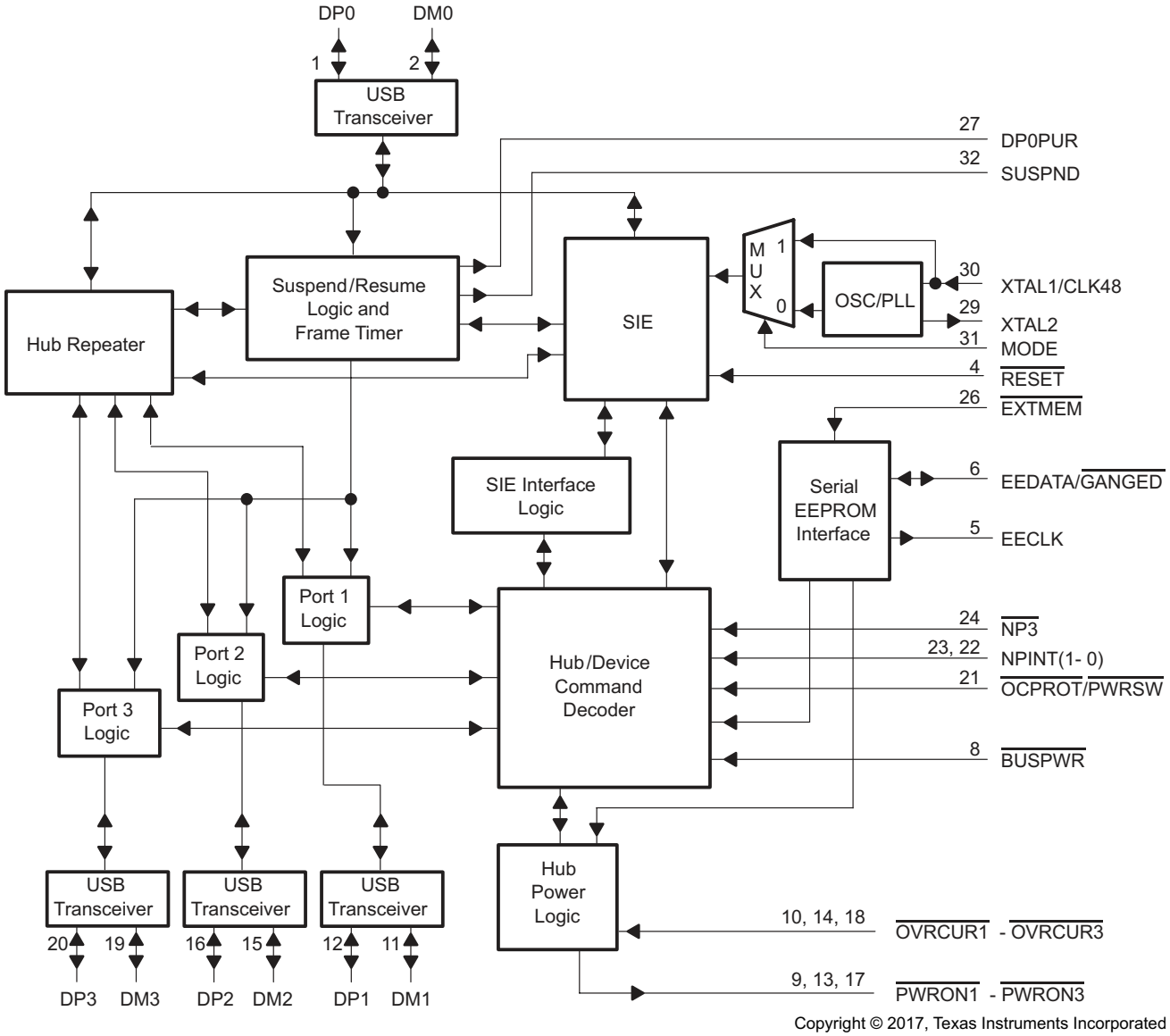
Figure 4. Differential Receiver Input Sensitivity vs Common Mode Input Range

8 Detailed Description

8.1 Overview

The TUSB2036 hub is a 3.3-V CMOS device that provides up to three downstream ports in compliance with the USB 2.0 specification. Because this device is implemented with a digital state machine instead of a microcontroller, no firmware programming is required. Fully-compliant USB transceivers are integrated into the ASIC for all upstream and downstream ports. The downstream ports support both full-speed and low-speed devices by automatically setting the slew rate according to the speed of the device attached to the ports.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 USB Power Management

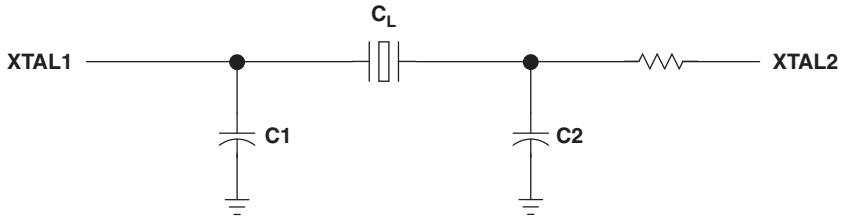
The TUSB2036 supports both bus-powered and self-powered modes. External power-management devices, such as the TPS2044, are required to control the 5-V power source switching (on/off) to the downstream ports and to detect an overcurrent condition from the downstream ports individually or ganged. Outputs from external power devices provide overcurrent inputs to the TUSB2036 $\overline{\text{OVRCUR}}$ pins in case of an overcurrent condition, the corresponding $\overline{\text{PWRON}}$ pins are disabled by the TUSB2036. In the ganged mode, all $\overline{\text{PWRON}}$ signals transition simultaneously, and any $\overline{\text{OVRCUR}}$ input can be used. In the nonganged mode, the $\overline{\text{PWRON}}$ outputs and $\overline{\text{OVRCUR}}$ inputs operate on a per-port basis.

Both bus-powered and self-powered hubs require overcurrent protection for all downstream ports. The two types of protection are individual-port management (individual-port basis) or ganged-port management (multiple-port basis). Individual-port management requires power-management devices for each individual downstream port, but adds robustness to the USB system because, in the event of an overcurrent condition, the USB host only powers down the port that has the condition. The ganged configuration uses fewer power management devices and thus has lower system costs, but in the event of an overcurrent condition on any of the downstream ports, all the ganged ports are disabled by the USB host.

Using a combination of the $\overline{\text{BUSPWR}}$ and EEDATA/$\overline{\text{GANGED}}$ inputs, the TUSB2036 supports four modes of power management: bus-powered hub with either individual-port power management or ganged-port power management, and the self-powered hub with either individual-port power management or ganged-port power management. Texas Instruments supplies the complete hub solution because we offer this TUSB2036 along with the power-management devices needed to implement a fully USB compliant system.

8.3.2 Clock Generation

The TUSB2036 provides the flexibility of using either a 6-MHz or a 48-MHz clock. The logic level of the MODE pin controls the selection of the clock source. When MODE is low, the output of the internal APLL circuitry is selected to drive the internal core of the chip. When MODE is high, the XTAL1 input is selected as the input clock source and the APLL circuitry is powered down and bypassed. The internal oscillator cell is also powered down while MODE is high. For 6-MHz operation, TUSB2036 requires a 6-MHz clock signal on XTAL1 pin (with XTAL2 for a crystal) from which its internal APLL circuitry generates a 48-MHz internal clock to sample the data from the upstream port. For 48-MHz operation, the clock cannot be generated with a crystal, using the XTAL2 output, since the internal oscillator cell only supports the fundamental frequency. If low-power suspend and resume are desired, a passive crystal or resonator must be used, although the hub supports the flexibility of using any device that generates a 6-MHz clock. Because most oscillators cannot be stopped while power is on, their use prohibits low-power suspend, which depends on disabling the clock. When the oscillator is used, by connecting its output to the XTAL1 pin and leaving the XTAL2 pin open, its TTL output level cannot exceed 3.6V. If a 6-MHz oscillator is used, it must be stopped at logic low whenever SUSPND is high. For crystal or resonator implementations, the XTAL1 pin is the input and the XTAL2 pin is used as the feedback path. A sample crystal tuning circuit is shown in Figure 5.



NOTE: This figure assumes a 6-MHz fundamental crystal that is parallel loaded. The component values of C1, C2, and R_d are determined using a crystal from Fox Electronics – part number HC49U-6.00MHz 30\50\0±70\20, which means ±30 ppm at 25°C and ±50 ppm from 0°C to 70°C. The characteristics for the crystal include a load capacitance (C_L) of 20 pF, maximum shunt capacitance (C_o) of 7 pF, and the maximum ESR of 50 Ω. In order to insure enough negative resistance, use C1 = C2 = 27 pF. The resistor R_d is used to trim the gain, and R_d = 1.5 kΩ is recommended.

Figure 5. Crystal Tuning Circuit

8.4 Device Functional Modes

8.4.1 2-3 Programmable Downstream Ports

The hub silicon can accurately reflect the system port configuration by the NP3 and NPINT1-0 pins. When NP3 is low, the hub is configured as a 3-port hub; when it is high, the hub is configured as a 2-port hub. The NPINT1-0 pins tell the hub silicon how many ports have permanently attached devices, according to Table 1.

Table 1. System Port Configuration

NPINT1-0	PORT AVAILABILITY	HUB DESCRIPTOR DEVICE REMOVABLE FIELD (7–0)
00	All ports are available through external USB connectors	00000000
01	Port 1 has a permanently attached device; ports 2 and 3 are externally available	00000010
10	Ports 1 and 2 have permanently attached devices; port 3 is externally available	00000110
11	All ports have permanently attached devices	$\overline{NP3}$ high: 00000110 $\overline{NP3}$ low: 00001110
NPINT1-0	**COMPOUND DEVICE OR NOT**	**HUB DESCRIPTOR WITH HUB CHARACTERISTICS FIELD BIT 2**
00	Hub is not part of a compound device	0
01, 10, 11	Hub is part of a compound device	1

8.4.2 Vendor ID and Product ID With External Serial EEPROM

The $\overline{EXTMEM}$ (pin 26) enables or disables the optional EEPROM interface. When $\overline{EXTMEM}$ is high, the vendor and product IDs (VID and PID) use defaults, such that the message displayed during enumeration is General Purpose USB Hub. For this configuration, pin 6 functions as the GANGED input terminal and the ECLK (pin 5) is unused. If custom VID and PID descriptors are desired, the $\overline{EXTMEM}$ must be tied low ($\overline{EXTMEM}$ = 0) and a SGS Thompson M93C46 EEPROM, or equivalent, stores the programmable VID, PID, and GANGED values. For this configuration, pins 5 and 6 function as the EEPROM interface signals with pin 5 as EECLK and pin 6 as EEDATA, respectively. A block diagram example of how to connect the external EEPROM if a custom product ID and vendor ID are desired is shown in Figure 6.

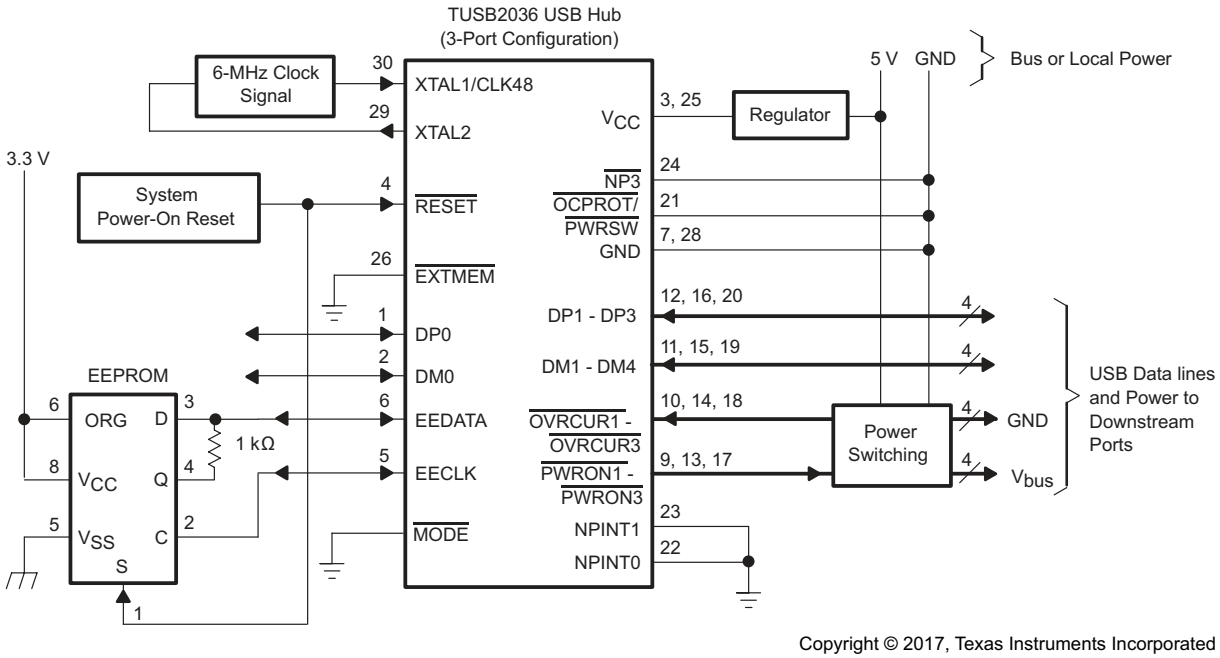


Figure 6. TUSB2036 USB Hub With External EEPROM

8.5 Programming

8.5.1 Programming the EEPROM

An SGS Thompson M93C46 EEPROM, or equivalent, stores the programmable VID and PID. When the EEPROM interface is enabled ($\overline{\text{EXTMEM}}$ = 0), the EECLK and EEDATA are internally pulled down (100 μA) inside the TUSB2036. The internal pulldowns are disabled when the EEPROM interface is disabled ($\overline{\text{EXTMEM}}$ = 1).

The EEPROM is programmed with the three 16-bit locations as shown in Table 2. Connecting pin 6 of the EEPROM high (ORG = 1) organizes the EEPROM memory into 64×16-bit words.

Table 2. EEPROM Memory Map

ADDRESS	D15	D14	D13	D12–D8	D7–D0
00000	0	$\overline{\text{GANGED}}$	00000	00000	00000000
00001	VID High-byte				VID Low-byte
00010	PID High-byte				PID Low-byte
	XXXXXXXX				

The D and Q signals of the EEPROM must be tied together using a 1-kΩ resistor with the common I/O operations forming a single-wire bus. After system power-on reset, the TUSB2036 performs a one-time access read operation from the EEPROM if the $\overline{\text{EXTMEM}}$ pin is pulled low and the chip select(s) of the EEPROM is connected to the system power-on reset. Initially, the EEDATA pin is driven by the TUSB2036 to send a start bit (1) which is followed by the read instruction (10) and the starting-word address (00000). Once the read instruction is received, the instruction and address are decoded by the EEPROM, which then sends the data to the output shift register. At this point, the hub stops driving the EEDATA pin and the EEPROM starts driving. A dummy (0) bit is then output and the first three 16-bit words in the EEPROM are output with the most significant bit (MSB) first.

The output data changes are triggered by the rising edge of the clock provided by the TUSB2036 on the EECLK pin. The SGS-Thompson M936C46 EEPROM is recommended because it advances to the next memory location by automatically incrementing the address internally. Any EEPROM used must have the automatic internal address advance function. After reading the three words of data from the EEPROM, the TUSB2036 puts the EEPROM interface into a high-impedance condition (pulled down internally) to allow other logic to share the EEPROM. The EEPROM read operation is summarized in Figure 7. For more details on EEPROM operation, refer to *SGS-Thompson Microelectronics M93C46 Serial Microwire Bus EEPROM* data sheet.

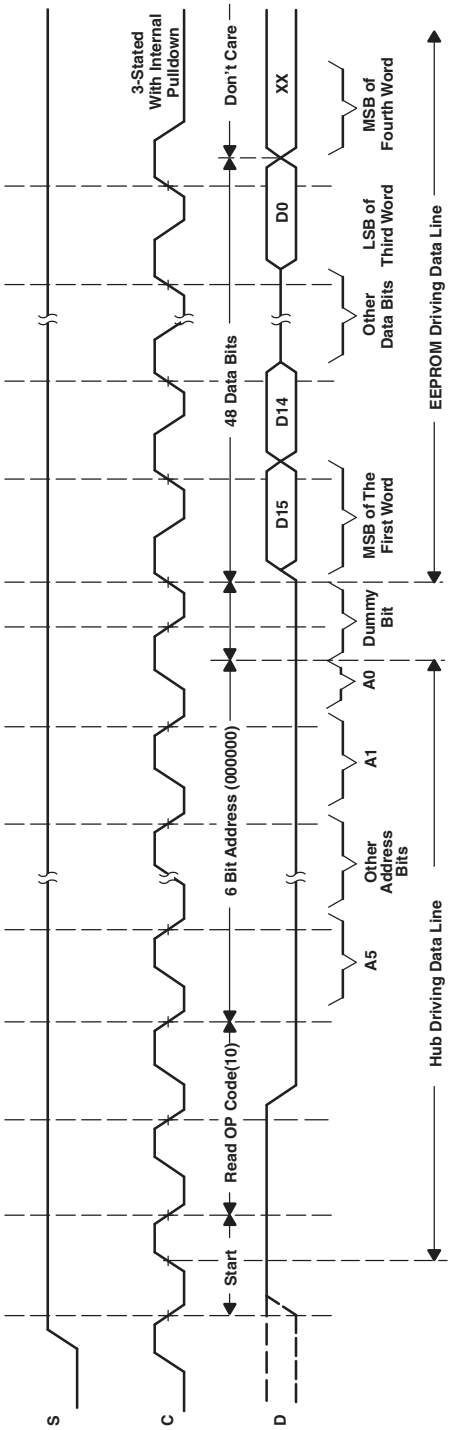


Figure 7. EEPROM Read Operation Timing Diagram

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

A major advantage of USB is the ability to connect 127 functions configured in up to 6 logical layers (tiers) to a single personal computer.

Another advantage of USB is that all peripherals are connected using a standardized four-wire cable that provides both communication and power distribution. The power configurations are bus-powered and self-powered modes. The maximum current that may be drawn from the USB 5-V line during power up is 100 mA. For the bus-powered mode, a hub can draw a maximum of 500 mA from the 5-V line of the USB cable. A bus-powered hub must always be connected downstream to a self-powered hub unless it is the only hub connected to the PC and there are no high-powered functions connected downstream. In the self-powered mode, the hub is connected to an external power supply and can supply up to 500 mA to each downstream port. High-powered functions may draw a maximum of 500 mA from each downstream port and may only be connected downstream to self-powered hubs. Per the USB specification, in the bus-powered mode, each downstream port can provide a maximum of 100 mA of current, and in the self-powered mode, each downstream port can provide a maximum of 500 mA of current.

Both bus-powered and self-powered hubs require overcurrent protection for all downstream ports. The two types of protection are individual-port management (individual-port basis) or ganged-port management (multiple-port basis). Individual-port management requires power-management devices for each individual downstream port, but adds robustness to the USB system because, in the event of an overcurrent condition, the USB host only powers down the port that has the condition. The ganged configuration uses fewer power management devices and thus has lower system costs, but in the event of an overcurrent condition on any of the downstream ports, all the ganged ports are disabled by the USB host.

Using a combination of the $\overline{\text{BUSPWR}}$ and EEDATA/$\overline{\text{GANGED}}$ inputs, the TUSB2036 supports four modes of power management: bus-powered hub with either individual-port power management or ganged-port power management, and the self-powered hub with either individual-port power management or ganged-port power management. Texas Instruments supplies the complete hub solution because we offer this TUSB2036 along with the power-management devices needed to implement a fully USB compliant system.

Note, even though no resistors are shown in the following applications, pullup, pulldown, and series resistors must be used to properly implement this device.

9.2 Typical Application

A common application for the TUSB2036 is as a self-powered USB hub product. The product is powered by an external 5-V DC Power adapter. In this application, using a USB cable TUSB2036's upstream port is plugged into a USB Host controller. The downstream ports of the TUSB2036 are exposed to users for connecting USB cameras, keyboards, printers, and so forth.

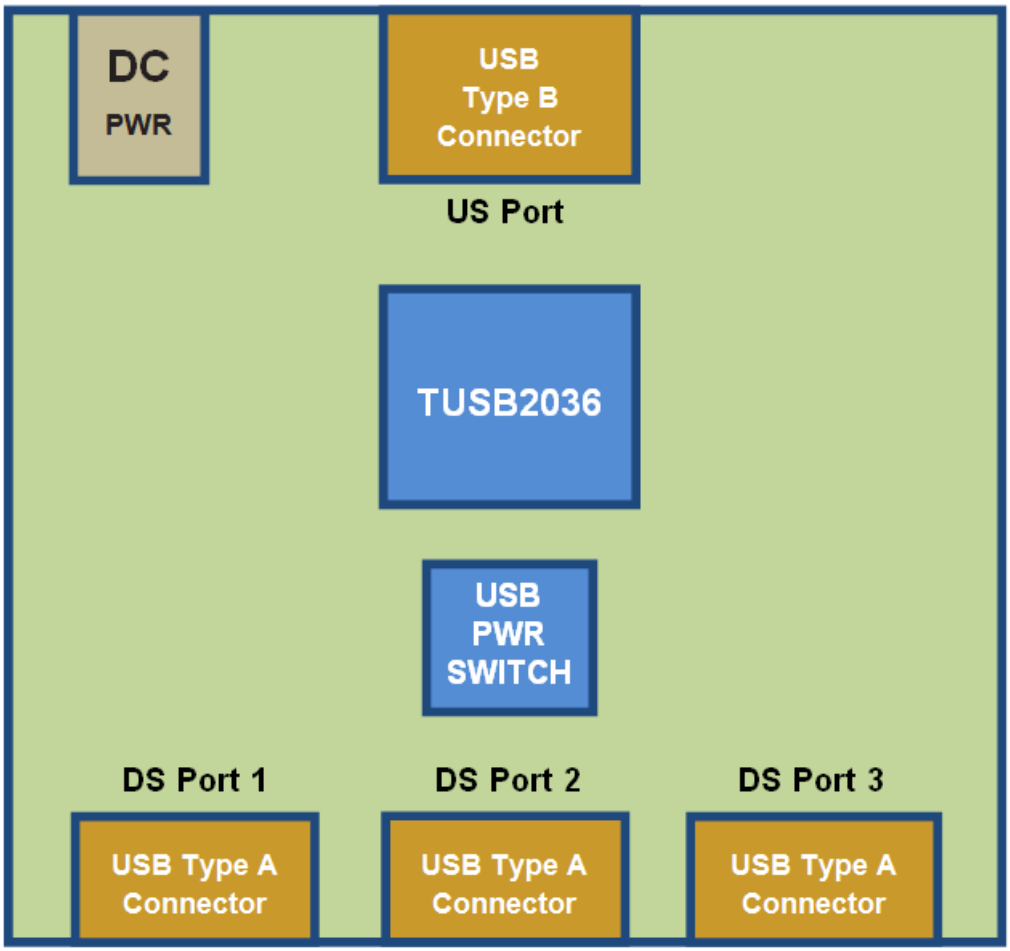


Figure 8. Self-Powered USB Hub Product

9.2.1 Design Requirements

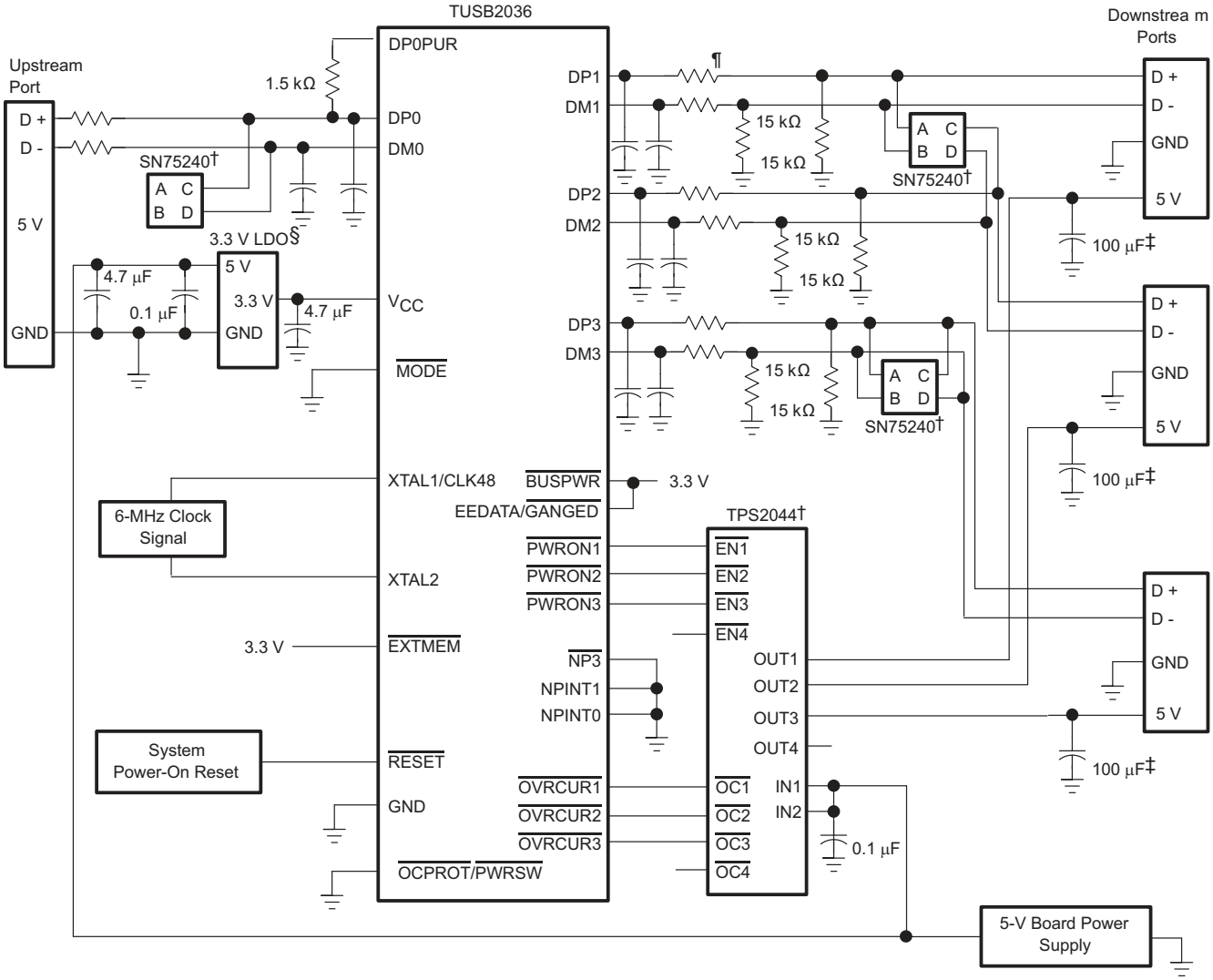
For this example, follow the design parameters listed in Table 3.

Table 3. Design Parameters

DESIGN PARAMETERS	EXAMPLE VALUE
VCC Supply	3.3 V
Downstream Ports	3
Power Management	Individual- Port
Clock Source	6-MHz Crystal
External EEPROM	No
Power Source Mode	Self-Powered

9.2.2 Detailed Design Procedure

In a self-powered configuration, the TUSB2036 can be implemented for individual-port power management when used with the TPS2044 because it is capable of supplying 500 mA of current to each downstream port and can provide current limiting on a per-port basis. When the hub detects a fault on a downstream port, power is removed from only the port with the fault and the remaining ports continue to operate normally. Self-powered hubs are required to implement overcurrent protection and report overcurrent conditions. The SN75240 transient suppressors reduce inrush current and voltage spikes on the data lines.



NOTES: † TPS2042 and SN75240 are Texas Instruments devices. Two TPS2042 devices can be substituted for the TPS2044.
‡ 120 µF per hub is the minimum required per the USB specification. However, TI recommends a 100-µF, low ESR, tantalum capacitor per port for immunity to voltage droop.
§ LDO is a 5-V-to-3.3-V voltage regulator. TPS76333 from Texas Instruments can be used.
¶ All USB DP, DM signal pairs require series resistors of approximately 27Ω to ensure proper termination. An optional filter capacitor of about 22 pF is recommended for EMI suppression. This capacitor, if used, must be placed between the hub terminal and the series resistor, as per section 7.1.6 of the USB specification.

Figure 9. TUSB2036 Self-Powered Hub, Individual-Port Power-Management Application

9.2.3 Application Curve

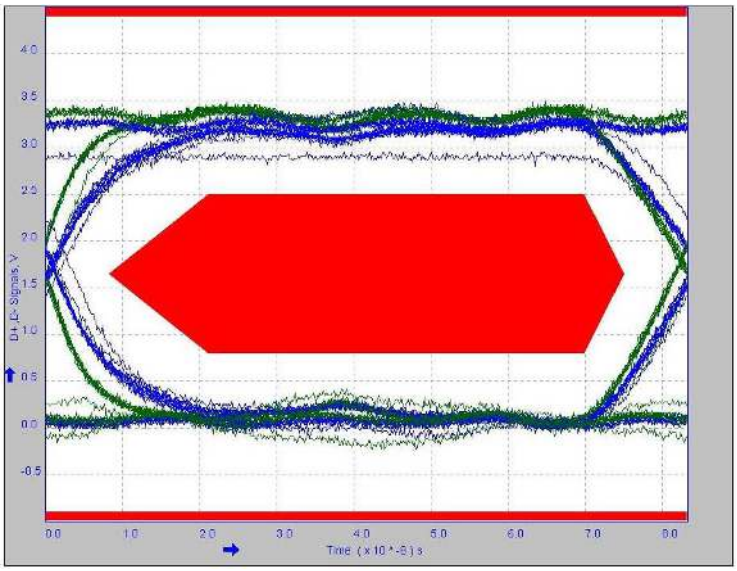


Figure 10. Downstream Port 1

10 Power Supply Recommendations

10.1 TUSB2036 Power Supply

V_{CC} should be implemented as a single power plane.

- The V_{CC} pins of the TUSB2036 supply 3.3-V power rail to the I/O of the TUSB2036. This power rail can be isolated from all other power rails by a ferrite bead to reduce noise.
- All power rails require a 10-μF capacitor or 1-μF capacitors for stability and noise immunity. These bulk capacitors can be placed anywhere on the power rail. The smaller decoupling capacitors should be placed as close to the TUSB2036 power pins as possible with an optimal grouping of two of differing values per pin.

10.2 Downstream Port Power

- The downstream port power, VBUS, must be supplied by a source capable of supplying 5 V and up to 500 mA per port. Downstream port power switches can be controlled by the TUSB2036 signals. It is also possible to leave the downstream port power always enabled.
- A large bulk low-ESR capacitor of 22 μF or larger is required on each downstream port's VBUS to limit in-rush current.
- The ferrite beads on the VBUS pins of the downstream USB port connections are recommended for both ESD and EMI reasons. A 0.1 μF capacitor on the USB connector side of the ferrite provides a low impedance path to ground for fast rise time ESD current that might have coupled onto the VBUS trace from the cable.

11 Layout

11.1 Layout Guidelines

11.1.1 Placement

1. A 0.1 μF should be placed as close as possible on VCC power pin.
2. The ESD and EMI protection devices (if used) should also be placed as possible to the USB connector.
3. If a crystal is used, it must be placed as close as possible to the TUSB2036's XTAL1 and XTAL2 pins.
4. Place voltage regulators as far away as possible from the TUSB2036, the crystal, and the differential pairs.
5. 5. In general, the large bulk capacitors associated with the power rail should be placed as close as possible to the voltage regulators.

11.1.2 Differential Pairs

1. Must be designed with a differential impedance of 90 Ω ±10%.
2. Route all differential pairs on the same layer adjacent to a solid ground plane.
3. Do not route differential pairs over any plane split.
4. Adding test points will cause impedance discontinuity and will therefore negative impact signal performance. If test points are used, they should be placed in series and symmetrically. They must not be placed in a manner that causes stub on the differential pair.
5. Avoid 90 degree turns in trace. The use of bends in differential traces should be kept to a minimum. When bends are used, the number of left and right bends should be as equal as possible and the angle of the bend should be ≥ 135 degrees. This will minimize any length mismatch causes by the bends and therefore minimize the impact bends have on EMI.
6. Minimize the trace lengths of the differential pair traces. The maximum recommended trace length for USB 2.0 differential pair signals is eight inches. Longer trace lengths require very careful routing to assure proper signal integrity.
7. Match the etch lengths of the differential pair traces. The USB 2.0 differential pairs should not exceed 50 mils relative trace length difference.
8. Minimize the use of vias in the differential pair paths as much as possible. If this is not practical, make sure that the same via type and placement are used for both signals in a pair. Any vias used should be placed as close as possible to the TUSB2036 device.
9. Do not place power fuses across the differential pair traces.

Layout Guidelines (continued)

11.1.3 Ground

It is recommended that only one board ground plane be used in the design. This provides the best image plane for signal traces running above the plane. The thermal pad of the TUSB2036 and any of the voltage regulators should be connected to this plane with vias. An earth or chassis ground is implemented only near the USB port connectors on a different plane for EMI and ESD purposes.

11.2 Layout Example

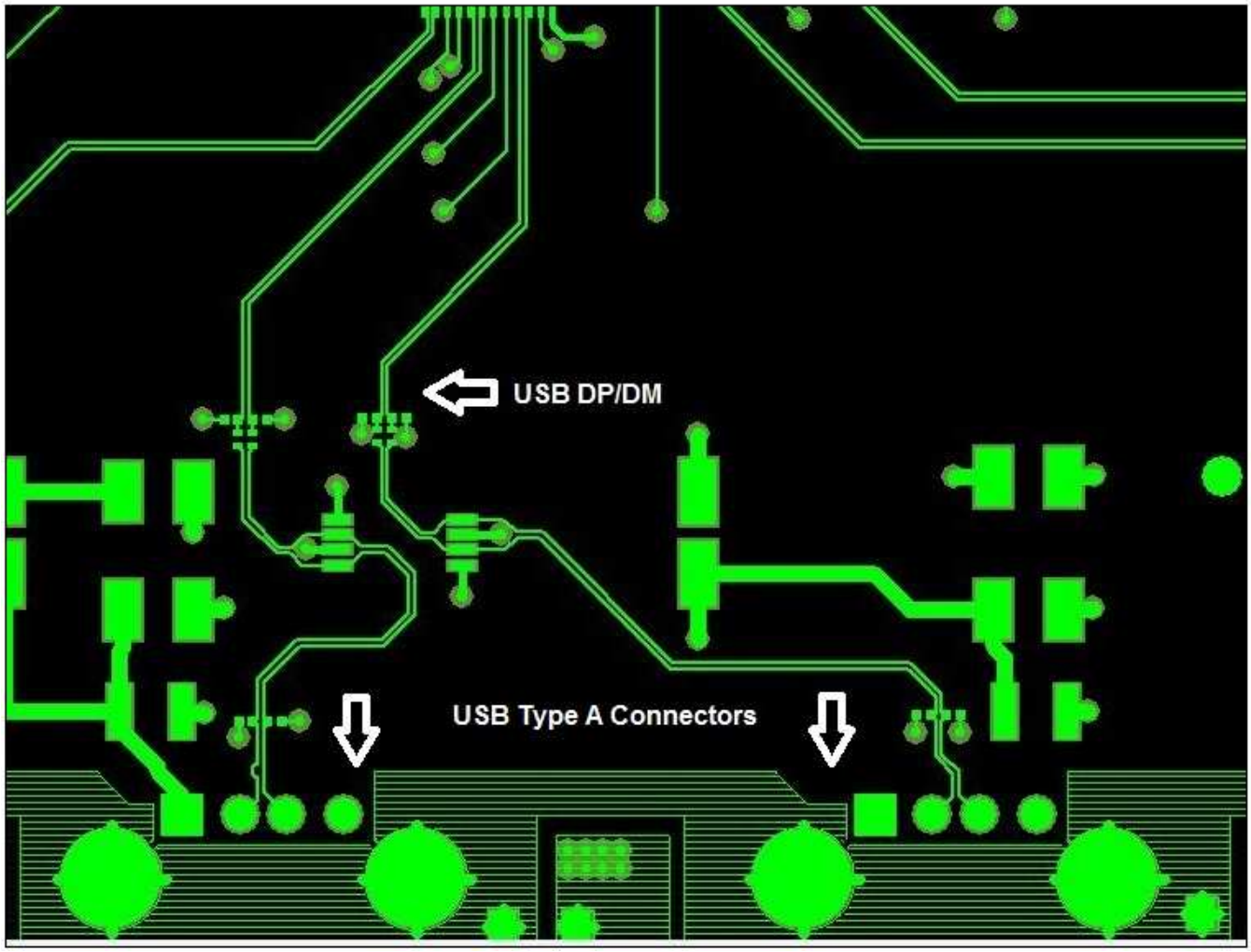


Figure 11. Downstream Ports

12 Device and Documentation Support

12.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised docum

12.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.3 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TUSB2036VF	ACTIVE	LQFP	VF	32	250	RoHS & Green	NIPDAU	Level-3-260C-168 HR	0 to 70	TUSB2036	Samples
TUSB2036VFG4	ACTIVE	LQFP	VF	32	250	RoHS & Green	NIPDAU	Level-3-260C-168 HR	0 to 70	TUSB2036	Samples
TUSB2036VFR	ACTIVE	LQFP	VF	32	1000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	0 to 70	TUSB2036	Samples
TUSB2036VFRG4	ACTIVE	LQFP	VF	32	1000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	0 to 70	TUSB2036	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

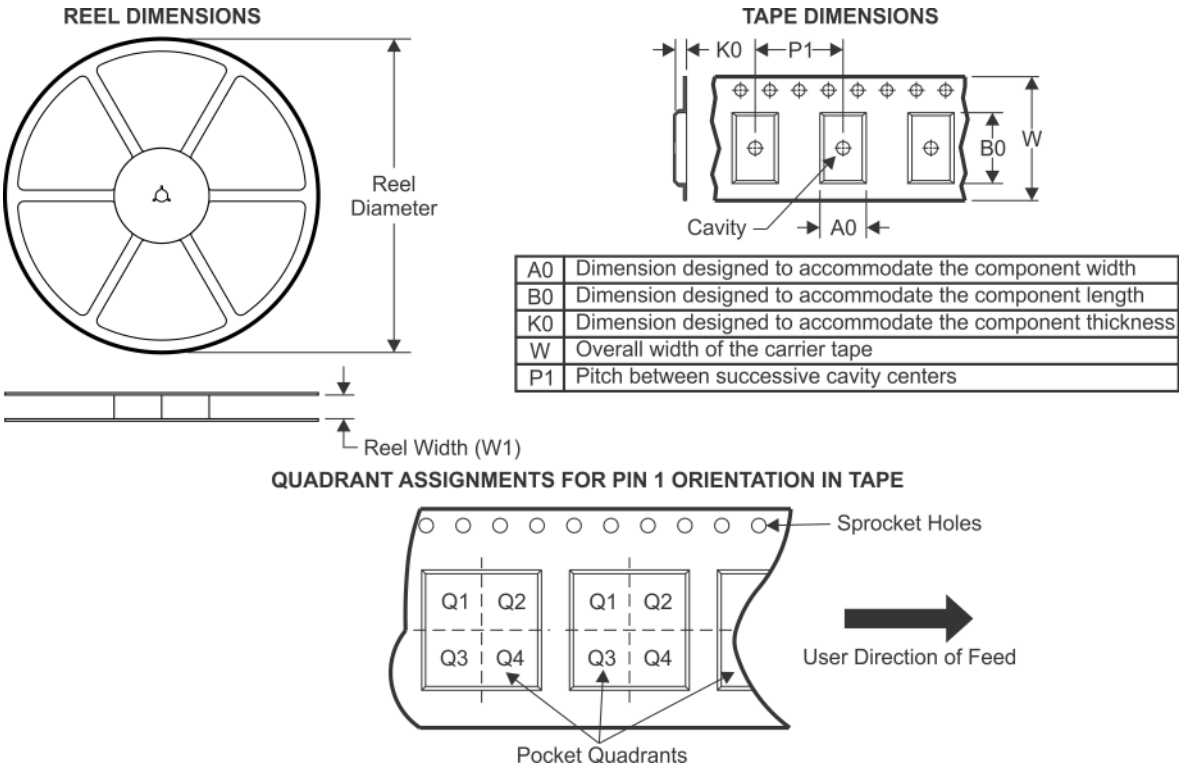
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals.
TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

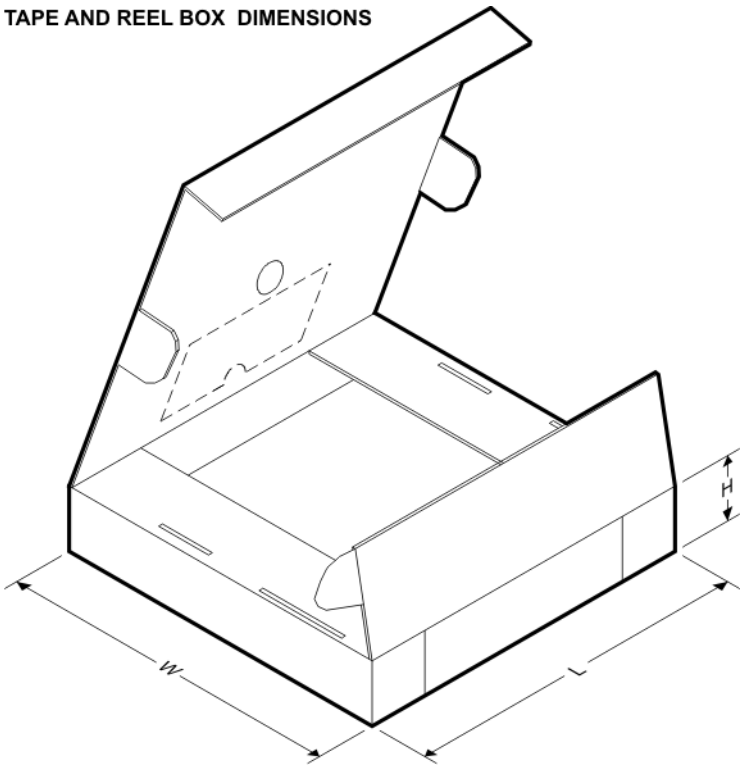


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TUSB2036VFR	LQFP	VF	32	1000	330.0	16.4	9.6	9.6	1.9	12.0	16.0	Q2

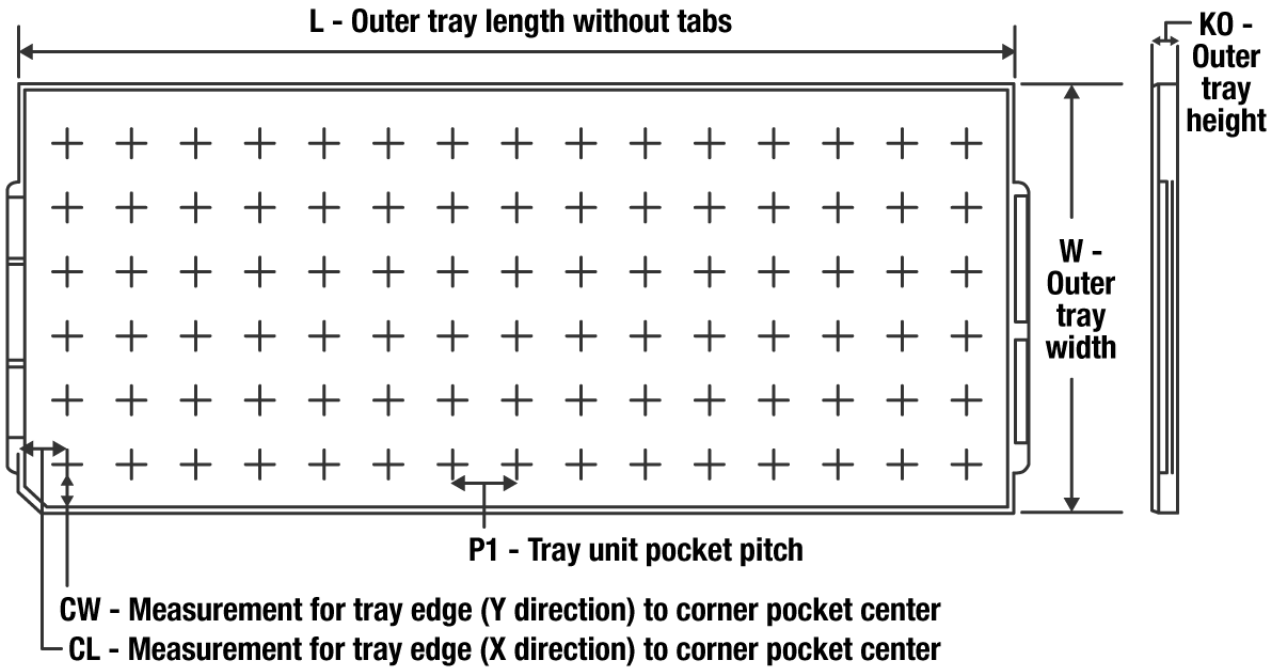
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TUSB2036VFR	LQFP	VF	32	1000	336.6	336.6	31.8

TRAY



Chamfer on Tray corner indicates Pin 1 orientation of packed units.

*All dimensions are nominal

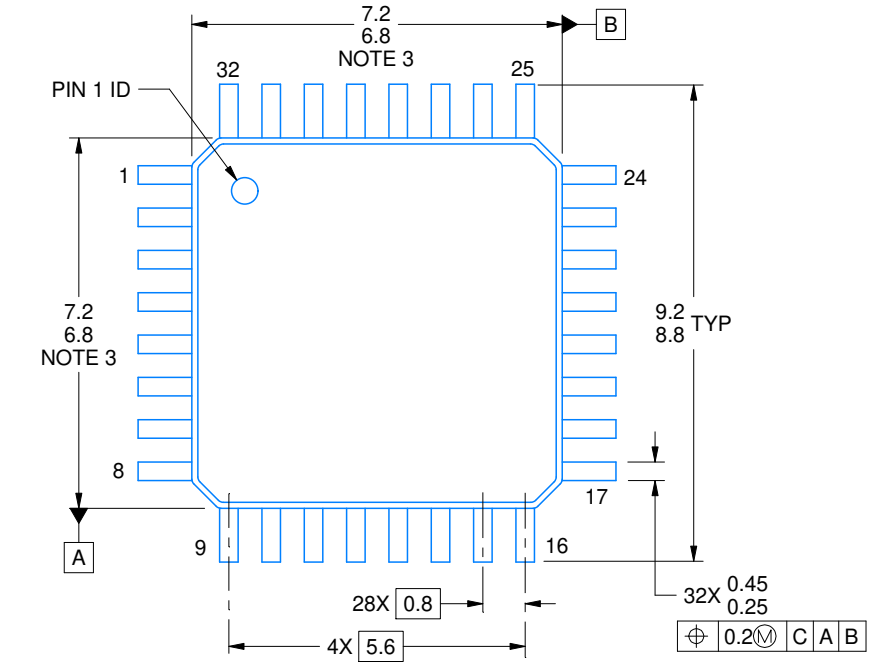
Device	Package Name	Package Type	Pins	SPQ	Unit array matrix	Max temperature (°C)	L (mm)	W (mm)	K0 (µm)	P1 (mm)	CL (mm)	CW (mm)
TUSB2036VF	VF	LQFP	32	250	10 x 25	150	315	135.9	7620	12.2	11.1	11.25
TUSB2036VFG4	VF	LQFP	32	250	10 x 25	150	315	135.9	7620	12.2	11.1	11.25

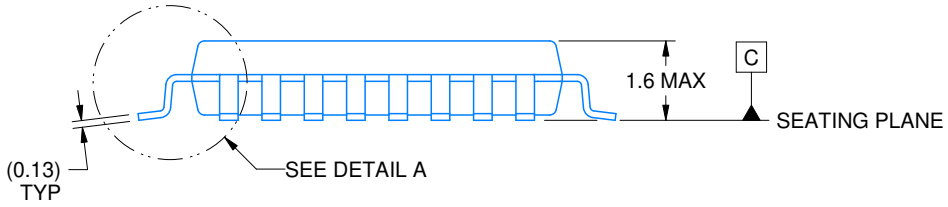
PACKAGE OUTLINE

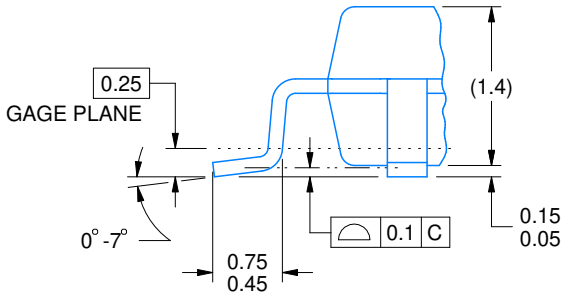
VF0032A

LQFP - 1.6 mm max height

PLASTIC QUAD FLATPACK







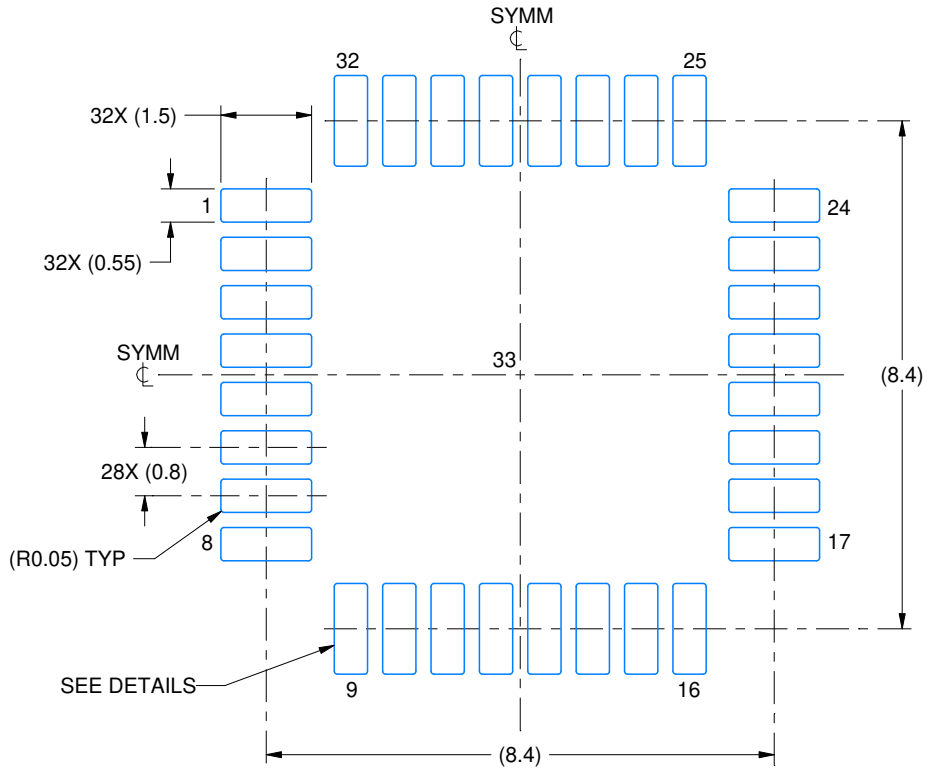
DETAIL A
TYPICAL

4219769/A 04/2019

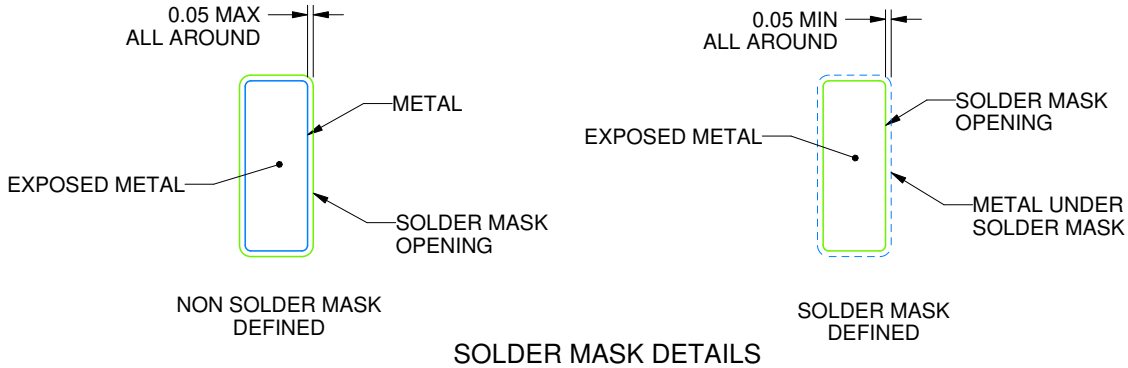
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs.
4. Reference JEDEC registration MS-026.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

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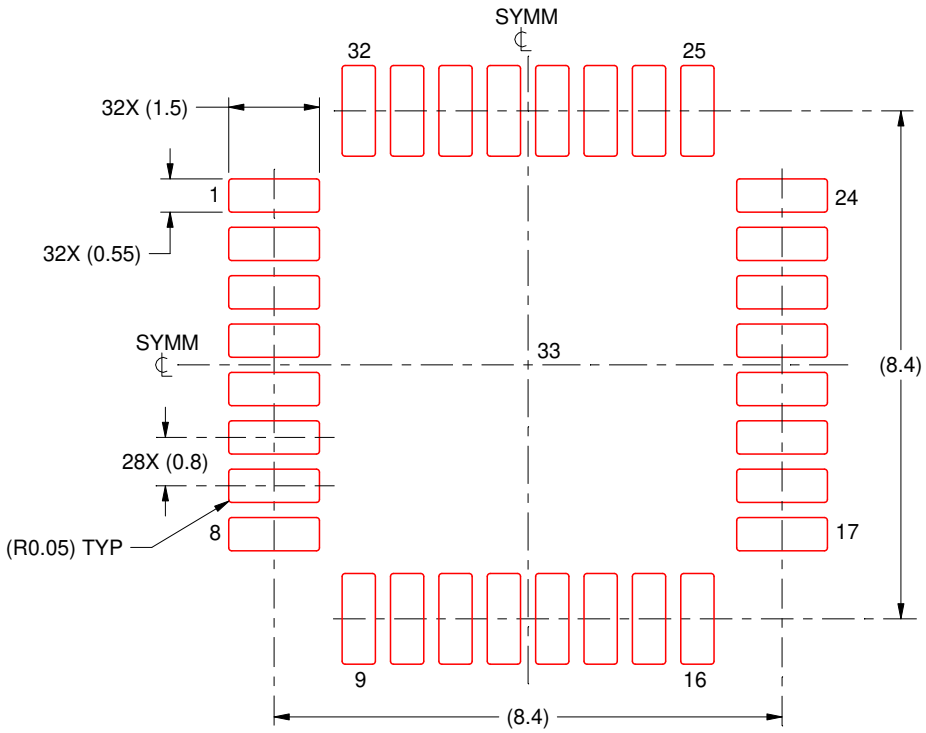
NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
SCALE:8X

4219769/A 04/2019

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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