CYPRESS

CY7C332

Registered Combinatorial EPLD

Features

- 12 I/O macrocells each having:
  - Registered, latched, or transparent array input
  - A choice of two clock sources
  - Global or local output enable (OE)
  - Up to 19 product terms (PTs) per output
  - Product term (PT) output polarity control
- 192 product terms with variable distribution to macrocells
  - An average of 14 PTs per macrocell sum node
- Two clock inputs with configurable polarity control
- 13 input macrocells, each having:
  - Complementary input
  - Register, latch, or transparent access
  - Two clock sources
- 15 ns t_{PD} max.
- Low power
  - 120 mA typical I_{CC} quiescent
  - 180 mA max.
  - Power-saving "Miser Bit" feature
- Security fuse
- 28-pin slim-line package; also available in 28-pin PLCC
- UV-erasable and reprogrammable
- Programming and operation 100% testable

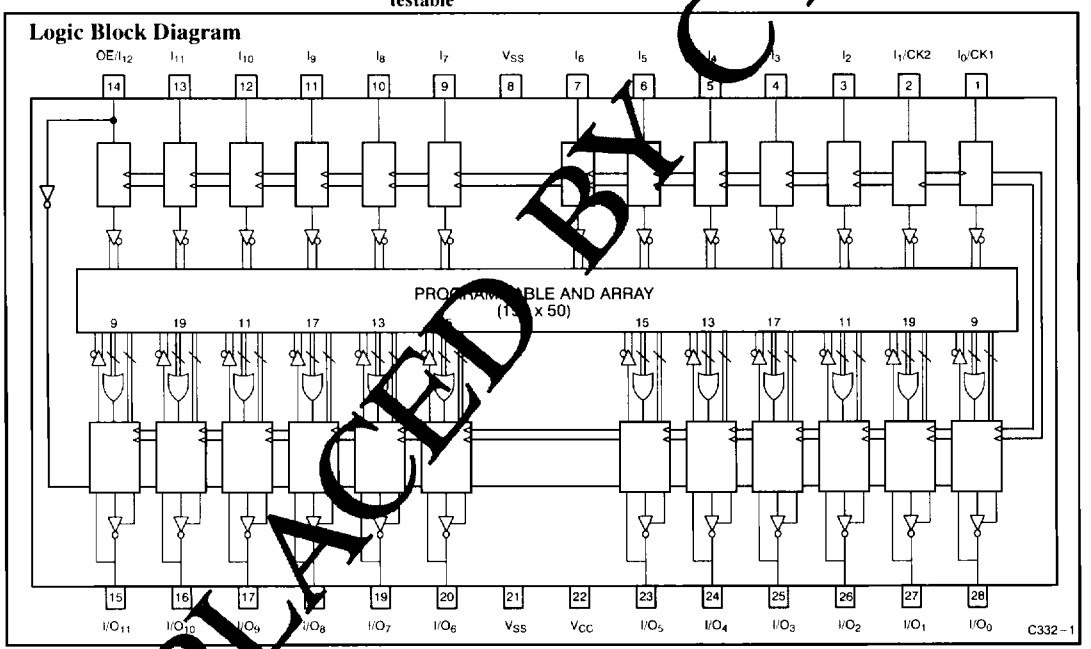
Functional Description

The CY7C332 is a versatile combinatorial PLD with I/O registers on-board. There are 25 array inputs; each has a macrocell that may be configured as a register, latch, or simple buffer. Outputs have polarity and three-state control product terms. The allocation of product terms to I/O macrocells is varied so that functions of up to 19 product terms can be accommodated.

I/O Resources

Pins 1 through 7 and 9 through 14 function as dedicated array inputs. Pins 1 and 2 function as input clocks as well as normal inputs. Pin 14 functions as a global output enable as well as a normal input.

Logic Block Diagram



Selection Guide

Generic Part Number	I_{CC1} (mA)		t_{ICO}/t_{PD} (ns)		t_{IS} (ns)	
	Commercial	Military	Commercial	Military	Commercial	Military
7C332-15	130		18/15		3	
7C332-20	120	160	20	23/20	3	4
7C332-25	120	150	25	25	3	4
7C332-30		150		30		4

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