

## Evaluating the ADN4620/ADN4621 3.75 kV RMS, Dual-Channel LVDS 2.5 Gigabit Isolators

### FEATURES

- ▶ Isolated ground planes (logic side and bus side)
- ▶ High speed layout supports 2.5 Gigabit operation and precision jitter measurements (<1 ps rms for random jitter)
- ▶ Convenient connections through SMA terminals
  - ▶ 1.8 V power on Side 1 ( $V_{DD1}$ ) and Side 2 ( $V_{DD2}$ )
  - ▶ 3.3 V power for LVDS receivers on Side 1 ( $V_{IO1}$ ) and Side 2 ( $V_{IO2}$ , used with [ADN4621](#) only)
  - ▶ Ground on Side 1 ( $GND_1$ ) and ground on Side 2 ( $GND_2$ )
  - ▶ Side 1 LVDS signals:  $D_{IN1+}$ ,  $D_{IN1-}$ ,  $D_{IN2+}$  or  $D_{OUT2+}$ ,  $D_{IN2-}$  or  $D_{OUT2-}$
  - ▶ Side 2 LVDS signals:  $D_{OUT1+}$ ,  $D_{OUT1-}$ ,  $D_{OUT2+}$  or  $D_{IN2+}$ ,  $D_{OUT2-}$  or  $D_{IN2-}$
- ▶ Jumper-selectable refresh mode
- ▶ Termination resistors on all LVDS receivers

### EVALUATION KIT CONTENTS

- ▶ EVAL-ADN4620EBZ or EVAL-ADN4621EBZ

### DOCUMENTS NEEDED

- ▶ [ADN4620/ADN4621](#) data sheet

### EQUIPMENT NEEDED

- ▶ Signal generator
- ▶ Oscilloscope
- ▶ Power supply

### GENERAL DESCRIPTION

The EVAL-ADN4620EBZ and EVAL-ADN4621EBZ allow quick and easy evaluation of the ADN4620/ADN4621 low voltage differential signaling (LVDS) isolators without the need for external components. The ADN4620/ADN4621 employ the Analog Devices, Inc., iCoupler® technology to combine a 2-channel isolator with LVDS receivers and drivers into a single, 20-lead SSOP package. The ADN4620/ADN4621 are capable of running at data rates of up to 2.5 Gbps with low jitter.

The EVAL-ADN4620EBZ/EVAL-ADN4621EBZ have separate ground and power planes for each side of the isolator, with individual 1.8 V power supplies required on each side of the ADN4620/ADN4621. This separation enables the evaluation of the ADN4620/ADN4621 with galvanic isolation between both sides of the devices. An additional power supply providing 3.3 V is required on Side 1 (and also Side 2 for the ADN4621).

For full details on the ADN4620/ADN4621, see the ADN4620/ADN4621 data sheet, which must be consulted in conjunction

with this user guide when using the EVAL-ADN4620EBZ or EVAL-ADN4621EBZ.

### EVALUATION BOARD PHOTOGRAPHS

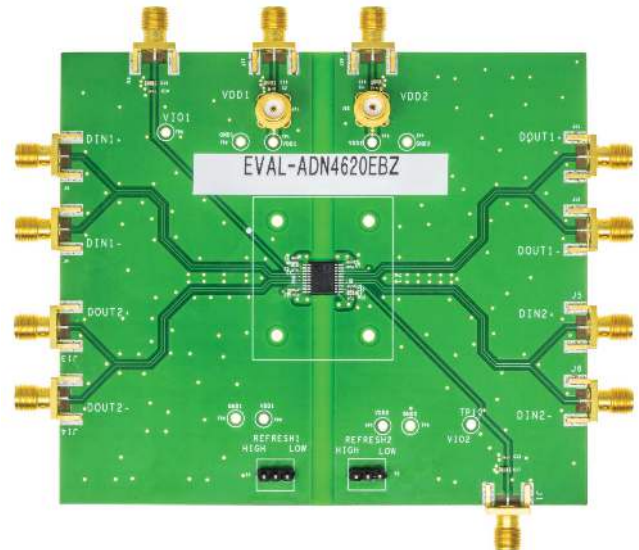


Figure 1. EVAL-ADN4620EBZ Photograph

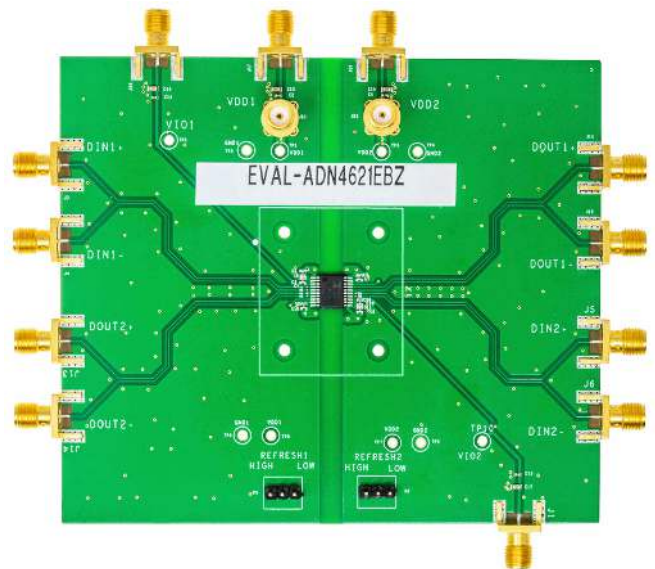


Figure 2. EVAL-ADN4621EBZ Photograph

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**REVISION HISTORY****6/2022—Revision 0: Initial Version**

EVALUATION BOARD CONFIGURATION

SETTING UP THE EVALUATION BOARD

On the EVAL-ADN4620EBZ or EVAL-ADN4621EBZ, connect a 3.3 V power supply to the J18 subminiature Version A (SMA) connector and connect 1.8 V power supplies to the J17 or J21 SMA connectors for Side 1 and the J19 or J22 SMA connectors for Side 2 (see Table 2). For the EVAL-ADN4621EBZ, also connect another 3.3 V power supply to the J1 SMA connector. At 1.25 GHz, with a load resistance of 100 Ω, the maximum operating current is 80 mA from each 1.8 V power supply, 14 mA from the 3.3 V supply on Side 1, and 7 mA from the 3.3 V supply on Side 2.

V<sub>DD1</sub> (Pin 1 and Pin 10 on the ADN4620/ADN4621) is bypassed to GND<sub>1</sub> and V<sub>DD2</sub> (Pin 11 and Pin 20 on the ADN4620/ADN4621) is bypassed to GND<sub>2</sub>. Similarly, V<sub>IO1</sub> (Pin 3 on the ADN4620/ADN4621) is bypassed to GND<sub>1</sub> and V<sub>IO2</sub> (Pin 13 on the ADN4621 only) is bypassed to GND<sub>2</sub>. Bypass capacitors of 0.1 μF are used in all cases.

The ADN4620/ADN4621 integrates a refresh function to correct, if necessary, the output state in the absence of any input transitions. This function ensures the correct output state at power-up, for example. To reduce internal switching noise and provide even lower jitter, the refresh function can be disabled. This functionality is accessed on the EVAL-ADN4620EBZ or EVAL-ADN4621EBZ by changing the position of the P1 and P2 jumpers for Side 1 and Side 2, respectively, as described in Table 1.

Figure 4 shows an example operation of the EVAL-ADN4621EBZ. The EVAL-ADN4620EBZ is set up similarly with the exception of no connection to J1. The SMA connectors reveal all LVDS inputs and outputs for the EVAL-ADN4620EBZ or EVAL-ADN4621EBZ (see

Table 3). To evaluate Channel 1 on the EVAL-ADN4620EBZ or EVAL-ADN4621EBZ, connect a signal generator to the evaluation board using the J3 connector and J4 connector and set up a 1.25 GHz square wave clock with an amplitude of 200 mV (400 mV peak-to-peak) and an offset of 1.2 V. Connect the oscilloscope to the J11 connector and J12 connector to perform timing measurements, including propagation delay, skew, and jitter. A differential probe with an SMA connector is recommended, terminating each output trace to 50 Ω connected to 1.24 V (providing 100 Ω differential termination and matching the ADN4620/ADN4621 driver offset voltage (V<sub>OS</sub>)). Refer to Table 3 for the connectors to use to evaluate Channel 2 on the EVAL-ADN4620EBZ or EVAL-ADN4621EBZ.

Figure 3 shows a plot of the oscilloscope connected via the J11 connector and J12 connector. The oscilloscope shows the differential voltage, that is, D<sub>OUT1+</sub> - D<sub>OUT1-</sub>.



Figure 3. D<sub>OUT1-</sub> and D<sub>OUT1+</sub> with a 1.25 GHz Clock, Differential

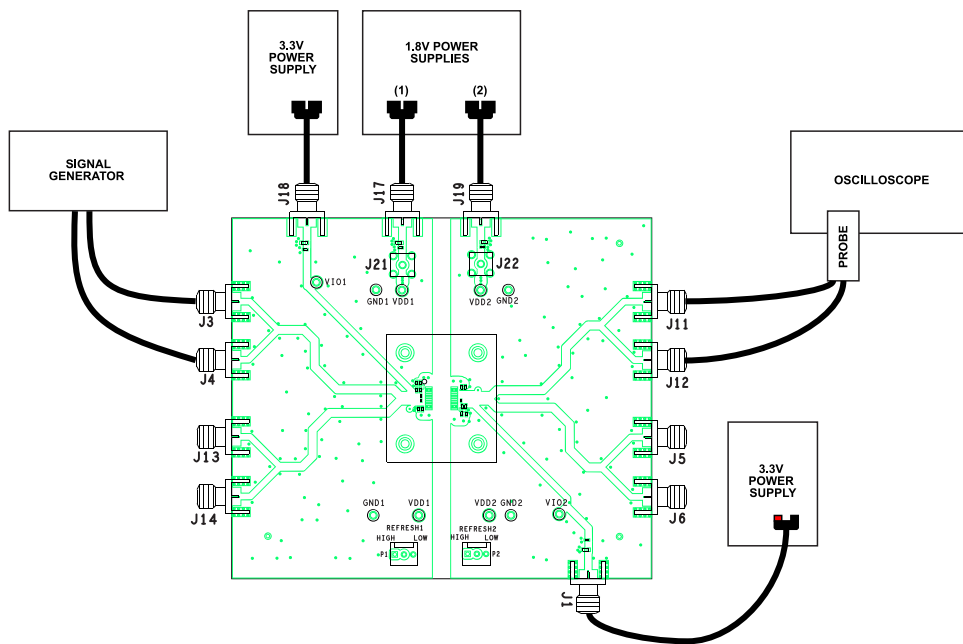


Figure 4. Basic LVDS Isolator Evaluation Board Operation for the EVAL-ADN4621EBZ

## EVALUATION BOARD CONFIGURATION

**Table 1. Jumper Configuration for EVAL-ADN4620EBZ and EVAL-ADN4621EBZ**

Jumper	Position	Description
P1	1 and 2	Side 1 refresh disabled (quiet operation): $\overline{\text{REFRESH}}_1$ shorted to $V_{DD1}$ .
	2 and 3	Side 1 refresh enabled (normal operation): $\text{REFRESH}_1$ shorted to $\text{GND}_1$ .
P2	1 and 2	Side 2 refresh disabled (quiet operation): $\overline{\text{REFRESH}}_2$ shorted to $V_{DD2}$ .
	2 and 3	Side 2 refresh enabled (normal operation): $\text{REFRESH}_2$ shorted to $\text{GND}_2$ .

**Table 2. Power Supply Connector Descriptions for EVAL-ADN4620EBZ and EVAL-ADN4621EBZ**

Connector	Description
Side 1	
J17, J21	Power supply, Side 1, connect 1.8 V to one connector option
J18	Input/output power supply, Side 1, connect 3.3 V
Side 2	
J19, J22	Power supply, Side 2, connect 1.8 V to one connector option
J1	Input/output power supply, Side 2, connect 3.3 V (leave open for EVAL-ADN4620EBZ)

**Table 3. Input and Output Connector Descriptions for EVAL-ADN4620EBZ**

Connector	EVAL-ADN4620EBZ Description
J3	$D_{IN1+}$ , noninverted LVDS input for Channel 1
J4	$D_{IN1-}$ , inverted LVDS input for Channel 1
J13	$D_{IN2+}$ , noninverted LVDS input for Channel 2
J14	$D_{IN2-}$ , inverted LVDS input for Channel 2
J11	$D_{OUT1+}$ , noninverted LVDS output for Channel 1
J12	$D_{OUT1-}$ , inverted LVDS output for Channel 1
J5	$D_{OUT2+}$ , noninverted LVDS output for Channel 2
J6	$D_{OUT2-}$ , inverted LVDS output for Channel 2

**Table 4. Input and Output Connector Descriptions for EVAL-ADN4621EBZ**

Connector	EVAL-ADN4621EBZ Description
J3	$D_{IN1+}$ , noninverted LVDS input for Channel 1
J4	$D_{IN1-}$ , inverted LVDS input for Channel 1
J13	$D_{OUT2+}$ , noninverted LVDS output for Channel 2
J14	$D_{OUT2-}$ , inverted LVDS output for Channel 2
J11	$D_{OUT1+}$ , noninverted LVDS output for Channel 1
J12	$D_{OUT1-}$ , inverted LVDS output for Channel 1
J5	$D_{IN2+}$ , noninverted LVDS input for Channel 2
J6	$D_{IN2-}$ , inverted LVDS input for Channel 2

EVALUATION BOARD SCHEMATICS AND ARTWORK

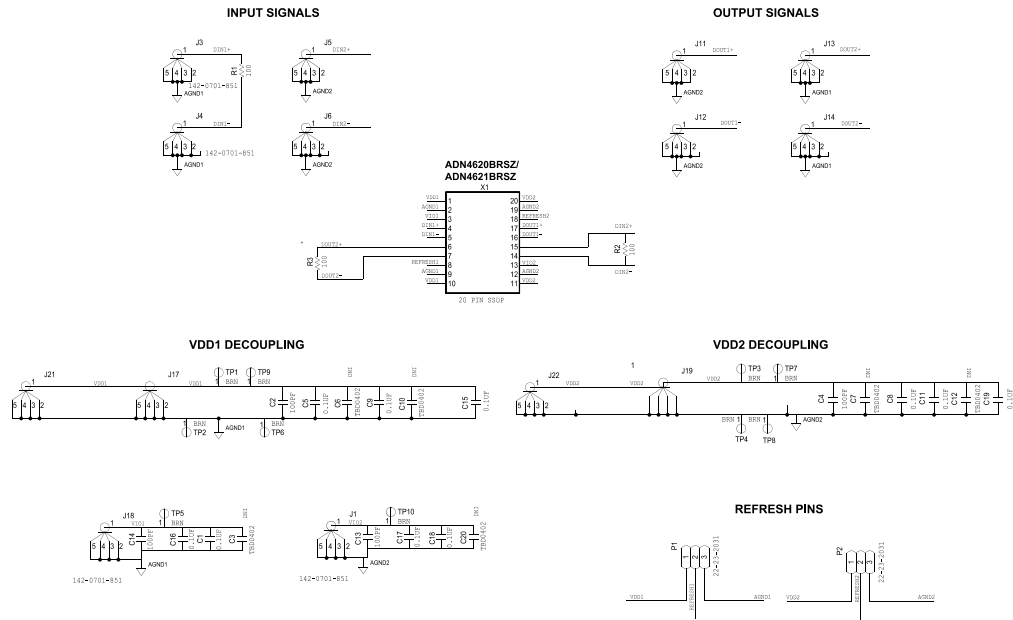


Figure 5. EVAL-ADN4620EBZ and EVAL-ADN4621EBZ Schematic

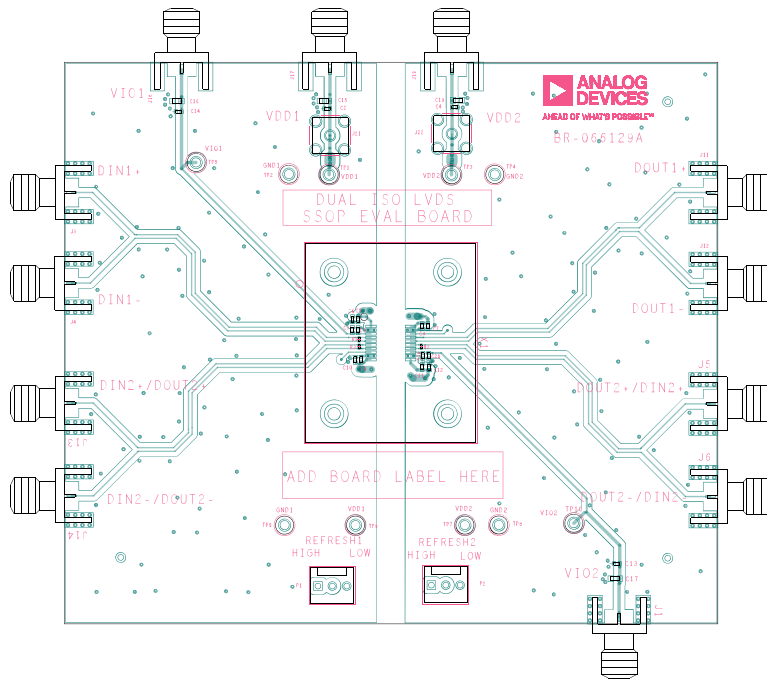


Figure 6. EVAL-ADN4620EBZ or EVAL-ADN4621EBZ Component Side and Silkscreen

EVALUATION BOARD SCHEMATICS AND ARTWORK

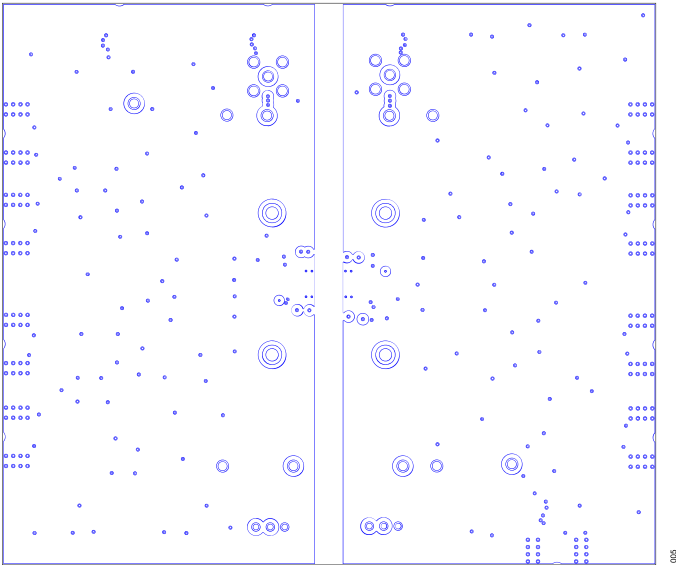


Figure 7. EVAL-ADN4620EBZ or EVAL-ADN4621EBZ Inner Layer 2, Ground

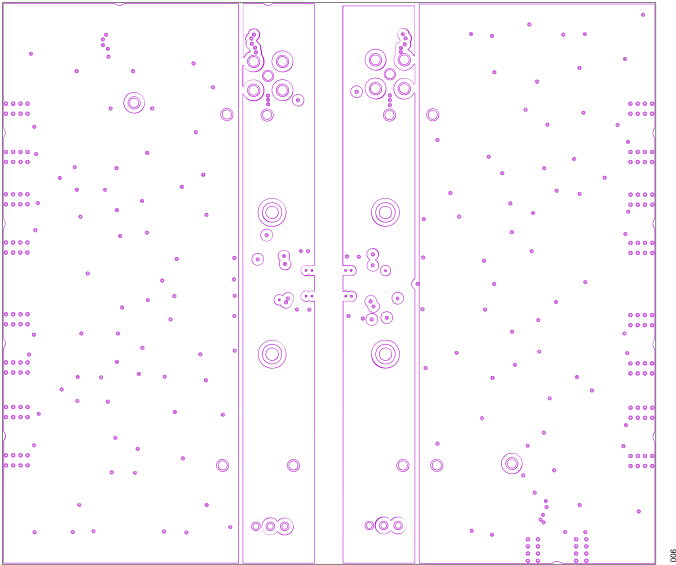


Figure 8. EVAL-ADN4620EBZ or EVAL-ADN4621EBZ Inner Layer 3, Power

EVALUATION BOARD SCHEMATICS AND ARTWORK

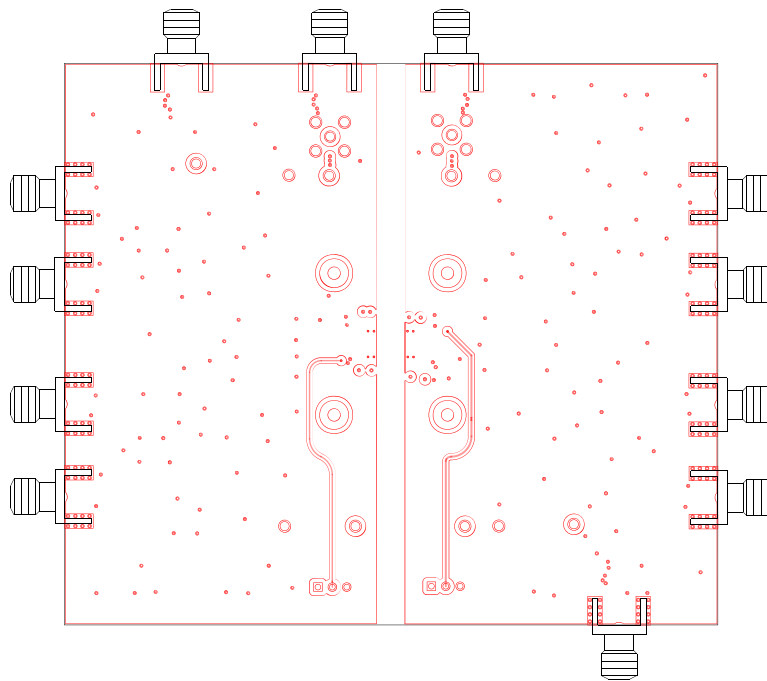


Figure 9. EVAL-ADN4620EBZ or EVAL-ADN4621EBZ Solder Side

## ORDERING INFORMATION

## BILL OF MATERIALS

Table 5. EVAL-ADN4620EBZ Bill of Materials

Quantity	Reference Designator	Description	Manufacturer	Part Number
5	C1, C5, C8, C9, C11	Capacitors, 0.1 $\mu$ F, 0402	Kemet	C0402C104K4RACTU
3	C2, C4, C14	Capacitors, 100 pF, 0402	Murata	GRM1555C1H101JA01D
8	C3, C6, C7, C10, C12, C13, C18, C20	Capacitors, 0402	Not fitted	Not applicable
3	C15, C16, C19	Capacitors, 0.1 $\mu$ F, 0603	AVX	06035C104KAT2A
1	C17	Capacitor, 0603	Not fitted	Not applicable
1	J1	Connector, SMA, edge	Not fitted	Not applicable
11	J3 to J6, J11 to J14, J17 to J19	Connectors, SMA, edge	Johnson - Cinch	142-0701-851
2	J21, J22	Connectors, SMA	Pasternack Enterprises	PE4117
2	P1, P2	3-pin, header (and jumper)	Molex (and Sullins)	22-23-2031 (and QPC02SXGN-RC)
2	R1, R3	Resistors, 100 $\Omega$ , 0201	Panasonic	ERJ-1GNF1000C
1	R2	Resistor, 0201	Not fitted	Not applicable
9	TP1 to TP9	Test points	Components Corporation	TP104-01-01
1	TP10	Test point	Not fitted	Not applicable
1	X1	<a href="#">ADN4620</a> 3.75 kV rms, dual-channel LVDS, 2.5 Gigabit isolator	Analog Devices	<a href="#">ADN4620BRSZ</a>



## ORDERING INFORMATION

Table 6. EVAL-ADN4621EBZ Bill of Materials

Quantity	Reference Designator	Description	Manufacturer	Part Number
6	C1, C5, C8, C9, C11, C18	Capacitors, 0.1 $\mu$ F, 0402	Kemet	C0402C104K4RACTU
4	C2, C4, C13, C14	Capacitors, 100 pF, 0402	Murata	GRM1555C1H101JA01D
6	C3, C6, C7, C10, C12, C20	Capacitors, 0402	Not fitted	Not applicable
4	C15, C16, C17, C19	Capacitors, 0.1 $\mu$ F, 0603	AVX	06035C104KAT2A
12	J1, J3 to J6, J11 to J14, J17 to J19	Connectors, SMA, edge	Johnson - Cinch	142-0701-851
2	J21, J22	Connectors, SMA	Pasternack Enterprises	PE4117
2	P1, P2	3-pin, header (and jumper)	Molex (and Sullins)	22-23-2031 (and QPC02SXGN-RC)
2	R1, R2	Resistors, 100 $\Omega$ , 0201	Panasonic	ERJ-1GNF1000C
1	R3	Resistor, 0201	Not fitted	Not applicable
10	TP1 to TP10	Test points	Components Corporation	TP104-01-01
1	X1	<a href="#">ADN4621</a> 3.75 kV rms, dual-channel LVDS 2.5 Gb/s Gigabit isolator	Analog Devices	<a href="#">ADN4621BRSZ</a>

**ESD Caution**

**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

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