Fixed Frequency PWM Controller - in DSO-8 Package

Product highlights

- Enhanced Active Burst Mode with selectable entry and exit standby power to reach the lowest standby power <100 mW
- Digital frequency reduction for better overall system efficiency
- Fast startup achieved with cascode configuration
- Frequency jitter and soft gate driving for low EMI
- Integrated error amplifier
- Comprehensive protection with input line over voltage protection
- Pb-free lead plating, halogen-free mold compound, RoHS compliant

PG-DSO-8

Features

- Enhanced Active Burst Mode with selectable entry and exit standby power
- Digital frequency reduction for better overall system efficiency
- Fast startup achieved with cascode configuration
- DCM and CCM operation with slope compensation
- Frequency jitter and soft gate driving for low EMI
- Built-in digital soft start
- Integrated error amplifier to support direct feedback in non-isolated flyback
- Comprehensive protection with input line over voltage protection, V_{CC} over voltage, V_{CC} under voltage, overload/open loop, over temperature and Current Sense (CS) short to GND
- All protections are in auto restart mode
- Limited charging current for V_{CC} short to GND

Applications

- Auxiliary power supply for home appliances/white goods, TV, PC & server
- Blu-ray player, set-top box & LCD/LED monitor

Product validation

Fully qualified according to JEDEC for Industrial Applications

Description

The ICE5xSAG is the 5th generation of fixed frequency PWM controller optimized for off-line switch mode power supply in cascode configuration. The cascode configuration helps achieve fast startup. The frequency reduction with soft gate driving and frequency jitter operation offers lower EMI and better efficiency between light load and 50% load. The selectable entry and exit standby power ABM enables flexibility and ultra-low power consumption at standby mode with small and controllable output voltage ripple. The product has a wide operating range (10.0 ~ 25.5 V) of IC power supply and lower power consumption. The numerous protection functions with adjustable line over voltage protection support the power supply system in failure situations. All these make the 5th generation ICE5xSAG series an outstanding PWM controller for fixed frequency flyback converter in the market.

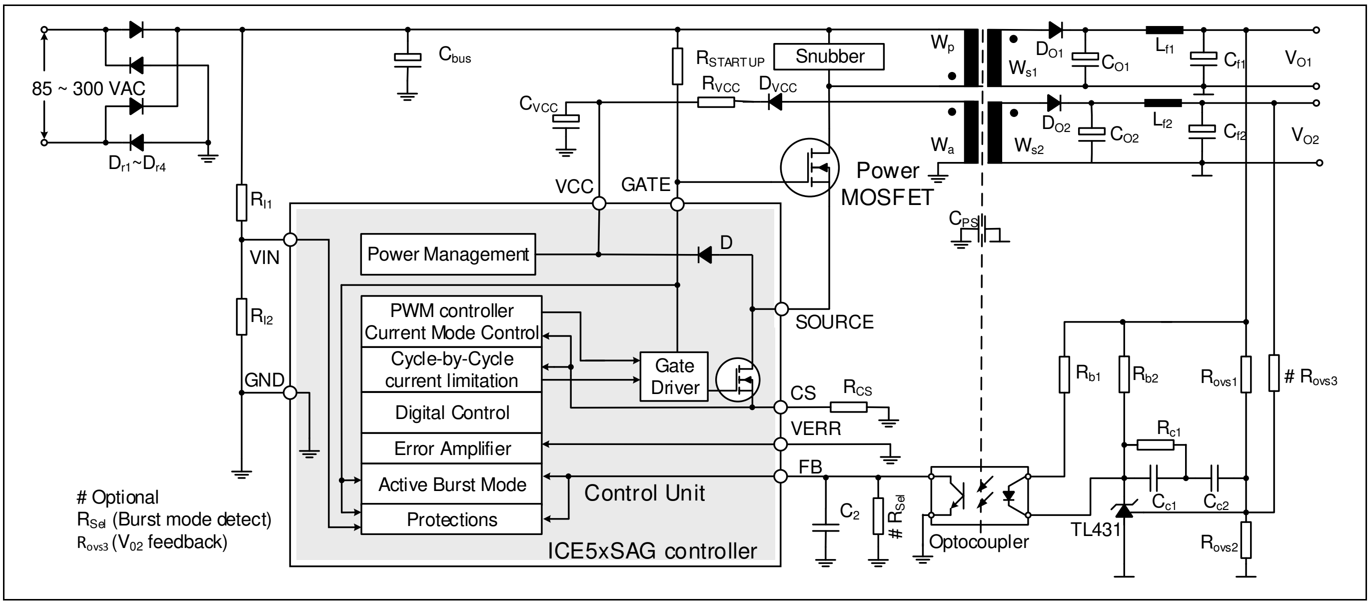

Figure 1 Typical application in isolated flyback using TL431 and optocoupler

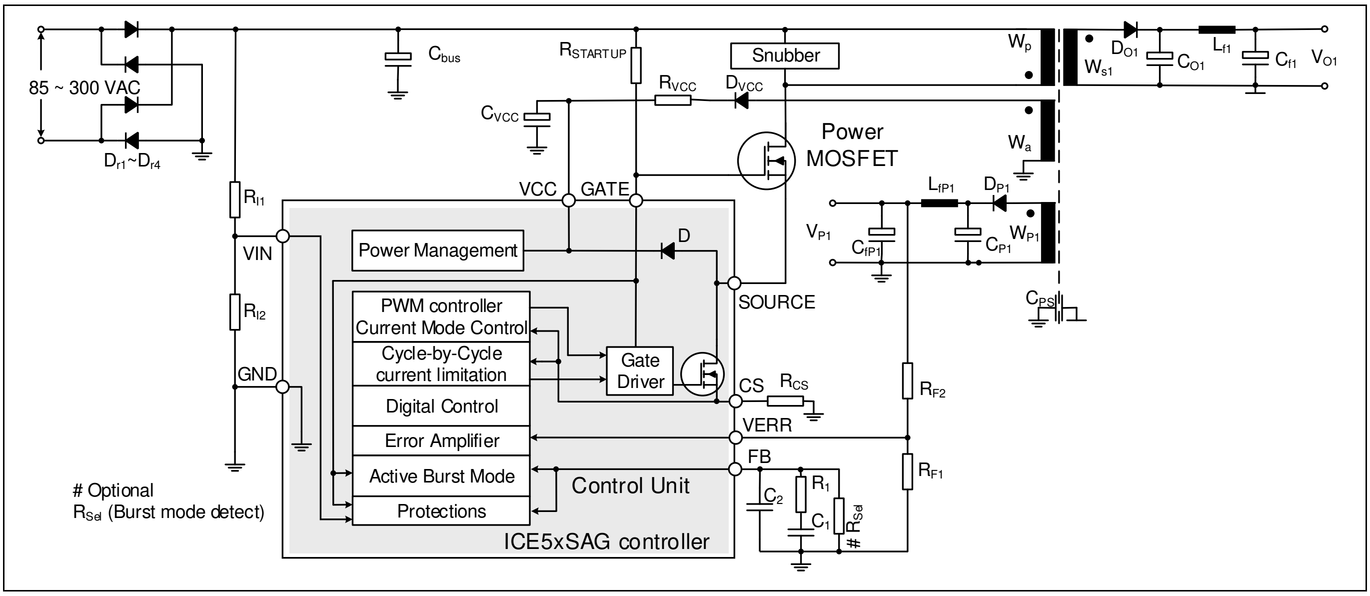

Figure 2 Typical application in non-isolated flyback utilizing integrated error amplifier

Output power of 5th generation Fixed-Frequency PWM controller

Table 1 Output power of 5th generation Fixed-Frequency PWM controller

Type	Package	Marking	Fsw	220 V AC ±20%[1] at DCM	85-300 V AC[1] at DCM	85-300 V AC[1] at CCM
ICE5ASAG	PG-DSO-8	5ASAG	100 kHz	108 W	60 W	66 W
ICE5GSAG	PG-DSO-8	5GSAG	125 kHz	108W	60 W	66 W

[1] Calculated maximum output power rating in an open frame design at T_a=50 °C, T_J=125 °C using minimum pin copper area in a 2 oz copper single sided PCB. The output power figure is for selection purpose only. The actual power can vary depending on particular designs. Please contact to a technical expert from Infineon for more information.

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1 Pin configuration and functionality

The pin configuration is shown in Figure 3 and the functions are described in Table 2.

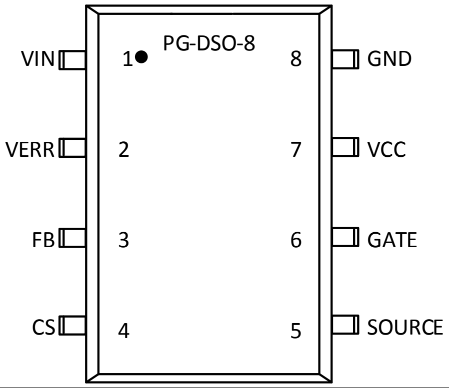


Figure 3 Pin configuration

Table 2 Pin definitions and functions

Pin	Symbol	Function
1	VIN	Input Line Over Voltage Protection (LOVP) VIN pin is connected to the bus via resistor divider (see Figure 1) to sense the line voltage. Internally, it is connected to the line over voltage comparator which will stop the switching when LOVP condition occurs. To disable LOVP, connect this pin to GND.
2	VERR	Error amplifier VERR pin is internally connected to the transconductance error amplifier for non-isolated flyback application. Connect this pin to GND for isolated flyback application.
3	FB	Feedback and ABM entry/exit control FB pin combines the functions of feedback control, selectable burst entry/exit control and overload/open loop protection.
4	CS	Current sense The CS pin is connected to the shunt resistor for the primary current sensing externally and to the PWM signal generator block for switch-off determination (together with the feedback voltage) internally. Moreover, CS short to ground protection is sensed via this pin.
5	SOURCE	SOURCE The SOURCE pin is connected to the source of external power MOSFET which is in series connection with internal low side MOSFET and internal VCC diode D.
6	GATE	Gate driver output The GATE pin is connected to the gate pin of the power MOSFET and additionally, a pull up resistor is connected from bus voltage to turn it on for charging up the V_{CC} capacitor during startup.
7	VCC	VCC(Positive voltage supply) The VCC pin is the positive voltage supply to the IC. The operating range is between V_{VCC_OFF} and V_{VCC_OVP}.
8	GND	Ground The GND pin is the common ground of the controller.

2 Representative block diagram

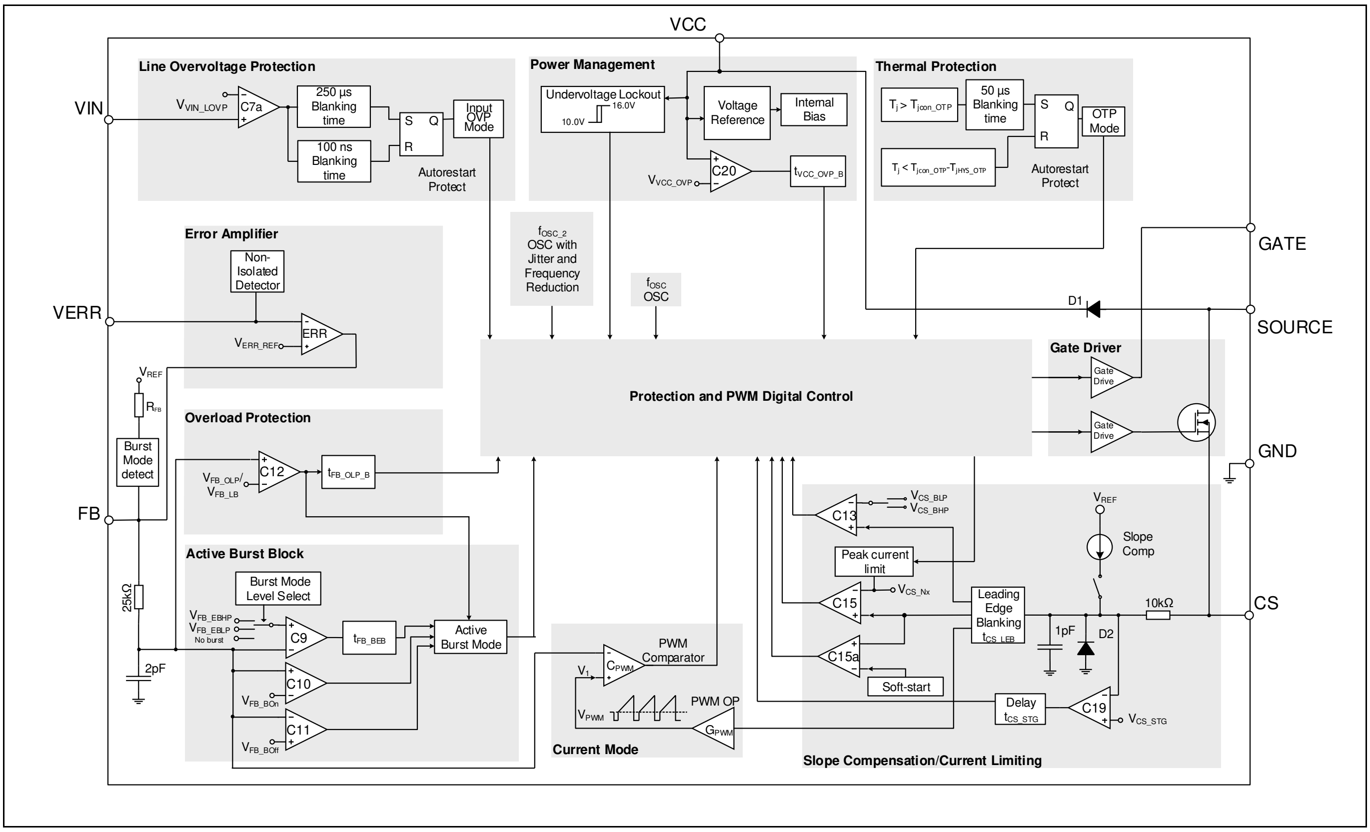


Figure 4 Representative block diagram

3 Functional description

3.1 V_{CC} pre-charging and typical V_{CC} voltage during start-up

As shown in Figure 1, once the line input voltage is applied, a rectified voltage appears across the capacitor C_{BUS}. The pull up resistor $R_{STARTUP}$ provides a current to charge the C_{iss} (input capacitance) of power MOSFET and gradually generate one voltage level. If the voltage over C_{iss} is high enough, power MOSFET turns on and V_{CC} capacitor will be charged through primary inductance of transformer L_P, power MOSFET and internal diode D_1 with two steps constant current source $I_{VCC\_Charge1}$[1] and $I_{VCC\_Charge3}$[1].

A very small constant current source ($I_{VCC\_Charge1}$) is charged to the V_{CC} capacitor till V_{CC} reach V_{CC_SCP} to protect the controller from V_{CC} pin short to ground during the start up. After this, the second step constant current source ($I_{VCC\_Charge3}$) is provided to charge the V_{CC} capacitor further, until the V_{CC} voltage exceeds the turned-on threshold V_{VCC_ON}. As shown in the time phase I in Figure 5, the V_{CC} voltage increase almost linearly with two steps.

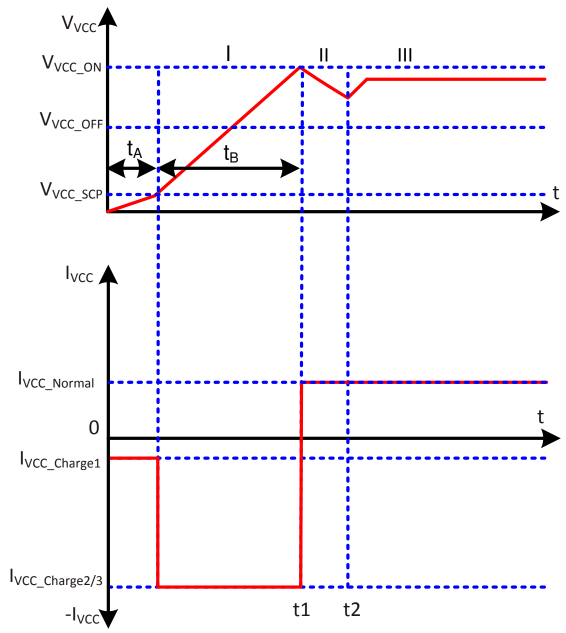


Figure 5 V_{CC} voltage and current at startup

The time taking for the V_{CC} pre-charging can then be approximately calculated as:

$$t_1 = t_A + t_B = \frac{V_{VCC\_SCP} \cdot C_{VCC}}{I_{VCC\_Charge1}} + \frac{(V_{VCC\_ON} - V_{VCC\_SCP}) \cdot C_{VCC}}{I_{VCC\_Charge3}} \quad (1)$$

When the V_{CC} voltage exceeds the V_{CC} turn on threshold V_{VCC_ON} at time t_1, the IC begins to operate with soft-start. Due to power consumption of the IC and the fact that there is still no energy from the auxiliary winding to charge the V_{CC} capacitor before the output voltage is built up, the V_{CC} voltage drops (Phase II). Once the output voltage rises close to regulation, the auxiliary winding starts to charge the V_{CC} capacitor from the time t_2 onward and delivering the I_{VCC_Normal}[2] to the controller. The V_{CC} then will reach a constant value depending on output load.

[1] $I_{VCC\_Charge1/2/3}$ is charging current from the controller to VCC capacitor during start up

[2] I_{VCC_Normal} is supply current from VCC capacitor or auxiliary winding to the controller during normal operation

3.2 Soft-start

As shown in Figure 6, the IC begins to operate with a soft-start at time t_{on}. The switching stresses on the power MOSFET, diode and transformer are minimized during soft-start. The soft-start implemented in ICE5xSAG is a digital time-based function. The preset soft-start time is t_{SS} (12 ms) with 4 steps. If not limited by other functions, the peak voltage on CS pin will increase step by step from 0.3 V to V_{CS_N} (0.8 V) finally. The normal feedback loop will take over the control when the output voltage reaches its regulated value.

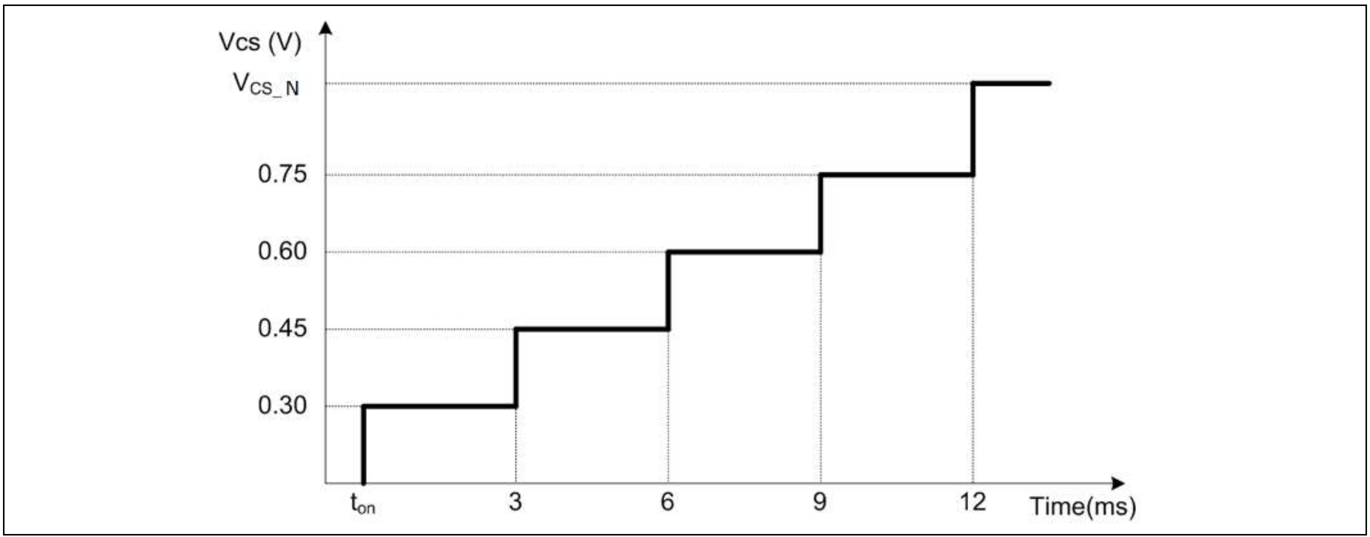


Figure 6 **Maximum current sense voltage during soft start**

3.3 Normal operation

The PWM controller during normal operation consists of a digital signal processing circuit including regulation control and an analog circuit including a current measurement unit and a comparator. Details about the full operation of the PWM controller in normal operation are illustrated in the following paragraphs.

3.3.1 PWM operation and peak current mode control

3.3.1.1 Switch-on determination

The power MOSFET turn-on is synchronized with the internal oscillator with a switching frequency f_{SW} that corresponds to the voltage level V_{FB} (see Figure 8).

3.3.1.2 Switch-off determination

In peak current mode control, the PWM comparator monitors voltage V_1 (see Figure 4) which is the representation of the instantaneous current of the power MOSFET. When V_1 exceeds V_{FB}, the PWM comparator sends a signal to switch off the GATE of the power MOSFET. Therefore, the peak current of the power MOSFET is controlled by the feedback voltage V_{FB} (see Figure 7).

At switch on transient of the power MOSFET, a voltage spike across R_{CS} can cause V_1 to increase and exceed V_{FB}. To avoid a false switch off, the IC has a blanking time t_{CS_LEB} before detecting the voltage across R_{CS} to mask the voltage spike. Therefore, the minimum turn on time of the power MOSFET is t_{CS_LEB}.

For some reason that the voltage level at V_1 takes long time to exceed V_{FB}, the IC has implemented a maximum duty cycle control to force the power MOSFET to switch off when D_{MAX} = 0.75 is reached.

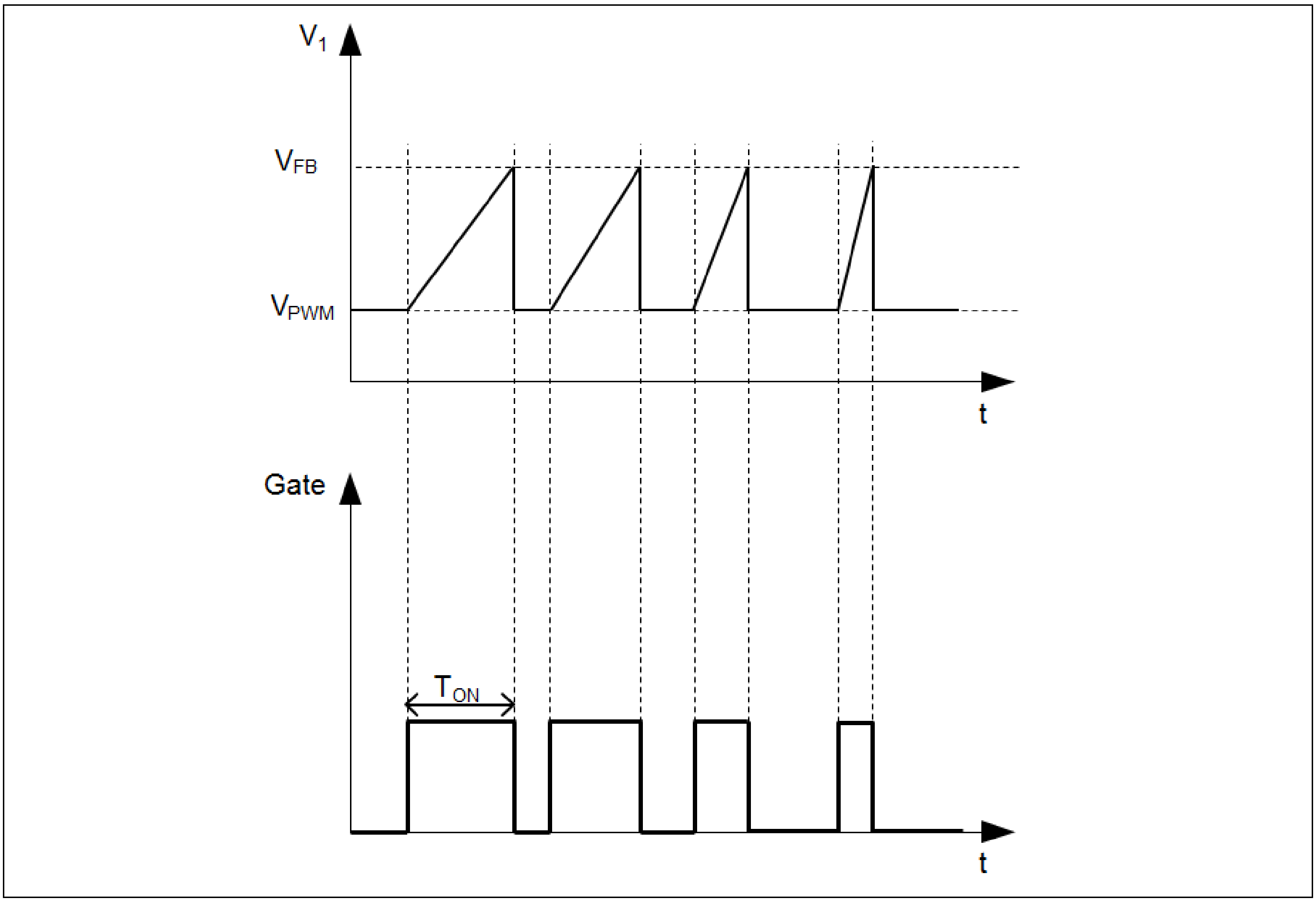


Figure 7 Pulse width modulation

3.3.2 Current sense

The power MOSFET current generates a voltage V_{CS} across the current sense resistor R_{CS} connected between the CS pin and the GND pin. V_{CS} is amplified with gain G_{PWM}, then, added with an offset V_{PWM} to become V_1 as described below in below equation 3.

$$V_{\mathrm{CS}} = I_{\mathrm{D}} \times R_{\mathrm{CS}} \tag{2}$$

$$V_1 = V_{\mathrm{CS}} * G_{\mathrm{PWM}} + V_{\mathrm{PWM}} \tag{3}$$

where, V_{CS} : CS pin voltage

I_D : power MOSFET current

R_{CS} : resistance of the current sense resistor

V_1 : voltage level compared to V_{FB} as described in section 3.3.1.2

G_{PWM} : PWM-OP gain

V_{PWM} : offset for voltage ramp

3.3.3 Frequency reduction

Frequency reduction is implemented in ICE5xSAG to achieve a better efficiency during the light load. At light load, the reduced switching frequency F_{SW} improves efficiency by reducing the switching loses.

When load decreases, V_{FB} decreases as well. F_{SW} is dependent on the V_{FB} as shown in Figure 8. Therefore, F_{SW} decreases as the load decreases.

Typically, F_{SW} at high load is 100 kHz/ 125 kHz and starts to decrease at V_{FB} = 1.7V. There is no further frequency reduction once it reached the f_{OSCx_MIN} even the load is further reduced.

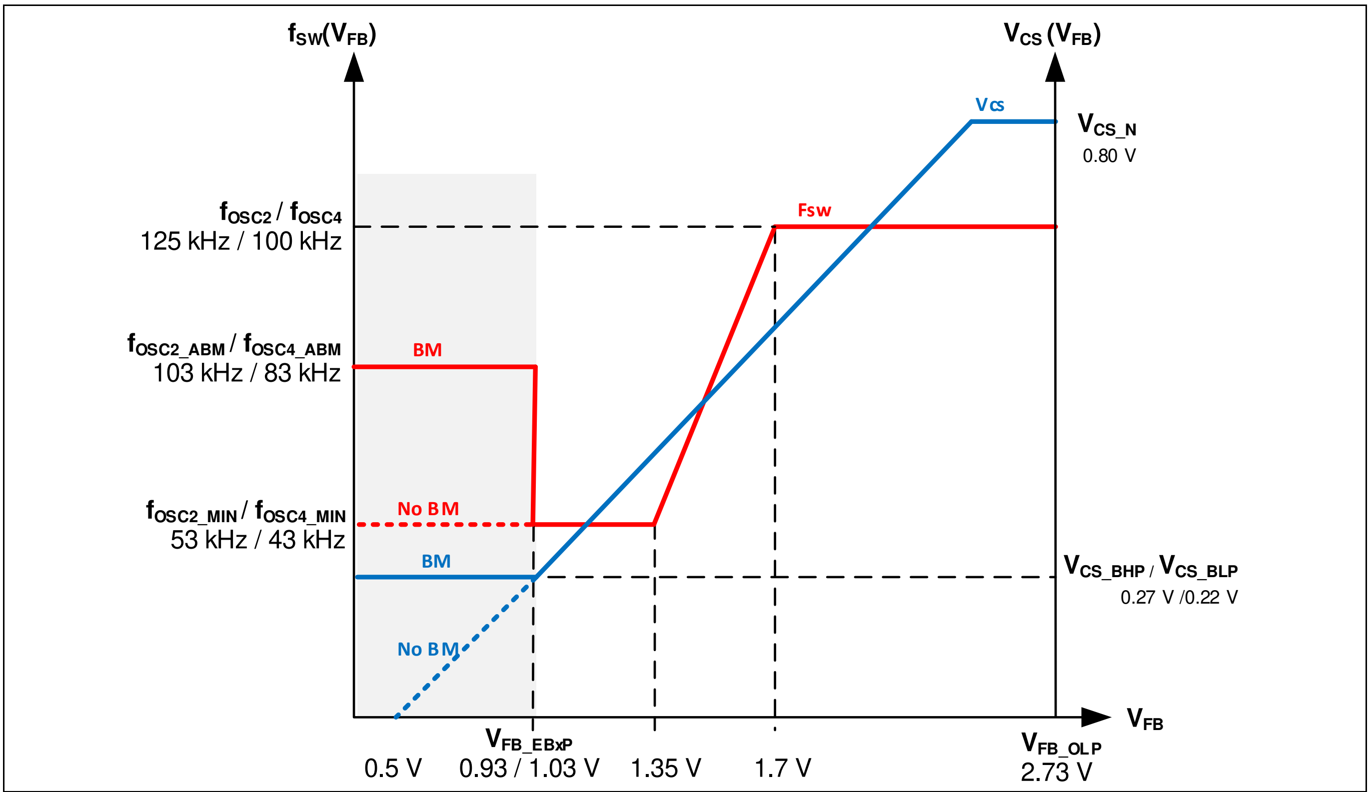


Figure 8 **Frequency reduction curve**

3.3.4 Slope compensation

ICE5xSAG can operate at Continuous Conduction Mode (CCM). At CCM operation, duty cycle greater than 50% may generate a sub-harmonic oscillation. To avoid the sub-harmonic oscillation, slope compensation is added to V_{CS} pin when the gate of the power MOSFET is turned on for more than 40% of the switching cycle period. The relationship between V_{FB} and the V_{CS} for CCM operation is described in below equation 4:

$$V_{FB} = V_{CS} * G_{PWM} + V_{PWM} + M_{COMP} * (T_{ON} - 40\% * T_{PERIOD}) \quad (4)$$

where, T_{ON} : gate turn on time of the power MOSFET

M_{COMP} : slope compensation rate

T_{PERIOD} : switching cycle period

Slope compensation circuit is disabled and no slope compensation is added into the V_{CS} pin during active burst mode to save the power consumption.

3.3.5 Oscillator and frequency jittering

The oscillator generates a frequency of 100 kHz/ 125 kHz with frequency jittering of ±4% at a jittering period of T_{JITTER} (4 ms). The frequency jittering helps to reduce conducted EMI.

A capacitor, a current source and current sink which determine the frequency are integrated. The charging and discharging current of the implemented oscillator capacitor are internally trimmed in order to achieve a highly accurate switching frequency.

Once the soft-start period is over and when the IC goes into normal operating mode, the frequency jittering is enabled. There is also frequency jittering during frequency reduction.

3.3.6 Modulated gate drive

The drive-stage is optimized for EMI consideration. The switch on speed is slowed down before it reaches the power MOSFET turn on threshold. That is a slope control of the rising edge at the output of driver (see Figure 9). Thus the leading switch spike during turn on is minimized.

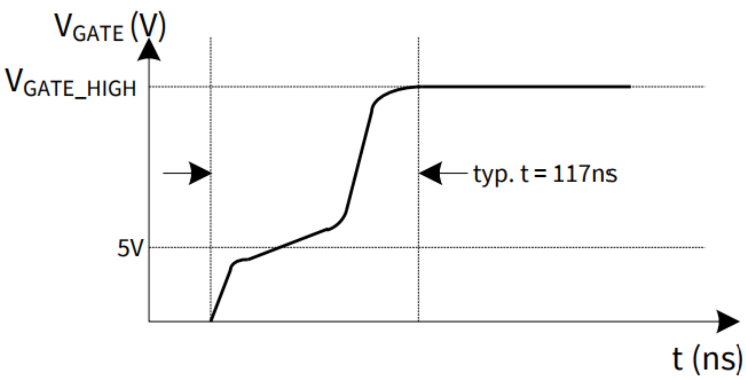


Figure 9 Gate rising waveform

3.4 Peak current limitation

There is a cycle by cycle peak current limitation realized by the current limit comparator to provide primary over-current protection. The primary current generates a voltage V_{CS} across the current sense resistor R_{CS} connected between the CS pin and the GND pin. If the voltage V_{CS} exceeds an internal voltage limit V_{CS_N}, the comparator immediately turns off the gate drive.

The primary peak current I_{PEAK_PRI} can be calculated as below:

$$I_{\mathrm{PEAK\_PRI}} = V_{\mathrm{CS\_N}}/R_{\mathrm{CS}} \quad (5)$$

To avoid mistriggering caused by MOSFET switch on transient voltage spikes, a leading edge blanking time (t_{CS_LEB}) is integrated in the current sensing path.

3.4.1 Propagation delay compensation

In case of overcurrent detection, there is always a propagation delay from sensing the V_{CS} to switching the power MOSFET off. An overshoot on the peak current I_{peak} caused by the delay depends on the ratio of dI/dt of the primary current (see Figure 10).

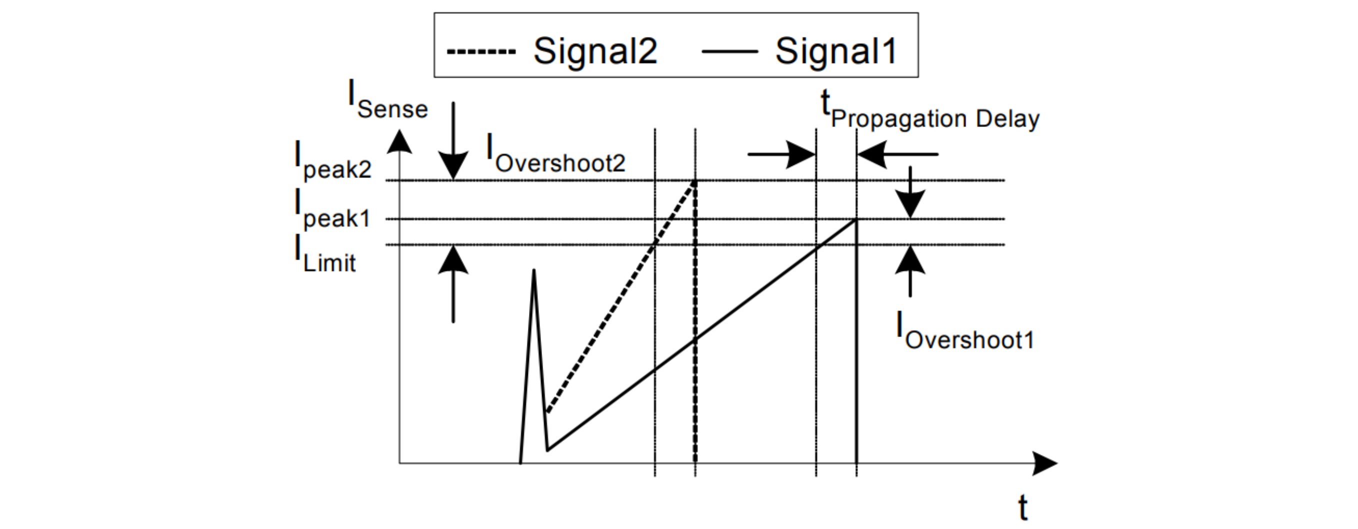


Figure 10 Current limiting

The overshoot of Signal2 is larger than Signal1 due to the steeper rising waveform. This change in the slope is depending on the AC input voltage. Propagation delay compensation is integrated to reduce the overshoot due to dI/dt of the rising primary current. Thus the propagation delay time between exceeding the current sense threshold V_{CS_N} and the switching off of the power MOSFET is compensated over wide bus voltage range. Current limiting becomes more accurate which will result in a minimum difference of overload protection triggering power between low and high AC line input voltage.

Under CCM operation, the same V_{CS} do not result in the same power. In order to achieve a close overload triggering level for CCM, ICE5xSAG has implemented a 2 compensation curve as shown Figure 11. One of the curve is used for T_{ON} greater than 0.40 duty cycle and the other is for lower than 0.40 duty cycle.

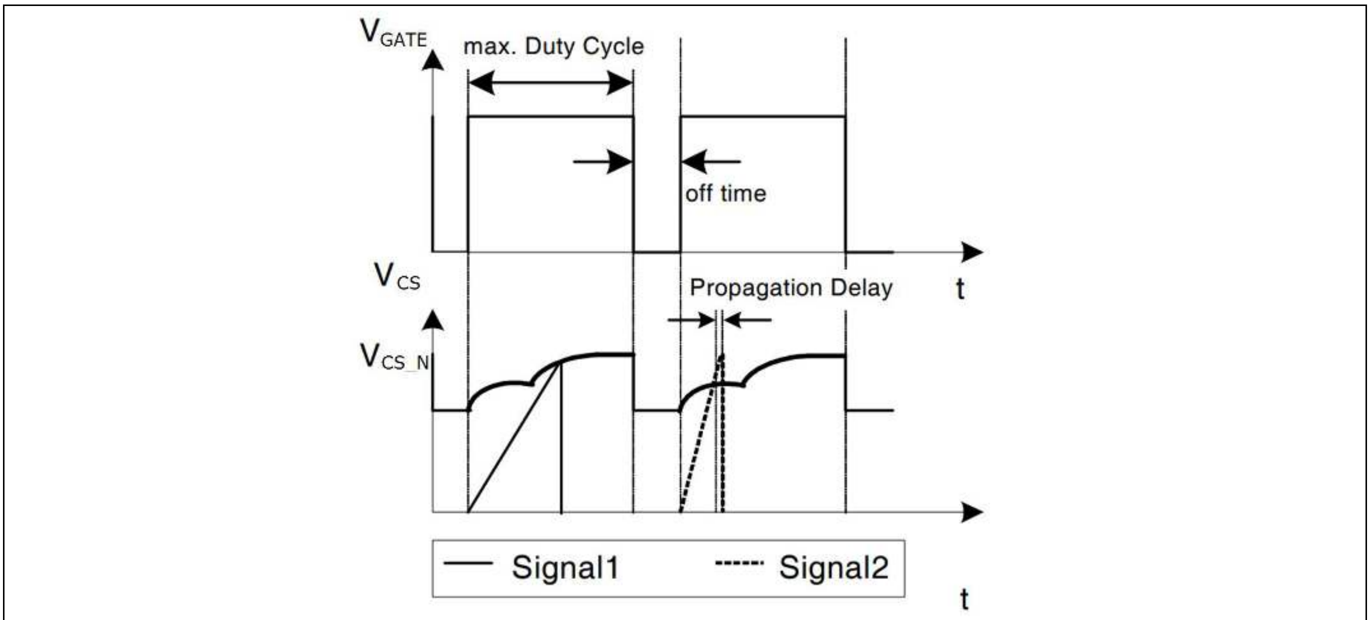


Figure 11 Dynamic voltage threshold V_{CS_N}

Similarly, the same concept of propagation delay compensation is also implemented in ABM with reduced level. With this implementation, the entry and exit burst mode power can be close between low and high AC line input voltage.

3.5 Active Burst Mode (ABM) with selectable power level

At light load condition, the IC enters ABM operation to minimize the power consumption. Details about ABM operation are explained in the following paragraphs.

3.5.1 Entering ABM operation

The sytem will enter into ABM operation when two conditions below are met:

- the FB voltage is lower than the threshold of V_{FB_EBLP}/V_{FB_EBHP} depending on burst configuration option setup
- and a certain blanking time t_{FB_BEB}

Once all of these conditions are fulfilled, the ABM flip-flop is set and the controller enters ABM operation. This multi-condition determination for entering ABM operation prevents mis-triggering of entering ABM operation, so that the controller enters ABM operation only when the output power is really low.

3.5.2 During ABM operation

After entering ABM, the PWM section will be inactive making the V_{OUT} start todecrease. As the V_{OUT} decreases, V_{FB} rises. Once V_{FB} exceeded V_{FB_BOn}, the internal circuit is again activated by the internal bias to start with the switching.

If the PWM is still operating and the output load is still low, V_{OUT} increases and V_{FB} signal starts to decrease. When V_{FB} reaches the low threshold V_{FB_BOff}, the internal bias is reset again and the PWM section is disabled with no switching until V_{FB} increases back to exceed V_{FB_BOn} threshold.

In ABM, V_{FB} is like a sawtooth waveform swinging between V_{FB_BOff} and V_{FB_BOn} shown in Figure 12.

During ABM, the switching frequency f_{OSCx_ABM} is 83 kHz for 100 kHz version and 103 kHz for 125 kHz version IC. The peak current $I_{PEAK_ABM}$of the power MOSFET is defined by:

$$I_{\mathrm{PEAK\_ABM}} = V_{\mathrm{CS\_BxP}}/R_{\mathrm{CS}} \tag{6}$$

where V_{CS_BxP} is the peak current limitation in ABM

3.5.3 Leaving ABM operation

The FB voltage immediately increases if there is a sudden increase in the output load. When V_{FB} exceeds $V_{FB\_LB,}$ it will leave ABM and the peak current limitation trhreshold voltage will return back to V_{CS_N} immediately.

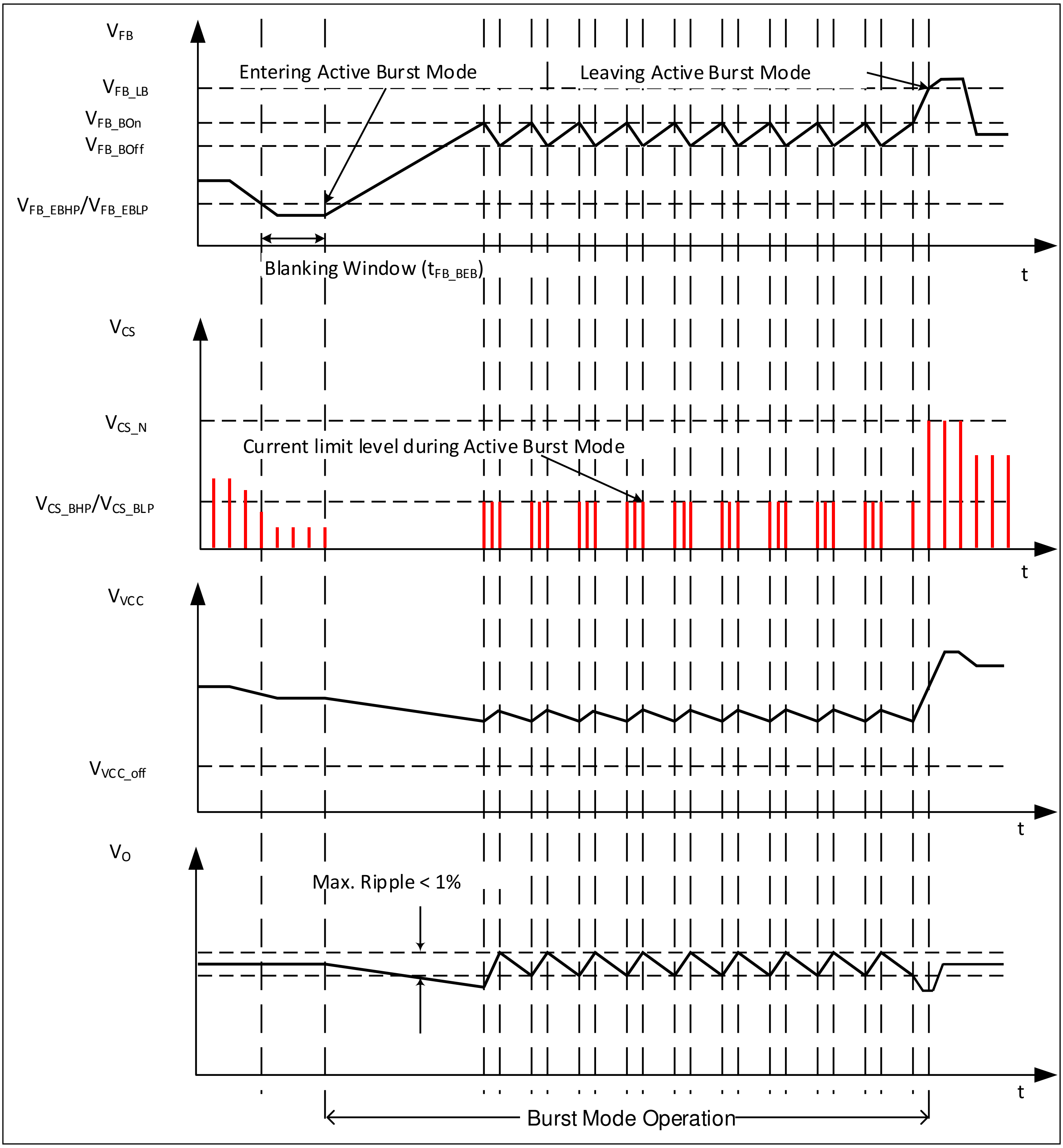


Figure 12 **Signals in Active Burst Mode**

3.5.4 ABM configuration

The burst mode entry level can be selected by changing the different resistance R_{Sel} at FB pin. There are 3 configuration options depending on R_{Sel} which corresponds to the options of no ABM (Option 1), low range of ABM power (Option 2) and high range of ABM power (Option 3). The table below shows the control logic for the entry and exit level with the FB voltage.

Table 3 ABM configuration option setup

Option	R_{Sel}	V_{FB}	V_{CS_BxP}	Entry level	Exit level
				V_{FB_EBxP}	V_{FB_LB}
1	<470 kΩ	$V_{FB} < V_{FB\_P\_BIAS1}$	-	No ABM	No ABM
2	720 kΩ ~ 790 kΩ	$V_{FB\_P\_BIAS1} < V_{FB} < V_{FB\_P\_BIAS2}$	0.22V	0.93 V	2.73 V
3(Default)	>1210 kΩ	$V_{FB} > V_{FB\_P\_BIAS2}$	0.27V	1.03 V	2.73 V

During IC first startup, the controller preset the ABM selection to Option 3, the FB resistor (R_{FB}) is turned off by internal switch S2 (see Figure 13)and a current source I_{sel} is turned on instead.From V_{CC}= 4.44 V to V_{CC} on threshold, the FB pin will start to charge resistor R_{Sel} with current I_{Sel} to a certain voltage level. When V_{CC} reaches V_{CC} on threshold, the FB voltage is sensed. The burst mode option is then chosen according to the FB voltage level. After finishing the selection, any change on the FB level will not change the burst mode option and the current source (I_{sel}) is turned off while the FB resistor (R_{FB}) is connected back to the circuit (Figure 13).

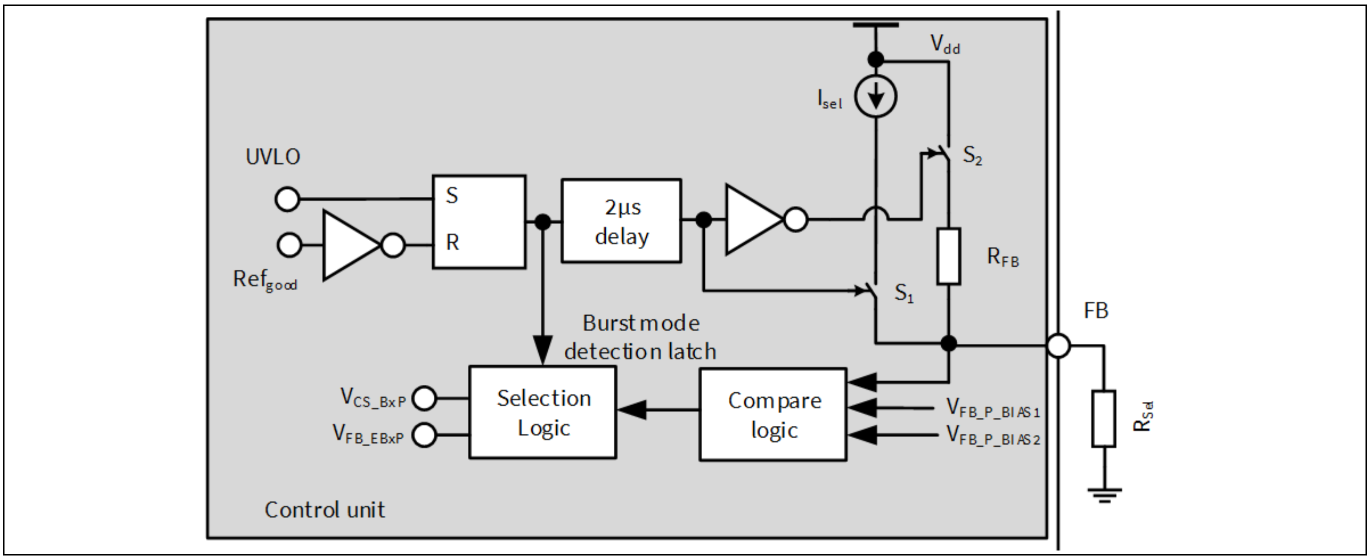


Figure 13 ABM detect and adjust

3.6 Non-isolated/isolated configuration

ICE5xSAG has a VERR Pin, which is connected to the input of an integrated error amplifier to support non-isolated flyback application (see Figure 2). When V_{CC} is charging and before reaching the V_{CC} on threshold, a current source $I_{ERR\_P\_BIAS}$ from VERR pin together with R_{F1} and R_{F2} will generate a voltage across it. If VERR voltage is more than $V_{ERR\_P\_BIAS}$ (0.2 V), non-isolated configuration is selected, otherwise, isolated configuration is selected. In isolated configuration, the error amplifier output is disconnected from the FB pin.

In case of non-isolated configuration, the voltage divider R_{F1} and R_{F2} is used to sense the output voltage and compared with the internal reference voltage V_{ERR_REF}. The difference between the sensed voltage and the reference voltage is converted as an output current by the error amplifier. The output current will charge/discharge the resistor and capacitor network connected at the FB pin for the loop compensation.

3.7 Protection functions

The ICE5xSAG provides numerous protection functions which considerably improve the power supply system robustness, safety and reliability. The following table summarizes these protection functions and the corresponding protection mode whether as a non switch auto restart, auto restart or odd skip auto restart mode. Refer to Figure 14, Figure 15 and Figure 16 for the waveform illustration of protection modes.

Table 4 Protection functions

Protection Functions	Normal Mode	Burst Mode		Protection Mode
		Burst ON	Burst OFF	
Line over voltage	√	√	√	Non switch auto restart
V_{CC} over voltage	√	√	NA[1]	Odd skip auto restart
V_{CC} under voltage	√	√	√	Auto restart
Overload/ open loop	√	NA[1]	NA[1]	Odd skip auto restart
Over temperature	√	√	√	Non switch auto restart
CS short to GND	√	√	NA[1]	Odd skip auto restart
V_{CC} short to GND	√	√	√	No startup

3.7.1 Line over voltage

The AC Line Over Voltage Protection (LOVP) is detected by sensing bus capacitor voltage through VIN pin via voltage divider resistors, Rl1 and Rl2 (Figure 1). Once V_{VIN} voltage is higher than the line over voltage threshold (V_{VIN_LOVP}), the controller enters into protection mode until V_{VIN} is lower than V_{VIN_LOVP}. This protection can be disabled by connecting VIN pin to GND.

3.7.2 V_{CC} over/under voltage

During operation, the V_{CC} voltage is continuously monitored. If V_{CC} is either below V_{VCC_OFF} for 50 µs ($t_{VCC\_OFF\_B}$) or above V_{VCC_OVP} for 55 µs ($t_{VCC\_OVP\_B}$), the power MOSFET is kept switch off. After the V_{CC} voltage falls below the threshold V_{VCCoff}, the new start up sequence is activated. The V_{CC} capacitor is then charged up. Once the voltage exceeds the threshold V_{VCC_ON}, the IC begins to operate with a new soft-start.

3.7.3 Overload/ open loop

In case of open control loop or output overload, the FB voltage will be pulled up. When V_{FB} exceeds V_{FB_OLP} after a blanking time of $t_{FB\_OLP\_B}$, the IC enters odd skip auto restart mode. The blanking time enables the converter to provide a peak power in case the increase in V_{FB} is due to a sudden load increase.

3.7.4 Over temperature

If the junction temperature of controller exceeds T_{jcon_OTP}, the IC enters into Over Temperature Protection (OTP) auto restart mode. The IC has also implemented with a 40 °C hysteresis. That means the IC can only be recovered from OTP when the controller junction temperature is dropped 40 °C lower than the over temperature trigger point.

[1] Not Applicable

3.7.5 CS short to GND

If the voltage at the current sense pin is lower than the preset threshold V_{CS_STG} with certain blanking time $t_{CS\_STG\_B}$ for three consecutive pulses during on-time of the power switch, the IC enters CS short to GND protection.

3.7.6 V_{CC} short to GND

To limit the power dissipation of the startup circuit at V_{CC} short to GND condition, the V_{CC} charging current is limited to a minimum level of $I_{VCC\_Charge1}$. With such low current, the power loss of the IC is limited to prevent overheating.

3.7.7 Protection modes

All the protections are in auto restart mode with a new soft start sequence. The three auto restart modes are illustrated in the following figures.

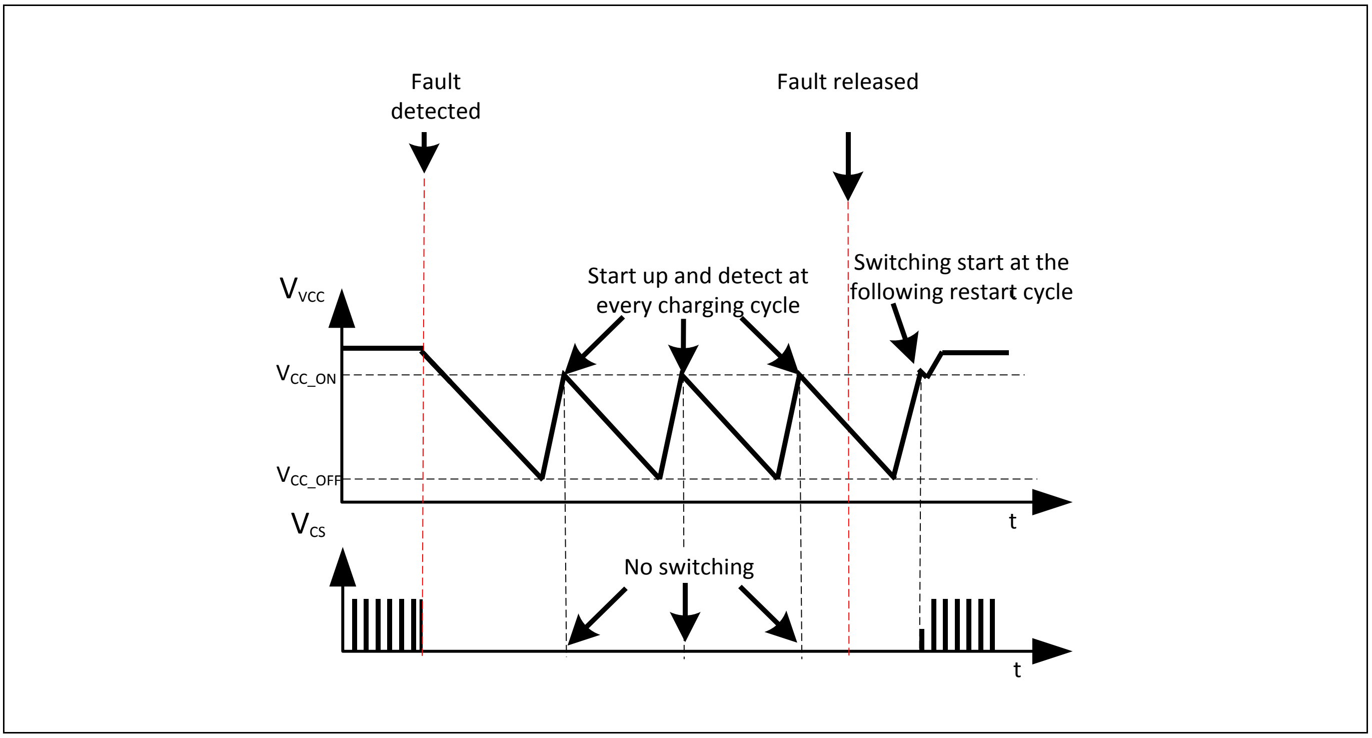


Figure 14 Non switch auto restart mode

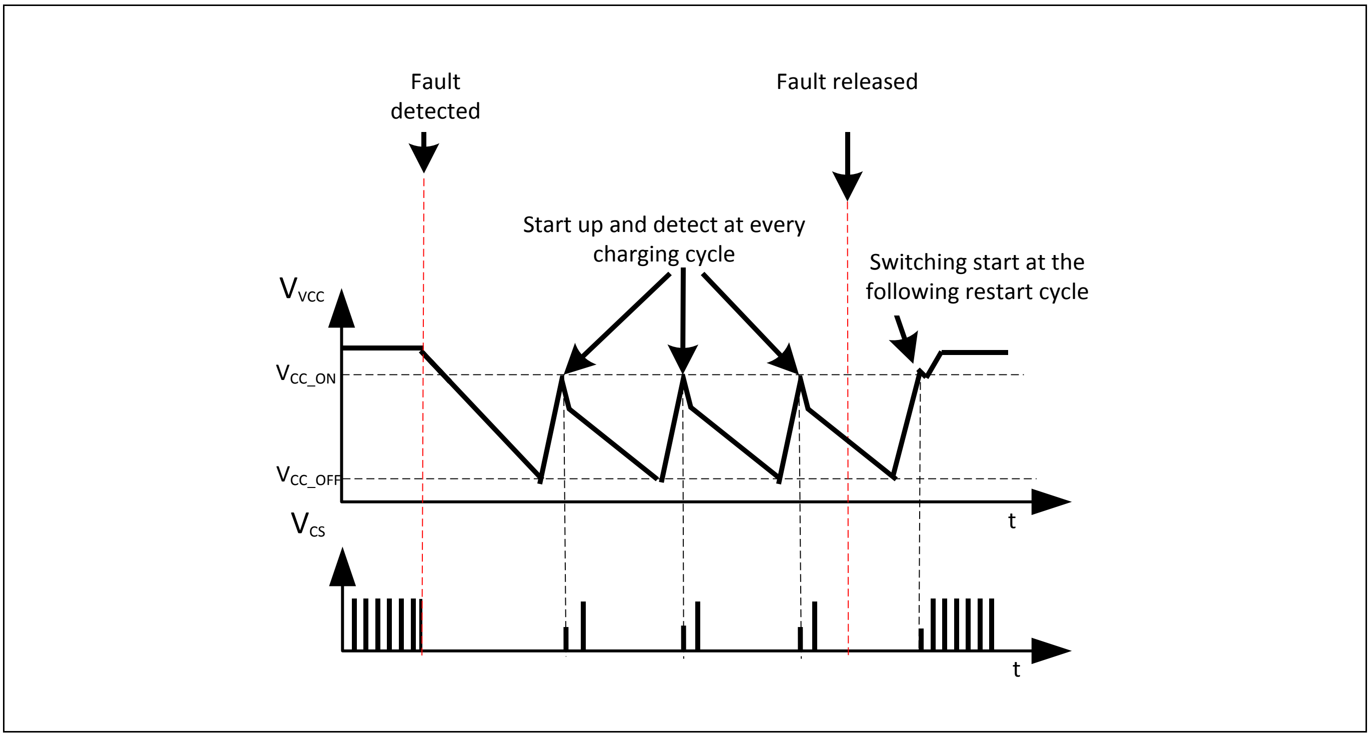


Figure 15 Auto restart mode

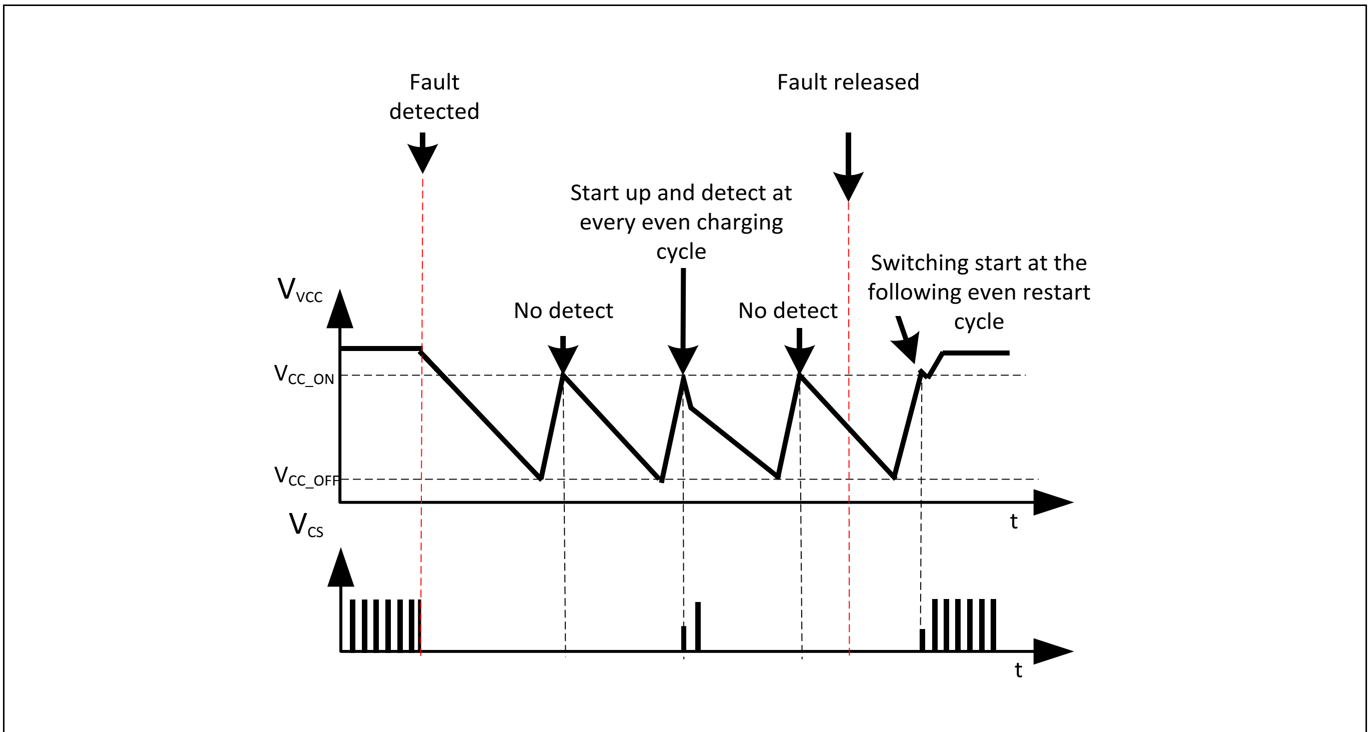


Figure 16 Odd skip auto restart

4 Electrical characteristics

Attention: *All voltages are measured with respect to ground (Pin 8). The voltage levels are valid if other ratings are not violated.*

4.1 Absolute maximum ratings

Attention: *Stresses above the maximum values listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Maximum ratings are absolute ratings; exceeding any one of these values may cause irreversible damage to the integrated circuit. For the same reason, make sure that any capacitor that will be connected to pin 7 (VCC) is discharged before assembling the application circuit. T_a=25 °C unless otherwise specified.*

Table 5 Absolute maximum ratings

Parameter	Symbol	Limit Values		Unit	Note / Test Condition
		Min.	Max.		
VCC Supply Voltage	V_{CC}	-0.3	27.0	V	
SOURCE Voltage	V_{SOURCE}	-0.3	27.0	V	
GATE Voltage	V_{GATE}	-0.3	27.0	V	
FB Voltage	V_{FB}	-0.3	3.6	V	
VERR Voltage	V_{ERR}	-0.3	3.6	V	
CS Voltage	V_{CS}	-0.3	3.6	V	
VIN Voltage	V_{IN}	-0.3	3.6	V	
DC current at SOURCE pin	I_{SOURCE}	-	0.9	A	Limited by $T_{J,Max}$
Single pulse current at SOURCE pin	I_{S_pulse}	-	5.8	A	Pulse width t_p = 20 µs and limited by $T_{J,Max}$
Maximum DC current on any pin		-10.0	10.0	mA	Except SOURCE and CS pin
ESD robustness HBM	V_{ESD_HBM}	-	2000	V	According to EIA/JESD22
ESD robustness CDM	V_{ESD_CDM}	-	500	V	
Junction temperature range	T_J	-40	150	°C	
Storage Temperature	T_{STORE}	-55	150	°C	
Thermal Resistance (Junction- Ambient)	R_{thJA}	-	185	K/W	Setup according to the JEDEC standard JESD51

4.2 Operating range

Note: *Within the operating range, the IC operates as described in the functional description.*

Table 6 Operating range

Parameter	Symbol	Limit Values		Unit	Remark
		Min.	Max.		
VCC Supply Voltage	V_{VCC}	V_{VCC_OFF}	V_{VCC_OVP}		

Junction Temperature of controller	T_{jCon_op}	*-40*	T_{jCon_OTP}	°C	Max value limited due to OTP of controller chip

4.3 Operating conditions

Note: *The electrical characteristics involve the spread of values within the specified supply voltage and junction temperature range T_J from – 40 °C to 125 °C. Typical values represent the median values, which are related to 25 °C. If not otherwise stated, a supply voltage of V_{CC} = 18 V is assumed.*

Table 7 Operating conditions

Parameter	Symbol	Limit Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
VCC Charge Current	$I_{VCC\_Charge1}$	-0.35	-0.20	-0.09	mA	V_{VCC}=0 V, $R_{StartUp}$=50 MΩ and V_{DRAIN}=90 V
	$I_{VCC\_Charge2}$	-	-3.2	-	mA	V_{VCC}=3 V, $R_{StartUp}$=50 MΩ and V_{DRAIN}=90 V
	$I_{VCC\_Charge3}$	-5	-3	-1	mA	V_{VCC}=15 V, $R_{StartUp}$=50 MΩ and V_{DRAIN}=90 V
Current Consumption, Startup Current	$I_{VCC\_Startup}$	-	0.25	-	mA	V_{VCC}=15 V
Current Consumption, Normal	I_{VCC_Normal}	-	0.9	-	mA	I_{FB}=0 A (No gate switching)
Current Consumption, Auto Restart	I_{VCC_AR}	-	410	-	µA	
Current Consumption, Burst Mode – Isolated	$I_{VCC\_BurstMode\_ISO}$	-	0.54	-	mA	
Current Consumption, Burst Mode – Non-Isolated	$I_{VCC\_BurstMode\_NISO}$	-	0.61	-	mA	
VCC Turn-on Threshold Voltage	V_{VCC_ON}	15.3	16.0	16.5	V	
VCC Turn-off Threshold Voltage	V_{VCC_OFF}	9.4	10.0	10.4	V	
VCC Short Circuit Protection	V_{VCC_SCP}	-	1.1	1.9	V	
VCC Turn-off blanking	$t_{VCC\_OFF\_B}$	-	50	-	µs	

4.4 Internal voltage reference

Table 8 Internal voltage reference

Parameter	Symbol	Limit Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Internal Reference Voltage	V_{REF}	3.20	3.30	3.39	V	Measured at pin FB I_{FB}=0 A

4.5 Gate driver

Table 9 Gate driver

Parameter	Symbol	Limit Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Output voltage at logic low	V_{GATE_LOW}	-	-	1.00	V	
Output voltage at logic high	V_{GATE_HIGH}	8	10	13	V	

Rise Time	t_{GATE_RISE}	-	117	-	ns	Cout = 1.1nF
Fall Time	t_{GATE_FALL}	-	27	-	ns	Cout = 1.1nF

4.6 PWM section

Table 10 PWM section

Parameter	Symbol	Limit Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Fixed Oscillator Frequency – 125 kHz	f_{OSC1}	117	125	133	kHz	
	f_{OSC2}	119	125	131	kHz	T_j = 25 °C
Fixed Oscillator Frequency – 100 kHz	f_{OSC3}	92	100	108	kHz	
	f_{OSC4}	94	100	106	kHz	T_j = 25 °C
Fixed Oscillator Frequency – 125 kHz (Active Burst Mode)	f_{OSC2_ABM}	91	103	114	kHz	T_j = 25 °C
Fixed Oscillator Frequency – 100 kHz (Active Burst Mode)	f_{OSC4_ABM}	71	83	94	kHz	T_j = 25 °C
Fixed Oscillator Frequency – 125 kHz (Minimum Fsw)	f_{OSC2_MIN}	46	53	61	kHz	T_j = 25 °C
Fixed Oscillator Frequency – 100 kHz (Minimum Fsw)	f_{OSC4_MIN}	36	43	51	kHz	T_j = 25 °C
Frequency Jittering Range	F_{JITTER}	-	+/- 4	-	%	T_j = 25 °C
Frequency Jittering period	T_{JITTER}	-	4	-	ms	T_j = 25 °C
Maximum Duty Cycle	D_{MAX}	70	75	80	%	
Feedback Pull-Up Resistor	R_{FB}	11	15	20	kΩ	
PWM-OP Gain	G_{PWM}	1.91	2.03	2.16		
Offset for Voltage Ramp	V_{PWM}	0.42	0.50	0.58	V	
Slope Compensation rate – 125 kHz	M_{COMP}	52.5	61.0	68.0	mV/µs	V_{CS}=0 V
Slope Compensation rate - 100 kHz	M_{COMP}	41	50	58	mV/µs	V_{CS}=0 V

4.7 Error amplifier

Table 11 Error amplifier

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Transconductance	G_{ERR_M}	2.14	2.80	3.44	mA/V	
Transconductance – Burst Mode	G_{ERR_BM}	6.9	9.2	11.6	mA/V	
Error Amplifier Source Current	I_{ERR_SOURCE}	85	150	223	µA	
Error Amplifier Sink Current	I_{ERR_SINK}	85	150	223	µA	
Error Amplifier Reference Voltage	V_{ERR_REF}	1.76	1.80	1.84	V	

Error Amplifier Output Dynamic Range of Transconductance	V_{ERR_DYN}	0.05	-	3.15	V	
Error Amplifier Mode Bias Current	$I_{ERR\_P\_BIAS}$	9.5	14.0	18.5	μ A	
Error Amplifier Mode Threshold	$V_{ERR\_P\_BIAS}$	0.16	0.20	0.24	V	

4.8 Current sense

Table 12 Current sense

Parameter	Symbol	Limit Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Peak current limitation in normal operation	V_{CS_N}	0.72	0.80	0.88	V	$dv_{sense}/dt = 0.41V/\mu s$
Peak current limitation in normal operation, 15% of T_{ON}	V_{CS_N15}	0.74	0.79	0.84	V	
Leading Edge Blanking time	t_{CS_LEB}	70	220	365	ns	
Peak Current Limitation in Active Burst Mode - High Power	V_{CS_BHP}	0.23	0.27	0.31	V	
Peak Current Limitation in Active Burst Mode - Low Power	V_{CS_BLP}	0.18	0.22	0.26	V	

4.9 Soft start

Table 13 Soft start

Parameter	Symbol	Limit Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Soft-Start time	t_{SS}	7.3	12.0	-	ms	
Soft-start time step	t_{SS_S}[1]	-	3	-	ms	
CS peak voltage at first step of soft start	V_{SS1}[1]	-	0.30	-	V	CS peak voltage
Step increment of CS peak voltage in soft start	V_{SS_S}[1]	-	0.15	-	V	CS peak voltage

4.10 Active Burst Mode

Table 14 Active Burst Mode

Parameter	Symbol	Limit Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Charging current to select burst mode	I_{sel}	2.5	3.0	3.5	μA	
Burst mode selection reference voltage Threshold	$V_{FB\_P\_BIAS1}$	1.65	1.73	1.80	V	

[1] The parameter is not subjected to production test - verified by design/characterization

Burst mode selection reference voltage Threshold	$V_{FB\_P\_BIAS2}$	2.76	2.89	3.01	V	
Feedback voltage for entering ABM for high power	V_{FB_EBHP}	0.98	1.03	1.08	V	
Feedback voltage for entering ABM for low power	V_{FB_EBLP}	0.88	0.93	0.98	V	
Blanking time for entering Active Burst Mode	t_{FB_BEB}	-	36	-	ms	
Feedback voltage for leaving Active Burst Mode	V_{FB_LB}	2.63	2.73	2.83	V	
Feedback voltage for burst-on – Isolated Case	$V_{FB\_Bon\_ISO}$	2.26	2.35	2.45	V	
Feedback voltage for burst-off – Isolated Case	$V_{FB\_Boff\_ISO}$	1.88	2.00	2.05	V	
Feedback voltage for burst-on – Non-Isolated Case	$V_{FB\_Bon\_NISO}$	1.88	1.95	2.05	V	
Feedback voltage for burst-off – Non-Isolated Case	$V_{FB\_Boff\_NISO}$	1.50	1.55	1.64	V	

4.11 Line over voltage protection

Table 15 Line OVP

Parameter	Symbol	Limit Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Line Over Voltage threshold	V_{VIN_LOVP}	2.75	2.85	2.95	V	
Line Over Voltage Blanking	$t_{VIN\_LOVP\_B}$	-	250	-	µs	

4.12 V_{CC} over voltage protection

Table 16 V_{CC} over voltage protection

Parameter	Symbol	Limit Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
VCC Over Voltage threshold	V_{VCC_OVP}	24.0	25.5	27.0	V	
VCC Over Voltage blanking	$t_{VCC\_OVP\_B}$	-	55	-	µs	

4.13 Overload protection

Table 17 Overload protection

Parameter	Symbol	Limit Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Over Load Detection threshold for OLP protection at FB pin	V_{FB_OLP}	2.63	2.73	2.83	V	

Over Load Protection Blanking Time	$t_{FB\_OLP\_B}$	30	54	-	ms	

4.14 Thermal protection

Table 18 Thermal protection

Parameter	Symbol	Limit Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Over temperature protection	T_{jcon_OTP}[1]	129	140	150	°C	
Over temperature Hysteresis	T_{jHYS_OTP}	-	40	-	°C	
Over temperature Blanking Time	$T_{jcon\_OTP\_B}$	-	50	-	µs	

4.15 CS short to GND protection

Table 19 CS short to GND protection

Parameter	Symbol	Limit Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
CS Short to Gnd Protection	V_{CS_STG}	0.06	0.10	0.15	V	
CS Short to Gnd Consecutive Trigger	P_{CS_STG}	-	3	-	cycle	
CS Short to Gnd Sample period	$t_{CS\_STG\_SAM}$	t_{PERIOD} * 0.36	t_{PERIOD} * 0.4	t_{PERIOD} * 0.44	µs	

4.16 Low side MOSFET

Table 20 Low side MOSFET

Parameter	Symbol	Limit Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Drain Source On-Resistance	R_{DSon}	- -	0.22 0.31[1]	0.29 -	Ω	$T_j = 25$ °C $T_j = 125$ °C

[1]The parameter is not subjected to production test - verified by design/characterization

5 Output power curve

The calculated output power curves versus ambient temperature are shown below. The curves are derived based on a typical DCM/CCM flyback in an open frame design setting the maximum T_J at 125 °C, using minimum pin copper area in a 2 oz copper single sided PCB and steady state operation only (no design margins for abnormal operation modes are included).

The output power figure is for reference only. The actual power can vary depending on a particular design. In a power supply system, appropriate thermal design margins must be considered to make sure that the operation of the device is within the maximum ratings given in section 4.1.

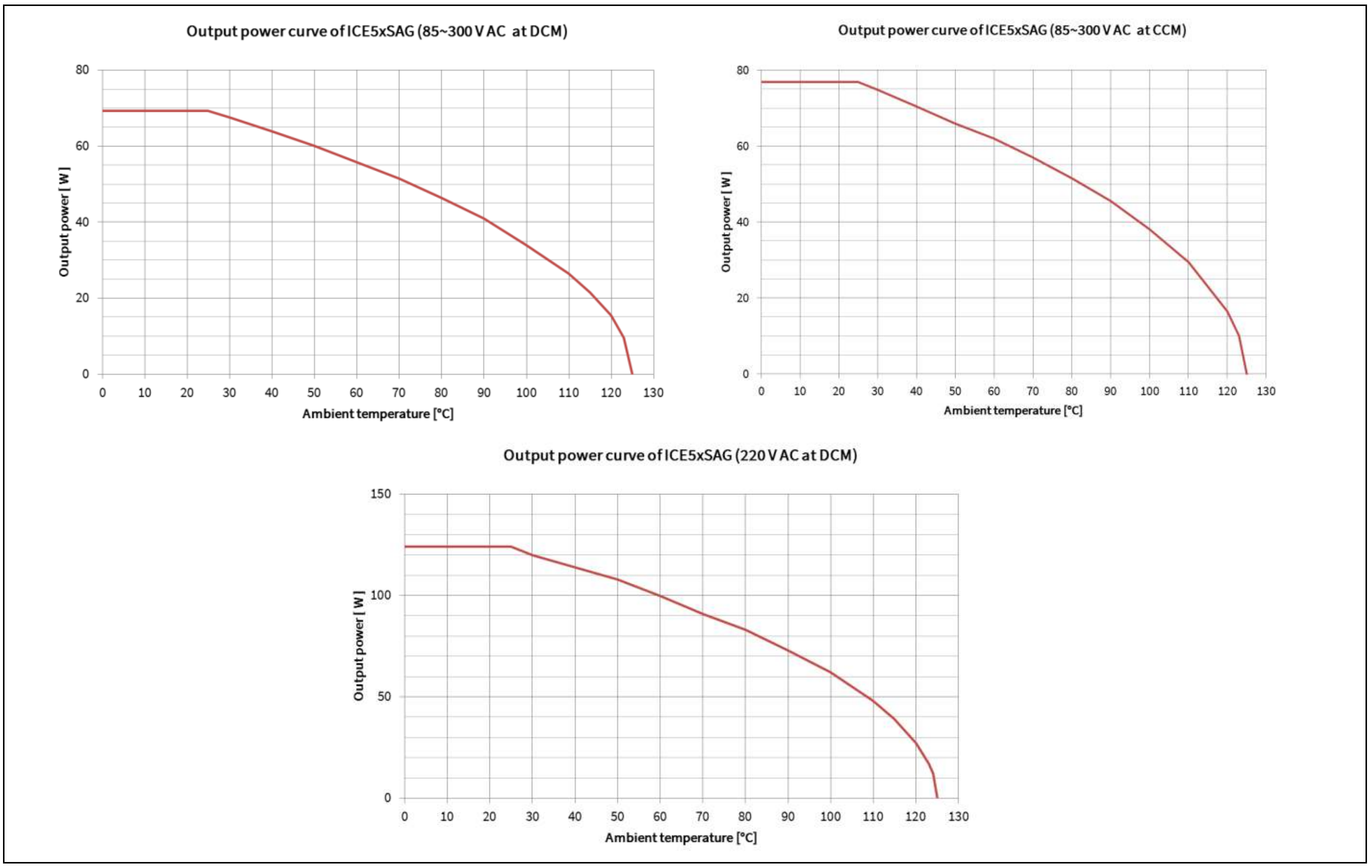
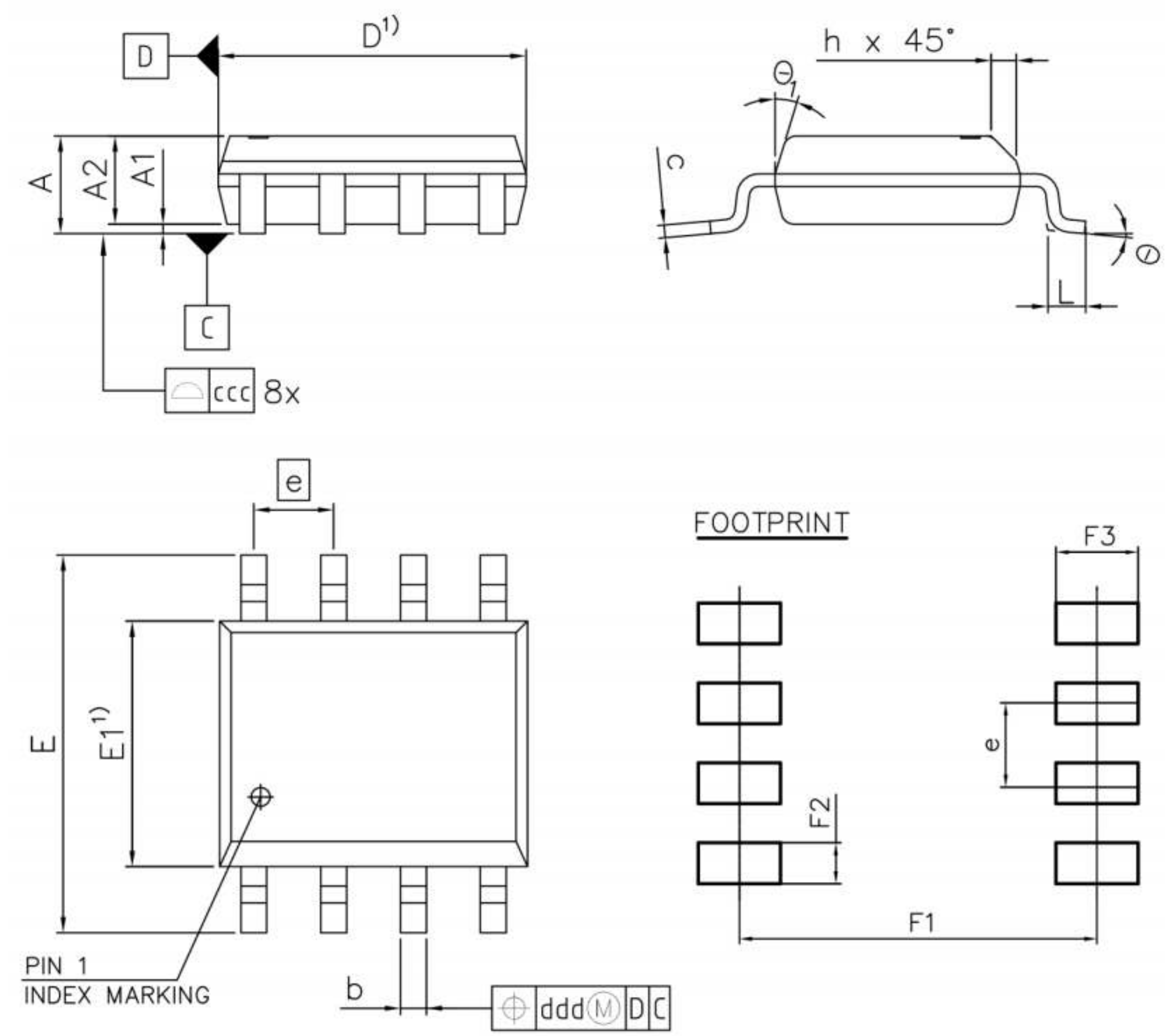


Figure 17 Output power curve of ICE5xSAG

6 Outline dimension



1) DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	-	1.75	-	0.069
A1	0.10	-	0.004	-
A2	1.25	1.65	0.049	0.065
b	0.35	0.51	0.014	0.020
c	0.17	0.25	0.007	0.010
D	4.80	5.00	0.189	0.197
E	5.80	6.20	0.228	0.244
E1	3.80	4.00	0.150	0.157
e	1.27		0.050	
N	8		8	
L	0.39	0.89	0.015	0.035
h	0.23	0.50	0.009	0.020
Θ	0°	8°	0°	8°
$Θ_1$	-	19°	-	19°
ccc	0.10		0.004	
ddd	0.25		0.010	
F1	5.59	5.79	0.220	0.228
F2	0.55	0.75	0.022	0.030
F3	1.21	1.41	0.048	0.056

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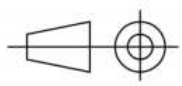

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Figure 18 PG-DSO-8

7 Marking

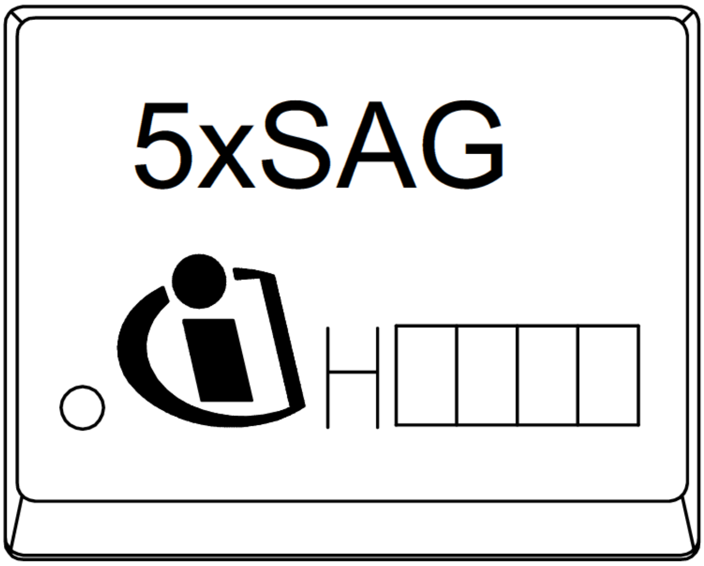

Figure 19 Marking of PG-DSO-8

Revision history

Document version	Date of release	Description of changes
V 2.0	21 Nov 2017	First release
V 2.1	27 Feb 2018	Page 1 Product validation text content revised
V 2.2	2 Mar 2018	Page 19, Table 5 • The symbol of parameter SOURCE voltage changed from V_{CC} to V_{SOURCE} • The symbol of parameter VIN voltage changed from V_{CS} to V_{IN} Page 19, Table 5 (refer to errata sheet 10167AERRA) • Add parameters DC current at SOURCE pin and Single pulse current at SOURCE pin

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