Document Number: A3I20X050N
Rev. 2, 05/2020

RoHS

RF LDMOS Wideband Integrated Power Amplifiers

A3I20X050N
A3I20X050GN

1800–2200 MHz, 6.3 W Avg., 28 V
AIRFAST RF LDMOS
INTEGRATED POWER AMPLIFIERS

The A3I20X050N integrated Doherty circuit is designed with on-chip matching that makes it usable from 1800 to 2200 MHz. This multi-stage structure is rated for 20 to 32 V operation and covers all typical cellular base station modulation formats.

1800 MHz

- Typical Doherty Single-Carrier W-CDMA Characterization Performance: V_{DD} = 28 Vdc, $I_{DQ(Carrier)}$ = 160 mA, $V_{GS(Peaking)}$ = 2.15 Vdc, P_{out} = 6.3 W Avg., Input Signal PAR = 9.9 dB @ 0.01% Probability on CCDF. (1)

Frequency	G_{ps} (dB)	PAE (%)	ACPR (dBc)
1805 MHz	28.7	38.1	–37.1
1840 MHz	28.7	39.1	–39.7
1880 MHz	28.7	39.0	–37.5

1800–2200 MHz

- Typical Doherty Single-Carrier W-CDMA Performance: V_{DD} = 28 Vdc, $I_{DQ(Carrier)}$ = 145 mA, $V_{GS(Peaking)}$ = 2.20 Vdc, P_{out} = 6.3 W Avg., Input Signal PAR = 9.9 dB @ 0.01% Probability on CCDF. (1)

Frequency	G_{ps} (dB)	PAE (%)	ACPR (dBc)
1800 MHz	28.3	37.3	–33.5
1900 MHz	28.4	38.0	–37.7
2000 MHz	28.7	37.6	–40.9
2100 MHz	29.0	38.0	–39.1
2200 MHz	29.0	37.6	–34.1

1. All data measured in fixture with device soldered to heatsink.

OM-400-8
PLASTIC
A3I20X050N

OM-400G-8
PLASTIC
A3I20X050GN

Features

- Integrated Doherty splitter and combiner
- On-chip matching (50 ohm input, DC blocked)
- Integrated quiescent current temperature compensation with enable/disable function (2)

2. Refer to AN1977, *Quiescent Current Thermal Tracking Circuit in the RF Integrated Circuit Family*, and to AN1987, *Quiescent Current Control for the RF Integrated Circuit Device Family.* Go to http://www.nxp.com/RF and search for AN1977 or AN1987.

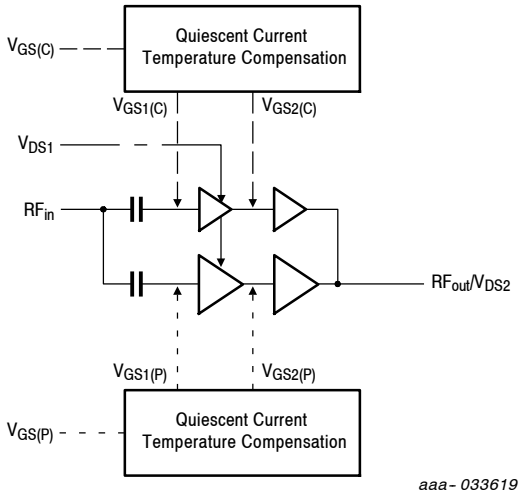
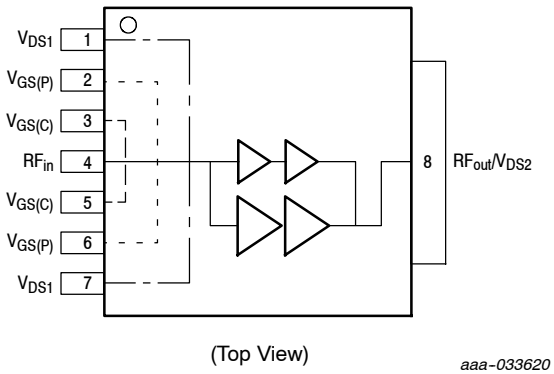


Figure 1. Functional Block Diagram



Note: Exposed backside of the package is the source terminal for the transistor.

Figure 2. Pin Connections

Note: V_{DS1} must be decoupled on the same pin as it is supplied. Do not supply voltage on Pin 1 and decouple on Pin 7 or supply voltage on Pin 7 and decouple on Pin 1. Maximum current allowed between Pin 1 and Pin 7 inside the device is 1.8 A.

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	–0.5, +65	Vdc
Gate-Source Voltage	V_{GS}	–0.5, +10	Vdc
Operating Voltage	V_{DD}	32, +0	Vdc
Storage Temperature Range	T_{stg}	–65 to +150	°C
Case Operating Temperature Range	T_C	–40 to +150	°C
Operating Junction Temperature Range (1,2)	T_J	–40 to +225	°C
Input Power	P_{in}	20	dBm

Table 2. Thermal Characteristics

Characteristic	Symbol	Value (2,3)	Unit
Thermal Resistance, Junction to Case Case Temperature 70°C, 10 W Avg., W-CDMA, 28 Vdc, $I_{DQ1(Carrier)}$ = 28 mA, $I_{DQ2(Carrier)}$ = 133 mA, $V_{GS(Peaking)}$ = 2.05 Vdc, 1840 MHz Stage 1 Stage 2	$R_{\theta JC}$	 7.1 1.9	°C/W

Table 3. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JS-001-2017)	Class 2
Charge Device Model (per JS-002-2014)	Class C2b

Table 4. Moisture Sensitivity Level

Test Methodology	Rating	Package Peak Temperature	Unit
Per JESD22-A113, IPC/JEDEC J-STD-020	3	260	°C

1. Continuous use at maximum temperature will affect MTTF.
2. MTTF calculator available at http://www.nxp.com.
3. Refer to AN1955, *Thermal Measurement Methodology of RF Power Amplifiers.* Go to http://www.nxp.com/RF and search for AN1955.

Table 5. Electrical Characteristics (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Carrier Stage 1 and Stage 2 — Off Characteristics					
Zero Gate Voltage Drain Leakage Current (V_{DS1} = V_{DS2} = 65 Vdc, V_{GS} = 0 Vdc)	$I_{DSS(1+2)}$	—	—	10	μAdc
Zero Gate Voltage Drain Leakage Current (V_{DS1} = V_{DS2} = 32 Vdc, V_{GS} = 0 Vdc)	$I_{DSS(1+2)}$	—	—	1	nAdc
Carrier Stage 1 and Stage 2 — On Characteristics					
Gate Threshold Voltage (V_{DS} = 10 Vdc, I_D = 21 μAdc)	$V_{GSC(th)}$	0.7	1.7	2.4	Vdc
Gate Quiescent Voltage (V_{DS} = 28 Vdc, $I_{DQ(Carrier)}$ = 160 mAdc)	$V_{GSC(Q)}$	—	2.05	—	Vdc
Fixture Gate Quiescent Voltage (V_{DD} = 28 Vdc, $I_{DQ(Carrier)}$ = 160 mAdc, Measured in Functional Test)	$V_{GGC(Q)}$	4.8	5.1	5.5	Vdc
Peaking Stage 1 and Stage 2 — Off Characteristics					
Zero Gate Voltage Drain Leakage Current (V_{DS1} = V_{DS2} = 65 Vdc, V_{GS} = 0 Vdc)	$I_{DSS(1+2)}$	—	—	10	μAdc
Zero Gate Voltage Drain Leakage Current (V_{DS1} = V_{DS2} = 32 Vdc, V_{GS} = 0 Vdc)	$I_{DSS(1+2)}$	—	—	1	nAdc
Peaking Stage 1 and Stage 2 — On Characteristics					
Gate Threshold Voltage (V_{DS1} = V_{DS2} = 10 Vdc, I_D = 36 μAdc)	$V_{GSP(th)}$	0.7	1.7	2.4	Vdc
Drain–Source On–Voltage ($V_{GS2(Peaking)}$ = 10 Vdc, I_D = 360 mAdc) Stage 2	$V_{DS(on)}$	0.05	0.2	0.3	Vdc

(continued)

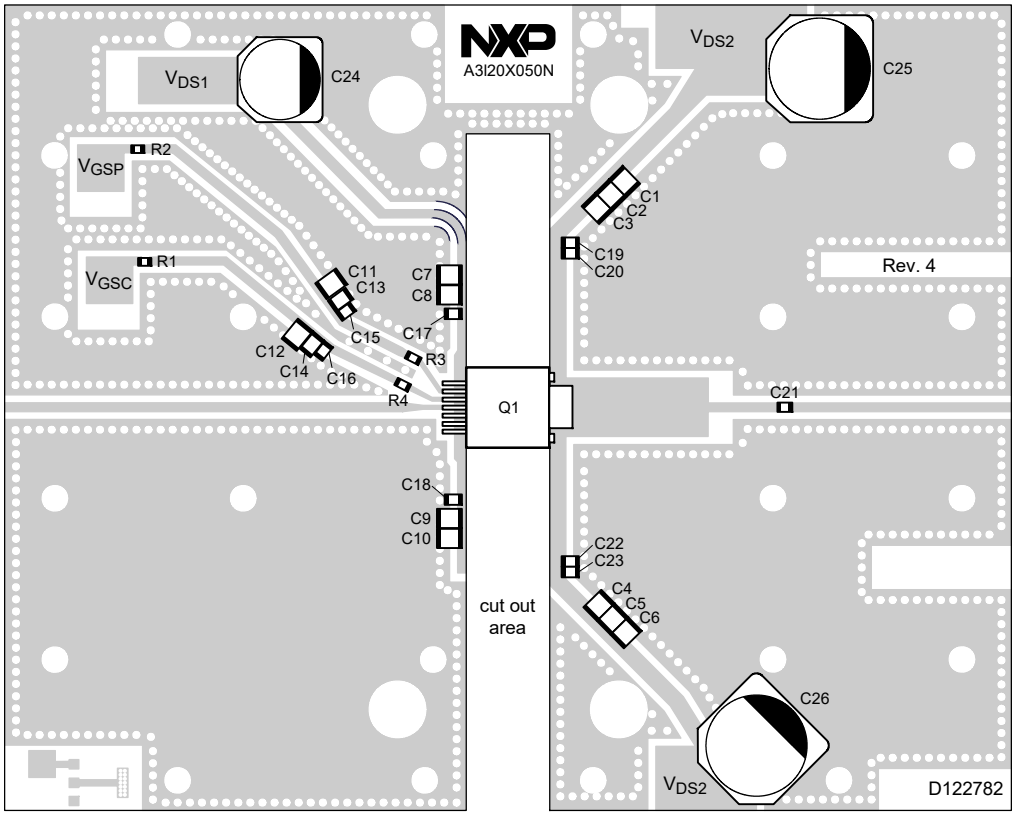
Table 5. Electrical Characteristics (T_A = 25°C unless otherwise noted) **(continued)**

Characteristic	Symbol	Min	Typ	Max	Unit
Functional Tests (1,2) (In NXP Production Test Fixture, 50 ohm system) V_{DD} = 28 Vdc, $I_{DQ(Carrier)}$ = 160 mA, $V_{GS(Peaking)}$ = 2.15 Vdc, P_{out} = 6.3 W Avg., f = 1840 MHz, Single-Carrier W-CDMA, IQ Magnitude Clipping, Input Signal PAR = 9.9 dB @ 0.01% Probability on CCDF. ACPR measured in 3.84 MHz Channel Bandwidth @ ±5 MHz Offset.					
Power Gain	G_{ps}	28.0	29.3	31.0	dB
Power Added Efficiency	PAE	36.7	39.5	—	%
Adjacent Channel Power Ratio	ACPR	—	–37.2	–33.0	dBc
P_{out} @ 3 dB Compression Point, CW	P3dB	57.5	63.1	—	W
Wideband Ruggedness (In NXP Doherty Production Test Fixture, 50 ohm system) $I_{DQ(Carrier)}$ = 160 mA, $V_{GS(Peaking)}$ = 2.15 Vdc, f = 1840 MHz, Additive White Gaussian Noise (AWGN) with 10 dB PAR					
ISBW < 120 MHz	No Device Degradation				
ISBW > 120 MHz	Maintain P_{out} at < 10 dB OBO and V_{DD} at < 30 V				
Typical Performance (3) (In NXP Characterization Test Fixture, 50 ohm system) V_{DD} = 28 Vdc, $I_{DQ(Carrier)}$ = 160 mA, $V_{GS(Peaking)}$ = 2.15 Vdc, 1805–1880 MHz Bandwidth					
P_{out} @ 3 dB Compression Point (4)	P3dB	—	63.0	—	W
AM/PM (Maximum value measured at the P3dB compression point across the 1805–1880 MHz frequency range.)	Φ	—	–19	—	°
VBW Resonance Point (IMD Third Order Intermodulation Inflection Point)	VBW_{res}	—	190	—	MHz
Quiescent Current Accuracy over Temperature (5) with 2 kΩ Gate Feed Resistors (–30 to 85°C) Stage 1+2 (Carrier)	ΔI_{QT}	—	6.5	—	%
Gain Flatness in 75 MHz Bandwidth @ P_{out} = 6.3 W Avg.	G_F	—	0.3	—	dB
Gain Variation over Temperature (–40°C to +85°C)	ΔG	—	0.037	—	dB/°C
Output Power Variation over Temperature (–40°C to +85°C)	ΔP3dB	—	0.009	—	dB/°C

Table 6. Ordering Information

Device	Tape and Reel Information	Package
A3I20X050NR1	R1 Suffix = 500 Units, 32 mm Tape Width, 13-inch Reel	OM-400-8
A3I20X050GNR1		OM-400G-8

1. Part internally input and output matched.
2. Measurements made with device in straight lead configuration before any lead forming operation is applied. Lead forming is used for gull wing (GN) parts.
3. All data measured in fixture with device soldered to heatsink.
4. P3dB = P_{avg} + 7.0 dB where P_{avg} is the average output power measured using an unclipped W-CDMA single-carrier input signal where output PAR is compressed to 7.0 dB @ 0.01% probability on CCDF.
5. Refer to AN1977, *Quiescent Current Thermal Tracking Circuit in the RF Integrated Circuit Family*, and to AN1987, *Quiescent Current Control for the RF Integrated Circuit Device Family.* Go to http://www.nxp.com/RF and search for AN1977 or AN1987.

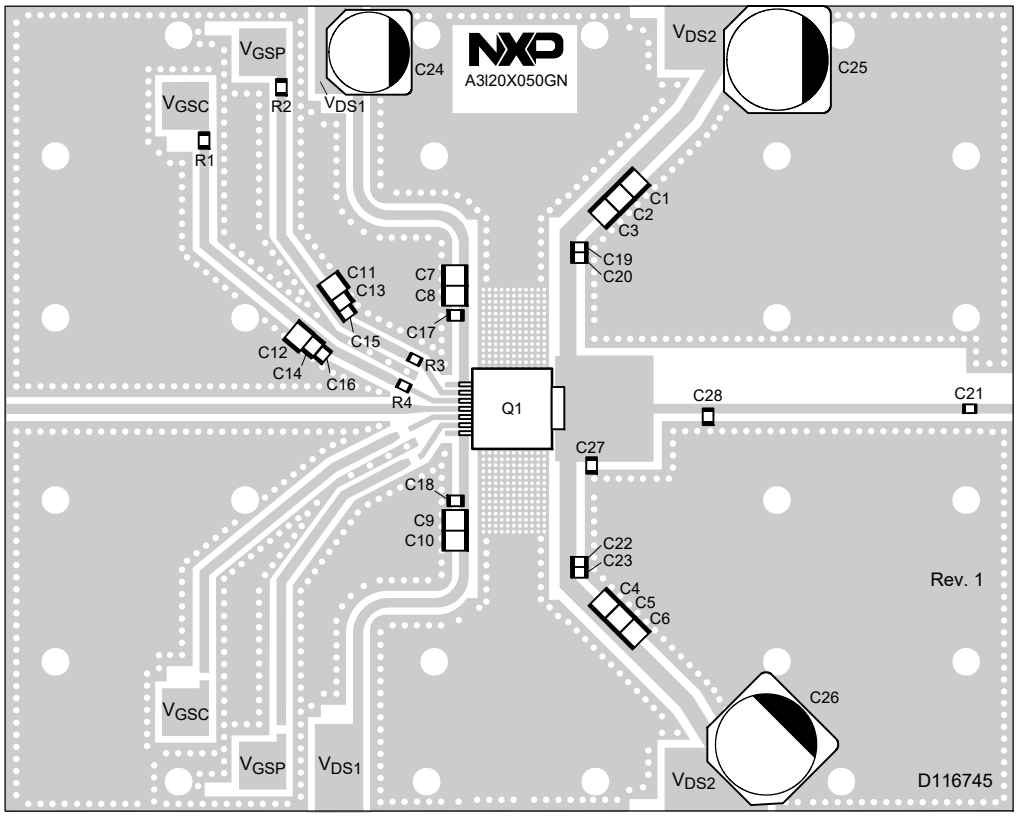


Note: All data measured in fixture with device soldered to heatsink. Production fixture does not include device soldered to heatsink.

Figure 3. A3I20X050N Characterization Test Circuit Component Layout — 1805–1880 MHz

Table 7. A3I20X050N Characterization Test Circuit Component Designations and Values — 1805–1880 MHz

Part	Description	Part Number	Manufacturer
C1, C2, C3, C4, C5, C6, C7, C8, C9, C10, C11, C12	10 μF Chip Capacitor	C3225X7S1H106M250AB	TDK
C13, C14	10 nF Chip Capacitor	C0805C103K5RAC	Kemet
C15, C16, C17, C18, C19, C20, C21, C22, C23	10 pF Chip Capacitor	600S100JT250XT	ATC
C24	150 μF, 100 V Electrolytic Capacitor	EEVFK2A151M	Panasonic
C25, 26	220 μF, 100 V Electrolytic Capacitor	EEVFK2A221M	Panasonic
Q1	RF Power LDMOS Amplifier	A3I20X050N	NXP
R1, R2	2.2 kΩ, 1/8 W Chip Resistor	CRCW08052K20JNEA	Vishay
R3, R4	10 Ω, 1/8 W Chip Resistor	CRCW080510R0FKEA	Vishay
PCB	Rogers RO4350B, 0.020″, ε_r = 3.66	D122782	MTL



Note: All data measured in fixture with device soldered to heatsink.

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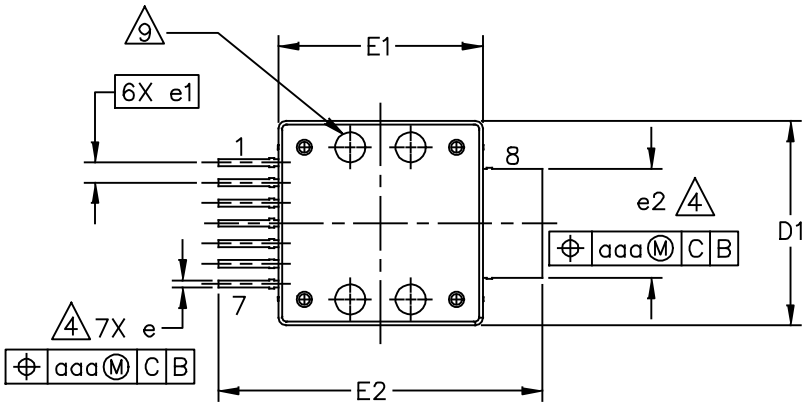
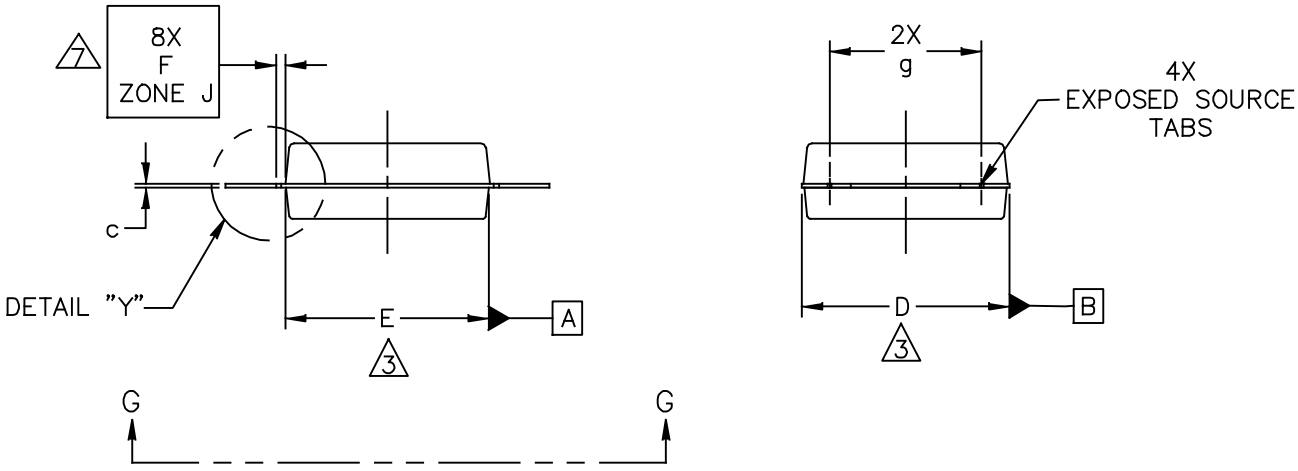
Figure 4. A3I20X050GN Test Circuit Component Layout — 1800–2200 MHz

Table 8. A3I20X050GN Test Circuit Component Designations and Values — 1800–2200 MHz

Part	Description	Part Number	Manufacturer
C1, C2, C3, C4, C5, C6, C7, C8, C9, C10, C11, C12	10 μF Chip Capacitor	C3225X7S1H106M250AB	TDK
C13, C14	10 nF Chip Capacitor	C0805C103K5RAC	Kemet
C15, C16, C17, C18, C19, C20, C21, C22, C23	10 pF Chip Capacitor	600S100JT250XT	ATC
C24	150 μF, 100 V Electrolytic Capacitor	EEVFK2A151M	Panasonic
C25, 26	220 μF, 100 V Electrolytic Capacitor	EEVFK2A221M	Panasonic
C27	0.8 pF Chip Capacitor	06035J0R8BBS	AVX
C28	1.8 pF Chip Capacitor	600S1R8BT250XT	ATC
Q1	RF Power LDMOS Amplifier	A3I20X050GN	NXP
R1, R2	2.2 kΩ, 1/8 W Chip Resistor	CRCW08052K20JNEA	Vishay
R3, R4	10 Ω, 1/8 W Chip Resistor	CRCW080510R0FKEA	Vishay
PCB	Rogers RO4350B, 0.020″, ε_r = 3.66	D116745	MTL

OM-400-8 SOT1981-1





DATE: 29 OCT 2019

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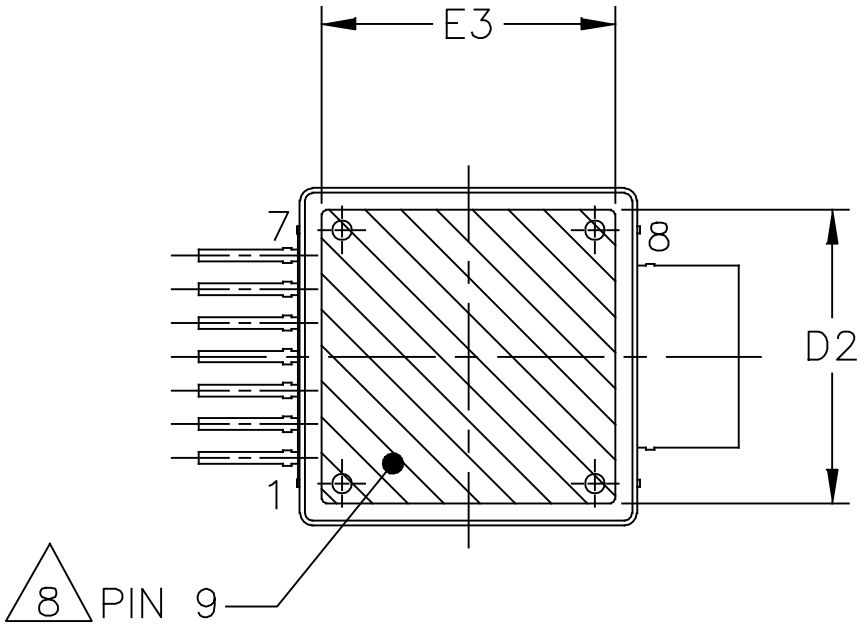
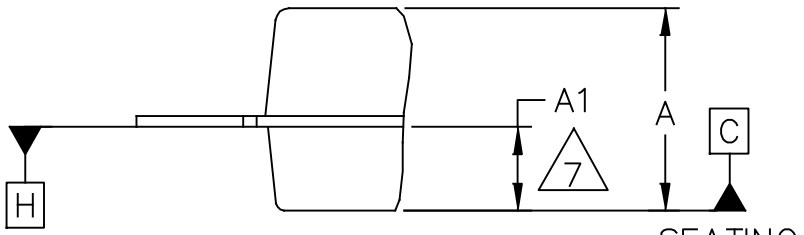


BOTTOM VIEW
VIEW G-G



DETAIL "Y"

DATE: 29 OCT 2019

MECHANICAL OUTLINE PRINT VERSION NOT TO SCALE	STANDARD: NON-JEDEC	DRAWING NUMBER: 98ASA01217D	REVISION: C	PAGE: 2

NOTES:

1. CONTROLLING DIMENSION: INCH

2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M−1994.

3. DIMENSIONS D & E DOES NOT REFLECT PLASTIC OR METAL PROTRUSIONS OF PACKAGE PART LINE. ALLOWABLE PROTRUSION IS .006 INCH (0.15 MM).

4. DIMENSIONS e & e2, DO NOT INCLUDE DAMBAR PROTRUSIONS. ALLOWABLE PROTRUSIONS IS .005 INCH (0.13 MM).

5. DATUM PLANE H IS LOCATE AT THE BOTTOM OF THE LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.

6. DATUMS A AND B TO BE DETERMINED AT DATUM PLANE H.

7. DIMENSION A1 APPLIES WITHIN ZONE J ONLY.

8. HATCHING AREA REPRESENTS EXPOSED AREA OF THE HEATSINK. DIMENSIONS D1 AND E1 REPRESENT THE VALUES BETWEEN THE TWO OPPOSITE POINTS ALONG THE EDGES OF THE EXPOSED AREA OF HEAT SLUG.

9. DIMPLED HOLE REPRESENTS PIN 1.

	INCH		MILLIMETER			INCH		MILLIMETER	
DIM	MIN	MAX	MIN	MAX	DIM	MIN	MAX	MIN	MAX
A	.147	.153	3.73	3.89	e1	.040 BSC		1.02 BSC	
A1	.059	.065	1.50	1.65	e2	.213	.219	5.41	5.56
D	.398	.402	10.11	10.21	c	.007	.009	0.18	0.23
D1	.402	.406	10.21	10.31	g	.295	.305	7.49	7.75
D2	.343	.353	8.71	8.97	aaa	.005		0.13	
E	.398	.402	10.11	10.21					
E1	.402	.406	10.21	10.31					
E2	.636	.644	16.15	16.36					
E3	.343	.353	8.71	8.97					
F	.025 BSC		0.635 BSC						
e	.011	.017	0.28	0.43					

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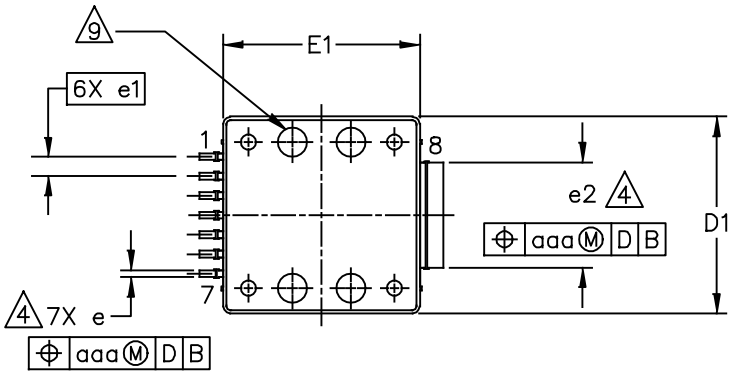

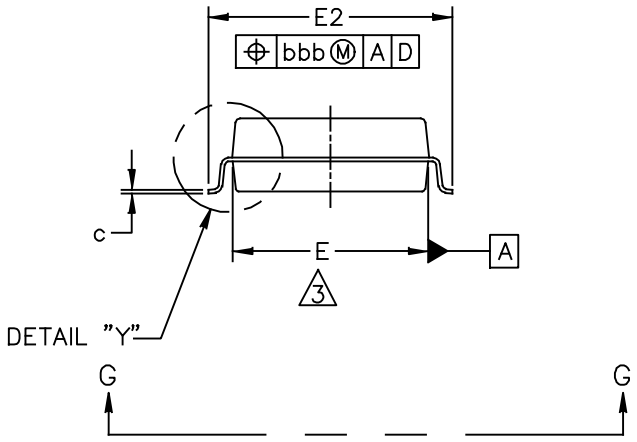

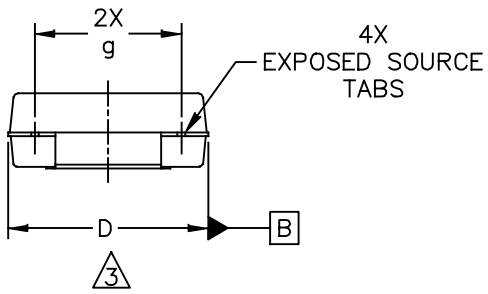

DATE: 12 JUN 2019

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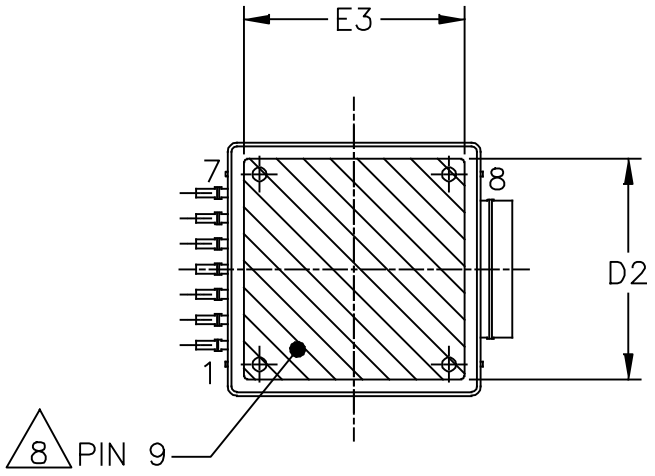
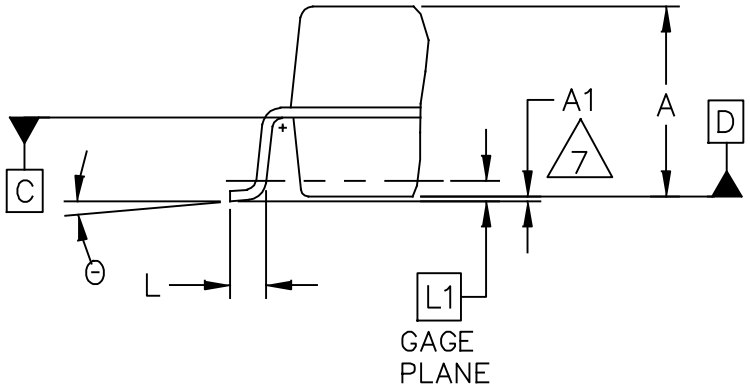


BOTTOM VIEW
VIEW G-G



DETAIL "Y"

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5. DATUM PLANE C IS LOCATE AT THE BOTTOM OF THE LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
6. DATUMS A AND B TO BE DETERMINED AT DATUM PLANE C.
7. DIMENSION A1 IS MEASURED WITH REFERENCE TO DATUM D. THE POSITIVE VALUE IMPLIES THAT THE BOTTOM OF THE PACKAGE IS HIGHER THAN THE BOTTOM OF THE LEAD.
8. HATCHING AREA REPRESENTS EXPOSED AREA OF THE HEATSINK. DIMENSIONS D1 AND E1 REPRESENT THE VALUES BETWEEN THE TWO OPPOSITE POINTS ALONG THE EDGES OF THE EXPOSED AREA OF HEAT SLUG.
9. DIMPLED HOLE REPRESENTS PIN 1.

DIM	INCH MIN	INCH MAX	MILLIMETER MIN	MILLIMETER MAX	DIM	INCH MIN	INCH MAX	MILLIMETER MIN	MILLIMETER MAX
A	.147	.153	3.73	3.89	e	.011	.017	0.28	0.43
A1	.000	.005	0.00	0.13	e1	.040 BSC		1.02 BSC	
D	.398	.402	10.11	10.21	e2	.213	.219	5.41	5.56
D1	.402	.406	10.21	10.31	c	.007	.009	0.18	0.23
D2	.343	.353	8.71	8.97	g	.295	.305	7.49	7.75
E	.398	.402	10.11	10.21	Θ	1°	9°	1°	9°
E1	.402	.406	10.21	10.31	aaa	.005		0.13	
E2	.495	.505	12.57	12.83	bbb	.010		0.25	
E3	.343	.353	8.71	8.97					
L	.026	.032	0.66	0.81					
L1	.010 BSC		0.25 BSC						

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PRODUCT DOCUMENTATION, SOFTWARE AND TOOLS

Refer to the following resources to aid your design process.

Application Notes

- AN1907: Solder Reflow Attach Method for High Power RF Devices in Plastic Packages
- AN1955: Thermal Measurement Methodology of RF Power Amplifiers
- AN1977: Quiescent Current Thermal Tracking Circuit in the RF Integrated Circuit Family
- AN1987: Quiescent Current Control for the RF Integrated Circuit Device Family

Engineering Bulletins

- EB212: Using Data Sheet Impedances for RF LDMOS Devices

Software

- Electromigration MTTF Calculator
- RF High Power Model
- .s2p File

Development Tools

- Printed Circuit Boards

REVISION HISTORY

The following table summarizes revisions to this document.

Revision	Date	Description
0	Oct. 2019	• Initial release of data sheet
1	Dec. 2019	• Table 6, Ordering Information: changed tape and reel suffix to R1 to reflect orderable quantity of 500 units, p. 4 • Package Outline Drawing: OM-400-8 package outline updated to Rev. C, pp. 7–9
2	May 2020	• Wideband Ruggedness table: Ruggedness results were changed based on ISBW. ISBW was split at 120 MHz to differentiate ISBW performance between varying applications, p. 4

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Rev. 2, 05/2020