To our customers,

Old Company Name in Catalogs and Other Documents

On April 1st, 2010, NEC Electronics Corporation merged with Renesas Technology Corporation, and Renesas Electronics Corporation took over all the business of both companies. Therefore, although the old company name remains in this document, it is a valid Renesas Electronics document. We appreciate your understanding.

Renesas Electronics website: http://www.renesas.com

April 1st, 2010
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (http://www.renesas.com)

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BB503C

Built in Biasing Circuit MOS FET IC
UHF RF Amplifier

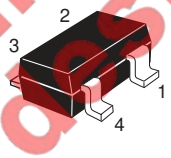
REJ03G0834-0500
(Previous ADE-208-812C)
Rev.5.00
Aug.10.2005

Features

- Built in Biasing Circuit; To reduce using parts cost & PC board space.
- Low noise; NF = 1.8 dB typ. at f = 900 MHz
- High gain; PG = 22 dB typ. at f = 900 MHz
- Withstanding to ESD;
  Built in ESD absorbing diode. Withstand up to 200V at C=200pF, Rs=0 conditions.
- Provide mini mold packages; CMPAK-4(SOT-343mod)

Outline

RENESAS Package code: PTSP0004ZA-A
(Package name: CMPAK-4)



1. Source
2. Gate1
3. Gate2
4. Drain

Notes: 1. Marking is “CS–”.
2. BB503C is individual type number of RENESAS BBFET.

Absolute Maximum Ratings

(Ta = 25°C)

Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DS}	6	V
Gate1 to source voltage	V_{G1S}	+6 –0	V
Gate2 to source voltage	V_{G2S}	+6 –0	V
Drain current	I_D	20	mA
Channel power dissipation	Pch	100	mW
Channel temperature	Tch	150	°C
Storage temperature	Tstg	–55 to +150	°C

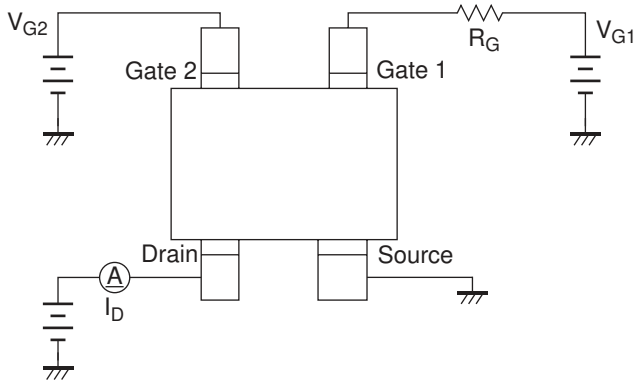
Electrical Characteristics

(Ta = 25°C)

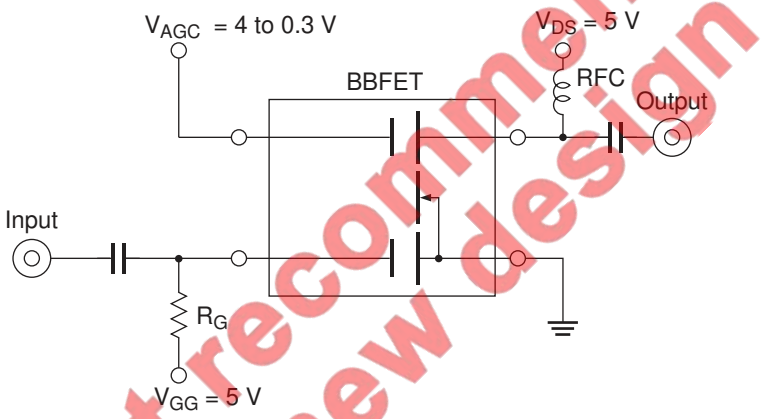
Item	Symbol	Min	Typ	Max	Unit	Test conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	6	—	—	V	I_D = 200 µA, V_{G1S} = V_{G2S} = 0
Gate1 to source breakdown voltage	$V_{(BR)G1SS}$	+6	—	—	V	I_{G1} = +10 µA, V_{G2S} = V_{DS} = 0
Gate2 to source breakdown voltage	$V_{(BR)G2SS}$	+6	—	—	V	I_{G2} = +10 µA, V_{G1S} = V_{DS} = 0
Gate1 to source cutoff current	I_{G1SS}	—	—	+100	nA	V_{G1S} = +5 V, V_{G2S} = V_{DS} = 0
Gate2 to source cutoff current	I_{G2SS}	—	—	+100	nA	V_{G2S} = +5 V, V_{G1S} = V_{DS} = 0
Gate1 to source cutoff voltage	$V_{G1S(off)}$	0.5	0.7	1.0	V	V_{DS} = 5 V, V_{G2S} = 4 V I_D = 100 µA
Gate2 to source cutoff voltage	$V_{G2S(off)}$	0.5	0.7	1.0	V	V_{DS} = 5 V, V_{G1S} = 5 V I_D = 100 µA
Drain current	$I_{D(op)}$	7	10	13	mA	V_{DS} = 5 V, V_{G1} = 5 V V_{G2S} = 4 V, R_G = 47 kΩ
Forward transfer admittance	$\|y_{fs}\|$	19	24	29	mS	V_{DS} = 5 V, V_{G1} = 5 V, V_{G2S} =4 V R_G = 47 kΩ, f = 1 kHz
Input capacitance	Ciss	1.4	1.7	2.0	pF	V_{DS} = 5 V, V_{G1} = 5 V V_{G2S} =4 V, R_G = 47 kΩ f = 1 MHz
Output capacitance	Coss	0.7	1.1	1.5	pF	
Reverse transfer capacitance	Crss	—	0.025	0.05	pF	
Power gain	PG	17	22	—	dB	V_{DS} = 5 V, V_{G1} = 5 V V_{G2S} =4 V, R_G = 47 kΩ f = 900 MHz
Noise figure	NF	—	1.8	2.4	dB	

Main Characteristics

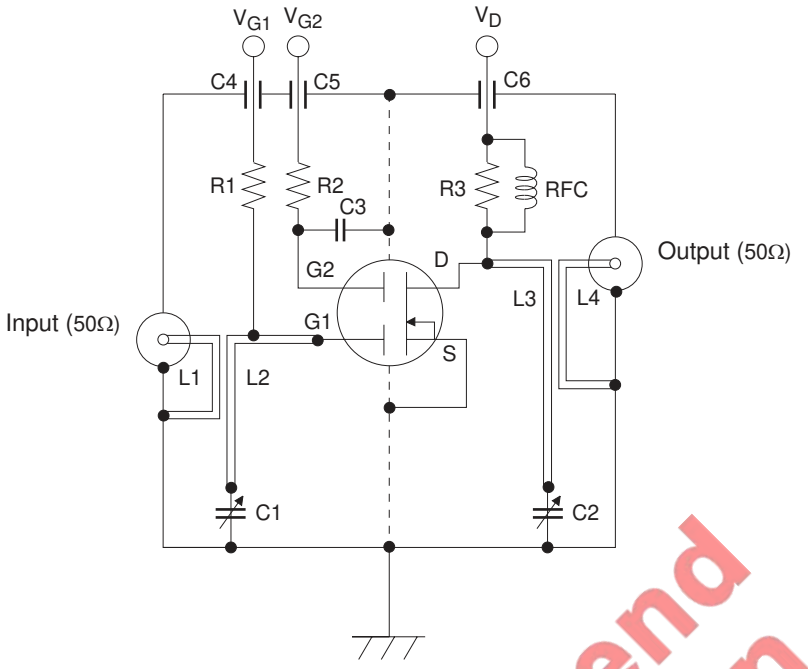
Test Circuit for Operating Items ($I_{D(op)}$, |yfs|, Ciss, Coss, Crss, NF, PG)



Application Circuit

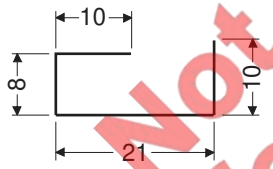


900MHz Power Gain, Noise Figure Test Circuit

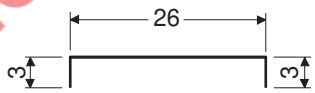


C1, C2 : Variable Capacitor (10pF MAX)
C3 : Disk Capacitor (1000pF)
C4 to C6 : Air Capacitor (1000pF)
R1 : 47 kΩ
R2 : 47 kΩ
R3 : 4.7 kΩ

L1:

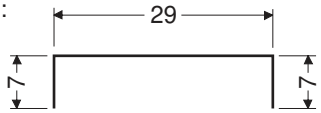


L2:

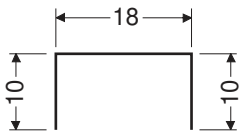


(ϕ1mm Copper wire)
Unit: mm

L3:

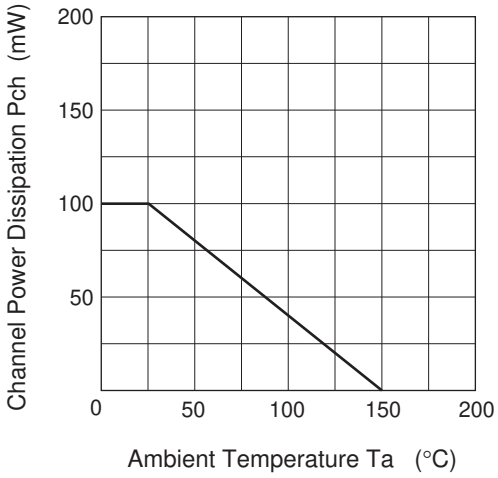


L4:

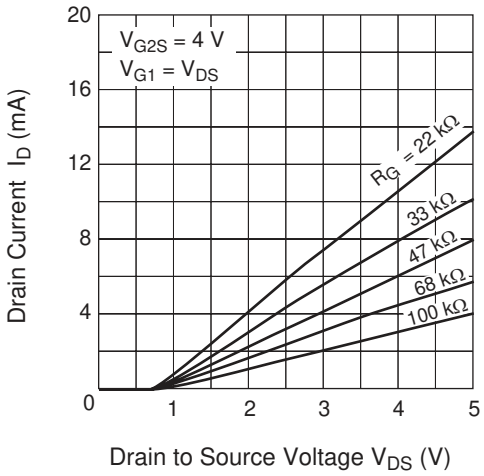


RFC:ϕ1mm Copper wire with enamel 4turns inside dia 6mm

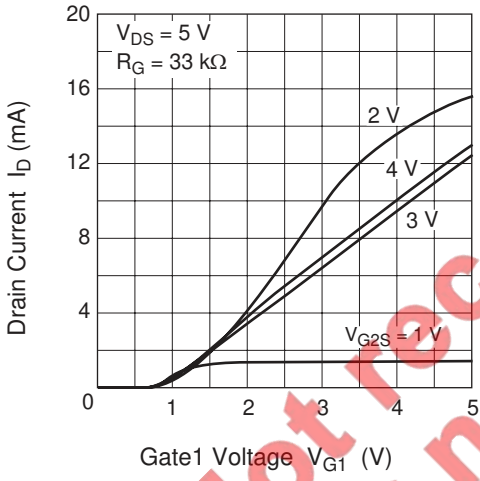
Maximum Channel Power Dissipation Curve



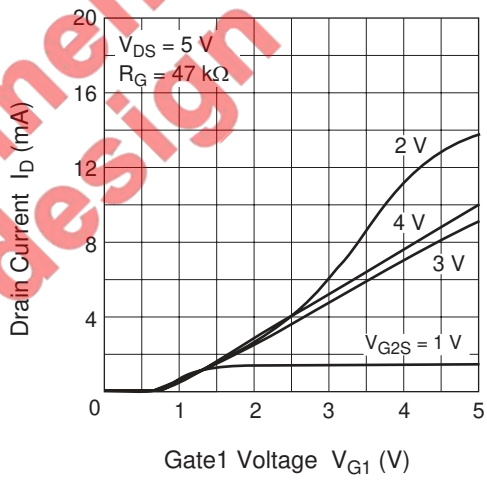
Typical Output Characteristics



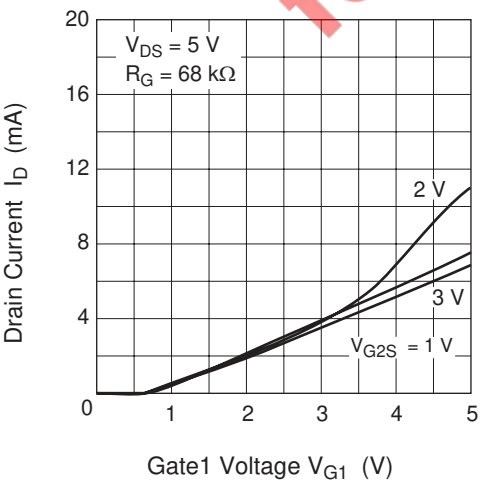
Drain Current vs. Gate1 Voltage



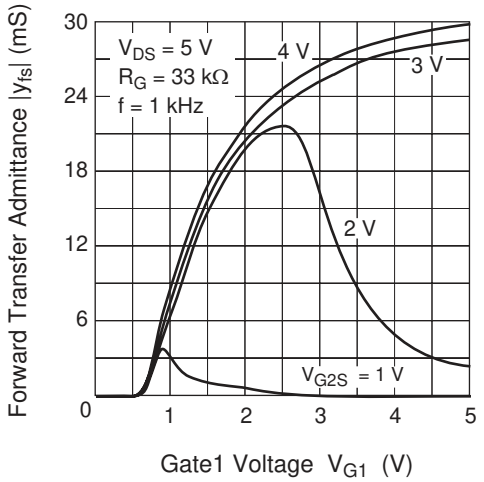
Drain Current vs. Gate1 Voltage



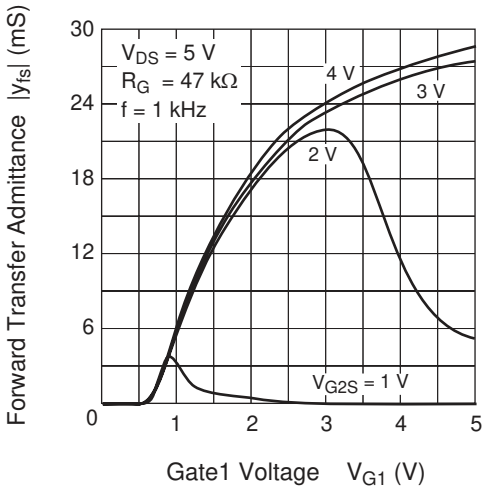
Drain Current vs. Gate1 Voltage



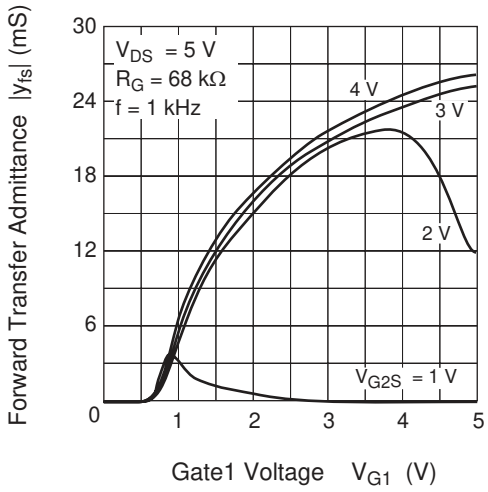
Forward Transfer Admittance vs. Gate1 Voltage



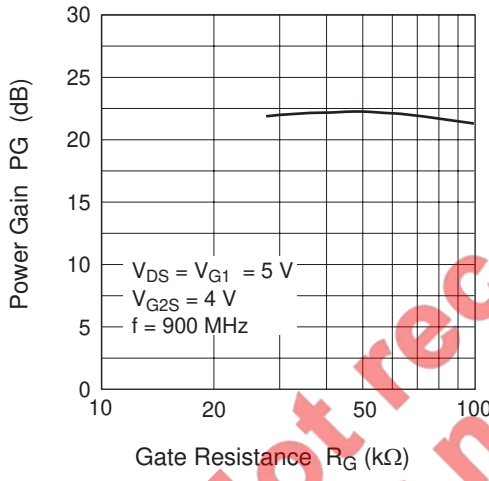
Forward Transfer Admittance vs. Gate1 Voltage



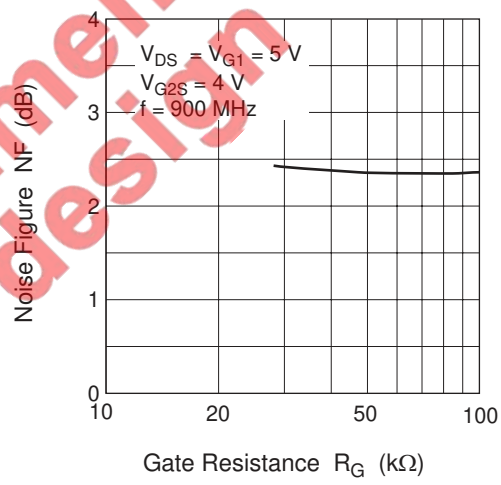
Forward Transfer Admittance vs. Gate1 Voltage



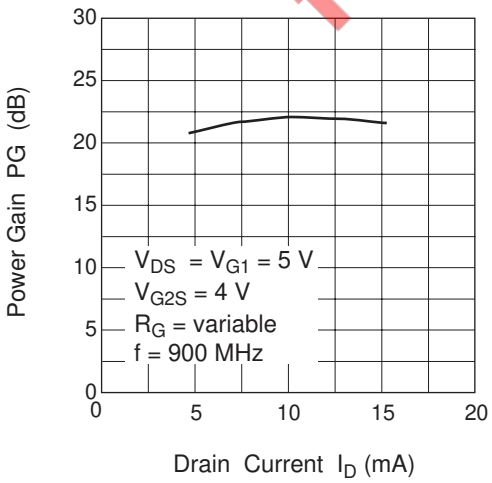
Power Gain vs. Gate Resistance



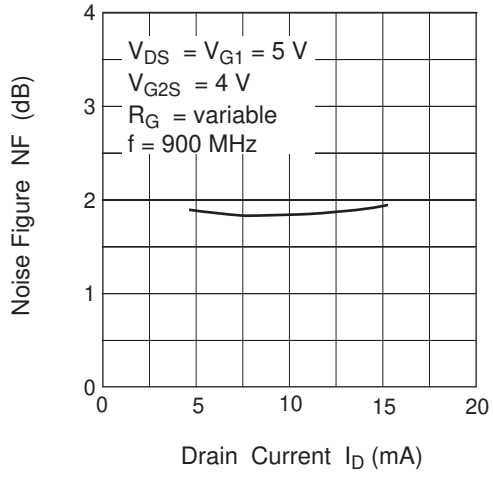
Noise Figure vs. Gate Resistance



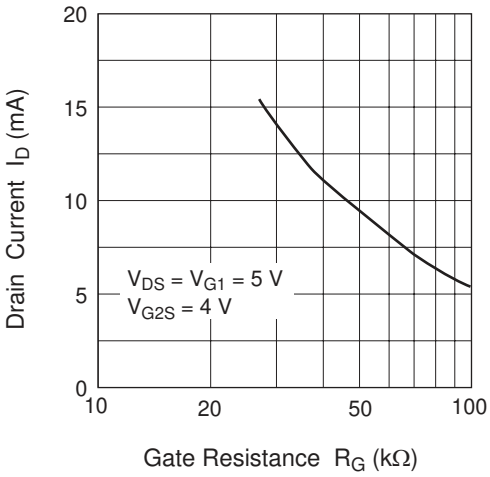
Power Gain vs. Drain Current



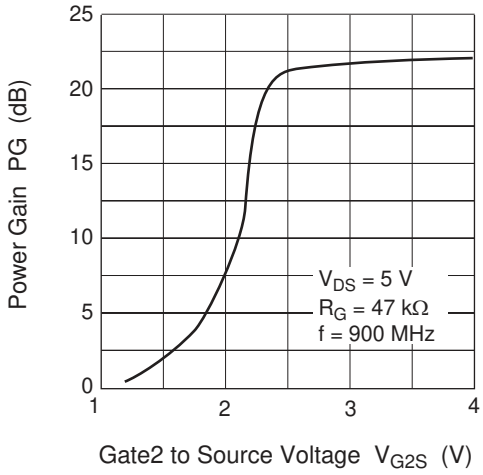
Noise Figure vs. Drain Current



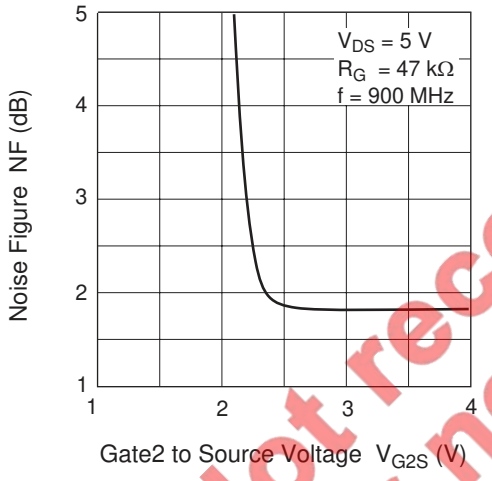
Drain Current vs. Gate Resistance



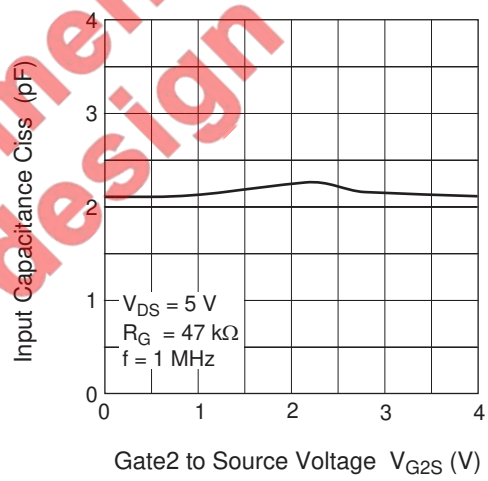
Power Gain vs.
Gate2 to Source Voltage



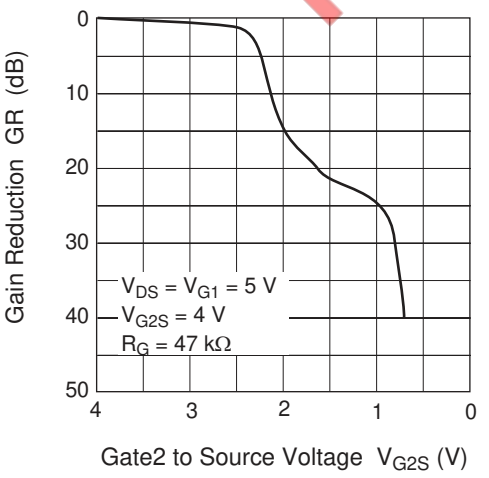
Noise Figure vs.
Gate2 to Source Voltage



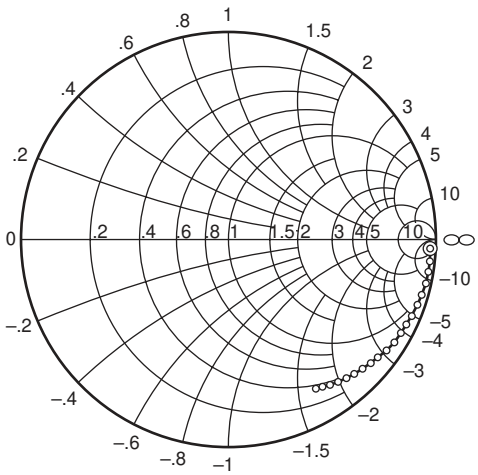
Input Capacitance vs.
Gate2 to Source Voltage



Gain Reduction vs.
Gate2 to Source Voltage



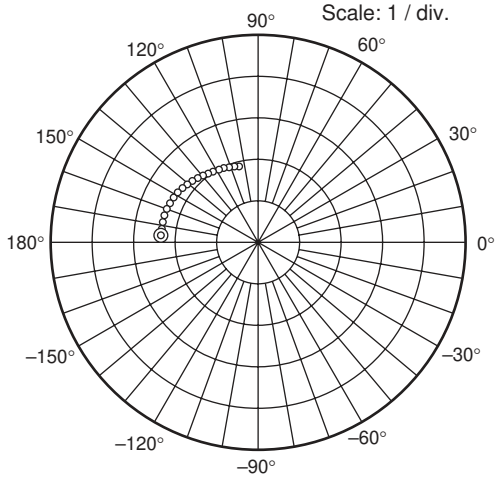
S11 Parameter vs. Frequency



Test Condition: V_{DS} = 5 V , V_{G1} = 5 V
V_{G2S} = 4 V , R_G = 47 kΩ ,
Zo = 50Ω

50 to 1000 MHz (50 MHz step)

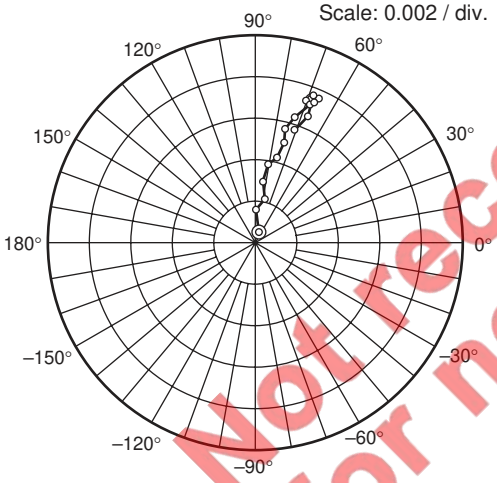
S21 Parameter vs. Frequency



Test Condition: V_{DS} = 5 V , V_{G1} = 5 V
V_{G2S} = 4 V , R_G = 47 kΩ ,
Zo = 50Ω

50 to 1000 MHz (50 MHz step)

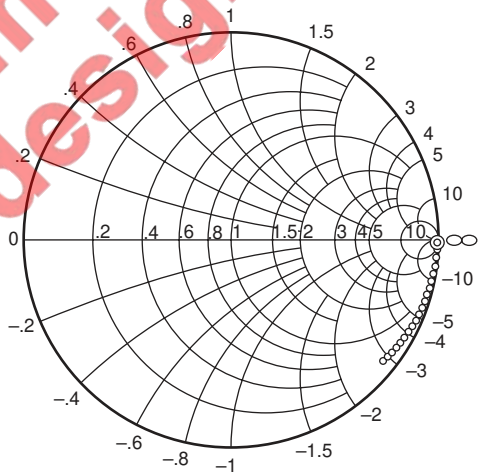
S12 Parameter vs. Frequency



Test Condition: V_{DS} = 5 V , V_{G1} = 5 V
V_{G2S} = 4 V , R_G = 47 kΩ ,
Zo = 50Ω

50 to 1000 MHz (50 MHz step)

S22 Parameter vs. Frequency



Test Condition: V_{DS} = 5 V , V_{G1} = 5 V
V_{G2S} = 4 V , R_G = 47 kΩ ,
Zo = 50Ω

50 to 1000 MHz (50 MHz step)

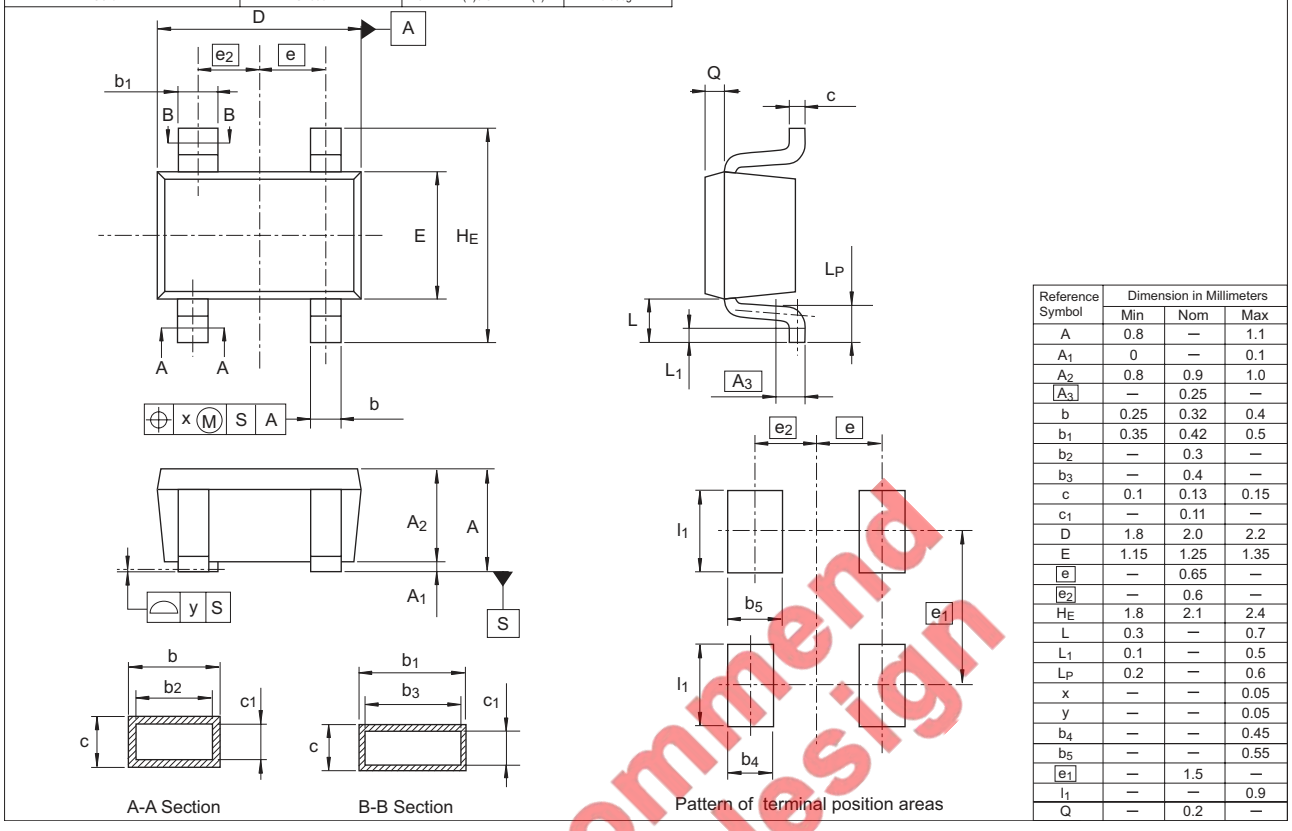
S Parameter

(V_{DS} = V_{G1} = 5V, V_{G2S} = 4V, R_G = 47kΩ, Zo = 50Ω)

f(MHz)	S11		S21		S12		S22	
	MAG.	ANG.	MAG.	ANG.	MAG.	ANG.	MAG.	ANG.
50	0.975	–2.6	2.37	176.1	0.00097	74.4	0.995	–1.9
100	0.977	–6.5	2.37	172.1	0.00162	89.8	0.998	–3.9
150	0.975	–9.1	2.36	168.0	0.00222	78.2	0.997	–5.8
200	0.972	–12.4	2.33	163.8	0.00282	83.8	0.996	–8.0
250	0.968	–15.6	2.32	159.9	0.00388	81.1	0.994	–10.0
300	0.963	–18.9	2.30	156.0	0.00437	76.0	0.993	–11.8
350	0.954	–22.2	2.28	151.8	0.00518	73.6	0.991	–13.9
400	0.946	–25.3	2.25	148.2	0.00567	75.6	0.989	–15.8
450	0.937	–28.2	2.22	144.1	0.00631	72.5	0.986	–17.8
500	0.930	–31.5	2.19	140.2	0.00637	72.7	0.984	–19.6
550	0.920	–34.7	2.16	136.3	0.00720	70.3	0.981	–21.6
600	0.914	–37.4	2.13	132.7	0.00747	67.0	0.978	–23.4
650	0.902	–40.4	2.09	129.3	0.00738	69.2	0.975	–25.4
700	0.886	–43.5	2.07	125.4	0.00758	68.6	0.972	–27.3
750	0.879	–46.1	2.03	122.0	0.00757	66.0	0.968	–29.0
800	0.873	–48.9	1.99	118.3	0.00729	67.5	0.966	–31.0
850	0.857	–52.0	1.96	114.9	0.00723	68.8	0.962	–32.9
900	0.845	–54.5	1.93	111.4	0.00706	68.3	0.959	–34.8
950	0.838	–57.2	1.90	108.1	0.00659	67.5	0.954	–36.6
1000	0.824	–59.6	1.86	104.9	0.00574	71.0	0.952	–38.5

Package Dimensions

JEITA Package Code	RENESAS Code	Package Name	MASS[Typ.]
SC-82A	PTSP0004ZA-A	CMPAK-4(T) / CMPAK-4(T)V	0.006g



Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	0.8	—	1.1
A_1	0	—	0.1
A_2	0.8	0.9	1.0
A_3	—	0.25	—
b	0.25	0.32	0.4
b_1	0.35	0.42	0.5
b_2	—	0.3	—
b_3	—	0.4	—
c	0.1	0.13	0.15
c_1	—	0.11	—
D	1.8	2.0	2.2
E	1.15	1.25	1.35
e	—	0.65	—
e_2	—	0.6	—
H_E	1.8	2.1	2.4
L	0.3	—	0.7
L_1	0.1	—	0.5
L_P	0.2	—	0.6
x	—	—	0.05
y	—	—	0.05
b_4	—	—	0.45
b_5	—	—	0.55
e_1	—	1.5	—
l_1	—	—	0.9
Q	—	0.2	—

Ordering Information

Part Name	Quantity	Shipping Container
BB503CCS-TL-E	3000	ϕ 178 mm Reel, 8 mm Emboss Taping

Note: For some grades, production may be terminated. Please contact the Renesas sales office to check the state of production before ordering the product.

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RENESAS SALES OFFICES

http://www.renesas.com

Refer to "**http://www.renesas.com/en/network**" for the latest and detailed information.

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