High-Performance, 24 Bit, 216 kHz Sampling, Stereo Audio Analog-to-Digital Converter

Check for Samples: PCM4202-EP

FEATURES

- Controlled Baseline
  - One Assembly/Test Site, One Fabrication Site
- Extended Temperature Performance of –40°C to 85°C
- Enhanced Diminishing Manufacturing Sources (DMS) Support
- Enhanced Product-Change Notification
- Qualification Pedigree

Component qualification in accordance with JEDEC and industry standards to ensure reliable operation over an extended temperature range. This includes, but is not limited to, Highly Accelerated Stress Test (HAST) or biased 85/85, temperature cycle, autoclave or unbiased HAST, electromigration, bond intermetallic life, and mold compound life. Such qualification testing should not be viewed as justifying use of this component beyond specified performance and environmental limits.

- Two High-Performance, Delta-Sigma Analog-to-Digital Converters
  - 24 Bit Linear PCM or 1 Bit Direct Stream Digital (DSD) Output Data
  - Supports PCM Output Sampling Rates up to 216 kHz
  - Supports 64 f_S and 128 f_S DSD Output Data Rates
- Dynamic Performance: PCM Output
  - Dynamic Range (V_{IN} = –60 dBF_S, f_{IN} = 1 kHz, A-Weighted): 118 dB
  - THD+N (V_{IN} = –0.5 dB, f_{IN} = 1 kHz): –105 dB
- Dynamic Performance: DSD Output, 64 f_S
  - Dynamic Range (A-Weighted): 115 dB
  - THD+N (V_{IN} = –0.5 dB, f_{IN} = 1 kHz): –102 dB
- Audio Serial Port
  - 24 Bit Linear PCM Output Data
  - Master or Slave Mode Operation
  - Supports Left-Justified, Right-Justified, and $I^2S^®$ Data Formats
- Additional PCM Output Features:
  - Linear-Phase Digital Decimation Filter
  - Digital High-Pass Filter for DC Removal
  - Clipping Flag Output for Each Channel
- Power Supplies: 5 V Analog and 3.3 V Digital
- Power Dissipation:
  - f_S = 48 kHz: 308 mW typical
  - f_S = 96 kHz: 338 mW typical
  - f_S = 192 kHz: 318 mW typical
- Power-Down Mode
- Available in a SSOP-28 Package
- Pin- and Function-Compatible with the PCM1804

APPLICATIONS

- Digital Recorders and Mixing Desks
- Digital Audio Effects Processors
- Broadcast Studio Equipment
- Surround-Sound Encoders
- High-End A/V Receivers

DESCRIPTION

The PCM4202 is a high-performance, stereo audio analog-to-digital (A/D) converter designed for professional and broadcast audio applications. The PCM4202 architecture utilizes a 1 bit delta-sigma modulator per channel, incorporating a novel density modulated dither scheme for improved dynamic performance.

The PCM4202 supports 24 bit linear PCM output data, with sampling frequencies up to 216 kHz. The PCM4202 can also be configured to output either 64× or 128× oversampled, 1 bit direct stream digital (DSD) data for each channel. Support for PCM and DSD output formats makes the PCM4202 suitable for a variety of digital audio recording and processing applications.

The PCM4202 includes a flexible audio serial port interface, which supports standard audio data formats. Audio data format selection, sampling mode configuration, and high-pass filter functions are all programmed using dedicated control pins.

The PCM4202 operates from a 5 V analog power supply and a 3.3 V digital power supply. The digital I/O pins are compatible with 3.3 V logic families. The PCM4202 is available in a small SSOP-28 package.

ORDERING INFORMATION(1)

PRODUCT	PACKAGE-LEAD	PACKAGE DESIGNATOR	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
PCM4202	SSOP-28	DB	–40°C to 85°C	PCM4202EP	PCM4202IDBREP	Tape and Reel, 1000

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range (unless otherwise noted)

		PCM4202	UNIT
Supply voltage	V_{CC}	6.0	V
	V_{DD}	3.6	V
Ground voltage difference	Any AGND to DGND	±0.1	V
Digital input voltage	FMT0, FMT1, S/$\overline{M}$, FS0, FS1, FS2, SCKI, $\overline{RST}$, HPFD, BCK, LRCK	–0.3 to (V_{DD} + 0.3)	V
Analog input voltage	V_{IN}L+, V_{IN}L–, V_{IN}R+, V_{IN}R–	–0.3 to (V_{CC} + 0.3)	V
Input current (any pin except supplies)		±10	mA
Operating temperature range		–40 to 85	°C
Storage temperature range, T_{STG}		–65 to 150	°C

(1) Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.

ELECTRICAL CHARACTERISTICS

All parameters are specified at T_A = 25°C with V_{CC} = 5 V, V_{DD} = 3.3 V (unless otherwise noted), and a measurement bandwidth from 20 Hz to 20 kHz, unless otherwise noted. System clock frequency is equal to 256 f_S for Single and Dual Rate sampling modes, and 128 f_S for Quad Rate sampling mode.

PARAMETER		TEST CONDITIONS	PCM4202 MIN	PCM4202 TYP	PCM4202 MAX	UNIT
RESOLUTION				24		Bits
AUDIO DATA FORMAT						
Linear PCM interface formats		Two's complement, MSB first data		I^2S, Left or Right Justified		
Linear PCM word length				24		Bits
Direct Stream Digital (DSD) output				1		Bit
DIGITAL CHARACTERISTICS						
Input logic level	V_{IH}		0.7 × V_{DD}		V_{DD}	V
	V_{IL}		0		0.3 × V_{DD}	V
Output logic level	V_{OH}	I_{OH} = –2 mA	0.8 × V_{DD}			V
	V_{OL}	I_{OL} = 2 mA			0.2 × V_{DD}	V
Input current	I_{IH}	V_{IN} = V_{DD} (– 40°C to 85°C)			10	µA
	I_{IL}	V_{IN} = 0 V (– 40°C to 85°C)			–10	µA
Input current(1)	I_{IH}	V_{IN} = V_{DD} (– 40°C to 85°C)			25	µA
	I_{IL}	V_{IN} = 0 V (– 40°C to 85°C)			–25	µA
Sampling frequency(2)	f_S	Single rate	8		54	kHz
		Dual rate	54		108	
		Quad rate	108		216	
System clock duty cycle			45	50	55	%
System clock frequency(2)		Single rate, SCKI = 256f_S	2.048		13.824	MHz
		Single rate, SCKI = 384f_S	3.072		20.736	MHz
		Single rate, SCKI = 512f_S	4.096		27.648	MHz
		Single rate, SCKI = 768f_S	6.144		38.4	MHz
		Dual rate, SCKI = 256f_S	13.824		27.648	MHz
		Dual rate, SCKI = 384f_S	20.736		38.4	MHz
		Quad rate, SCKI = 128f_S	13.824		27.648	MHz
		Quad rate, SCKI = 192f_S	20.736		38.4	MHz
ANALOG INPUTS						
Input voltage, full-scale		Differential input		6		V_{PP}
Input impedance				3		kΩ
Common-mode rejection				85		dB
DC PERFORMANCE						
Output offset error		HPFD = 1		±4		% of FSR
Gain error				±4		% of FSR
Gain mismatch channel-to-channel				±3		% of FSR

(1) Applies to the $\overline{RST}$ input, pin 19.
(2) Single, Dual, and Quad Rate sampling modes are described within this data sheet.

ELECTRICAL CHARACTERISTICS (continued)

All parameters are specified at T_A = 25°C with V_{CC} = 5 V, V_{DD} = 3.3 V (unless otherwise noted), and a measurement bandwidth from 20 Hz to 20 kHz, unless otherwise noted. System clock frequency is equal to 256 f_S for Single and Dual Rate sampling modes, and 128 f_S for Quad Rate sampling mode.

PARAMETER		TEST CONDITIONS	PCM4202			UNIT
			MIN	TYP	MAX	
DYNAMIC PERFORMANCE[3]						
f_S = 48 kHz, Single Rate		BW = 20 Hz to 20 kHz				
Total harmonic distortion + noise	THD+N	V_{IN} = –0.5 dBFS, f_{IN} = 1 kHz		–105	–95	dB
		V_{IN} = –0.5 dBFS, f_{IN} = 1 kHz (–40°C to 85°C)			–90	
Dynamic range		V_{IN} = –60 dBFS, f_{IN} = 1 kHz, A-Weighted	112	118		dB
		V_{IN} = –60 dBFS, f_{IN} = 1 kHz, A-Weighted (–40°C to 85°C)	108			
Dynamic range, no weighting		V_{IN} = –60 dBFS, f_{IN} = 1 kHz		116		dB
Channel separation		(–40°C to 85°C)	100	120		dB
f_S = 96 kHz, Dual Rate		BW = 20 Hz to 40 kHz				
Total harmonic distortion + noise	THD+N	V_{IN} = –0.5 dBFS, f_{IN} = 1 kHz		–105		dB
Dynamic range		V_{IN} = –60 dBFS, f_{IN} = 1 kHz, A-Weighted		118		dB
Dynamic range, no weighting		V_{IN} = –60 dBFS, f_{IN} = 1 kHz		112		dB
Channel separation				120		dB
f_S = 192 kHz, Quad Rate		BW = 20 Hz to 40 kHz				
Total harmonic distortion + noise	THD+N	V_{IN} = –0.5 dBFS, f_{IN} = 1 kHz		–103		dB
Dynamic range		V_{IN} = 0 V_{RMS}, A-Weighted		117		dB
Dynamic range, no weighting		V_{IN} = 0 V_{RMS}		108		dB
Channel separation				120		dB
DSD Output, 64 f_S Rate		DSDBCK = 2.8224 MHz				
Total harmonic distortion + noise	THD+N	V_{IN} = –0.5 dBFS, f_{IN} = 1 kHz		–102		dB
Dynamic range		V_{IN} = –60 dBFS, f_{IN} = 1 kHz, A-Weighted		115		dB
Channel separation				120		dB
DSD Output, 128 f_S Rate		DSDBCK = 5.6448 MHz				
Total harmonic distortion + noise	THD+N	V_{IN} = –0.5 dBFS, f_{IN} = 1 kHz		–105		dB
Dynamic range		V_{IN} = –60 dBFS, f_{IN} = 1 kHz, A-Weighted		118		dB
Channel separation				120		dB
DIGITAL DECIMATION FILTER						
Passband edge		Single and Dual Rate			0.453 f_S	Hz
Passband ripple		Single and Dual Rate			�0.005	dB
Passband edge		Single and Dual Rate	0.547 f_S			Hz
Stop band attenuation		Single and Dual Rate	–100			dB
Group delay		Single and Dual Rate		37/f_S		sec
Passband edge (–0.005 dB)		Quad Rate			0.375 f_S	Hz
–3 dB cutoff frequency		Quad Rate			0.490 f_S	Hz
Passband ripple		Quad Rate			±0.005	dB
Passband edge		Quad Rate	0.770 f_S			Hz
Stop band attenuation		Quad Rate	–135			dB

(3) Dynamic performance parameters are measured using an Audio Precision System Two Cascade or Cascade Plus test system. The measurement bandwidth is limited by using the Audio Precision 22 Hz high-pass filter in combination with the Audio Precision 20 kHz, f_S/2, or a user-defined 40 kHz low-pass filter. All A-weighted measurements are performed using the Audio Precision A-weighting filter in combination with the previously mentioned filters.

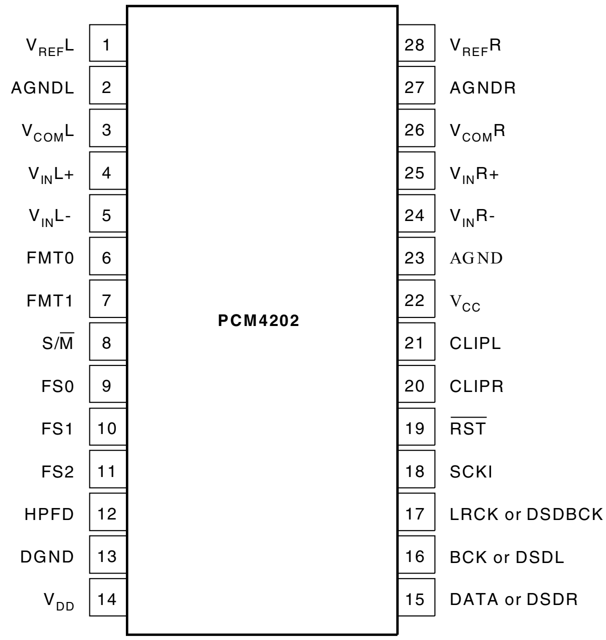
ELECTRICAL CHARACTERISTICS (continued)

All parameters are specified at T_A = 25°C with V_{CC} = 5 V, V_{DD} = 3.3 V (unless otherwise noted), and a measurement bandwidth from 20 Hz to 20 kHz, unless otherwise noted. System clock frequency is equal to 256 f_S for Single and Dual Rate sampling modes, and 128 f_S for Quad Rate sampling mode.

PARAMETER		TEST CONDITIONS	PCM4202 MIN	PCM4202 TYP	PCM4202 MAX	UNIT
Group delay		Quad Rate		9.5/f_S		sec
DIGITAL HIGH PASS FILTER						
Frequency response (–3 dB)				f_S/48000		Hz
POWER SUPPLY						
Voltage range	V_{CC}		4.75	5	5.25	V
	V_{DD}		3	3.3	3.6	V
Operating supply current	I_{CC}	V_{CC} = 5 V, V_{DD} = 3.3 V				
		f_S = 48 kHz, Single Rate		55	65	mA
		f_S = 48 kHz, Single Rate (–40°C to 85°C)			70	
		f_S = 96 kHz, Dual Rate		55	65	mA
		f_S = 96 kHz, Dual Rate (–40°C to 85°C)			70	
		f_S = 192 kHz, Quad Rate		55	65	mA
		f_S = 192 kHz, Quad Rate(–40°C to 85°C)			70	mA
	I_{DD}	V_{CC} = 5 V, V_{DD} = 3.3 V				
		f_S = 48 kHz, Single Rate(–40°C to 85°C)		10	12	mA
		f_S = 96 kHz, Dual Rate(–40°C to 85°C)		19	25	mA
		f_S = 192 kHz, Quad Rate(–40°C to 85°C)		13	15	mA
Power–down mode current		V_{CC} = 5 V, V_{DD} = 3.3 V, $\overline{RST}$ = 0				
	I_{CC}	Clocks applied (–40°C to 85°C)			10	mA
	I_{DD}	Clocks applied (–40°C to 85°C)			2	mA
Total power dissipation		V_{CC} = 5 V, V_{DD} = 3.3 V				
		f_S = 48 kHz, Single Rate		308	365	mW
		f_S = 96 kHz, Dual Rate		338	408	mW
		f_S = 192 kHz, Quad Rate		318	375	mW

PIN ASSIGNMENTS

DB PACKAGE
(TOP VIEW)



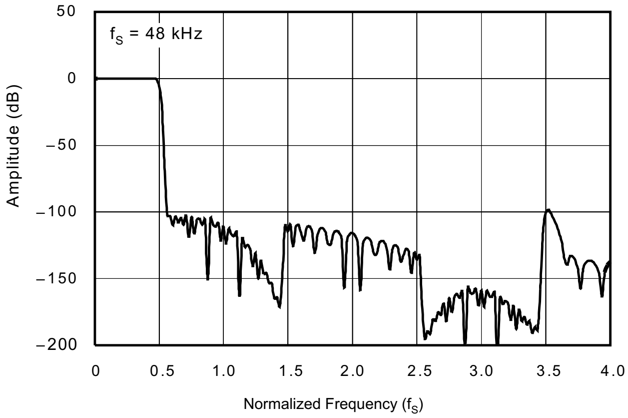
TERMINAL FUNCTIONS

TERMINAL		I/O	DESCRIPTION
PIN NO.	NAME		
1	$V_{REF}L$	Output	Left Channel Voltage Reference
2	AGNDL	Ground	Left Channel Reference Ground
3	$V_{COM}L$	Output	Left Channel DC Common-mode Voltage, 2.5 V Typical
4	$V_{IN}L+$	Input	Left Channel Non-inverting Analog Input
5	$V_{IN}L–$	Input	Left Channel Inverting Analog Input
6	FMT0	Input	Audio Data Format Selection
7	FMT1	Input	Audio Data Format Selection
8	$S/\overline{M}$	Input	Audio Serial Port Slave/Master Mode Selection (0 = Master, 1 = Slave)
9	FS0	Input	Sampling Mode Selection
10	FS1	Input	Sampling Mode Selection
11	FS2	Input	Sampling Mode Selection
12	HPFD	Input	High-pass Filter Disable (Active High)
13	DGND	Ground	Digital Ground
14	V_{DD}	Power	Digital Power Supply, 3.3 V
15	DATA or DSDR	Output	Audio Serial Port Left and Right Channel PCM Data or Right Channel DSD Data
16	BCK or DSDL	I/O	Audio Serial Port Bit (or Data) Clock or Left Channel DSD Data Output
17	LRCK or DSDBCK	I/O	Audio Serial Port Left/Right (or Word) Clock or DSD Data Clock Output
18	SCKI	Input	System Clock
19	$\overline{RST}$	Input	Reset/Power-down (Active Low with internal pull-up)
20	CLIPR	Output	Right Channel Clipping Flag (Active High)
21	CLIPL	Output	Left Channel Clipping Flag (Active High)
22	V_{CC}	Power	Analog Power Supply, 5 V
23	AGND	Ground	Analog Ground
24	$V_{IN}R–$	Input	Right Channel Inverting Analog Input
25	$V_{IN}R+$	Input	Right Channel Non–inverting Analog Input
26	$V_{COM}R$	Output	Right Channel DC Common–mode Voltage, 2.5 V Typical
27	AGNDR	Ground	Right Channel Reference Ground
28	$V_{REF}R$	Output	Right Channel Voltage Reference

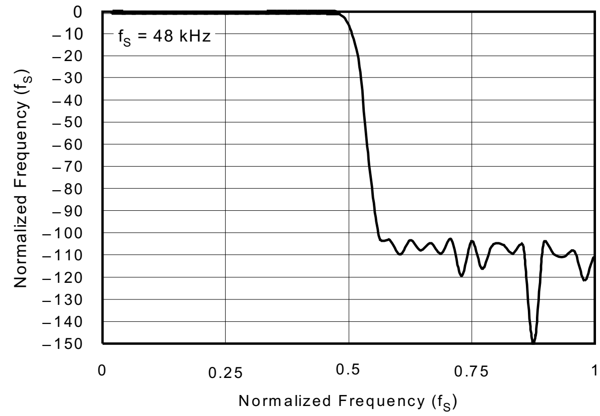
TYPICAL CHARACTERISTICS

All parameters are specified at T_A = 25°C with V_{CC} = 5 V, V_{DD} = 3.3 V, and a measurement bandwidth from 20 Hz to 20 kHz, unless otherwise noted.

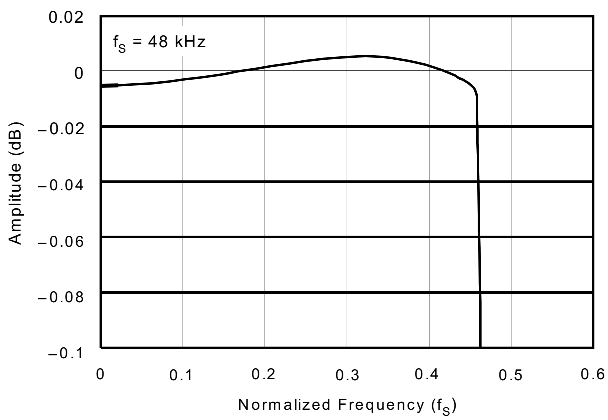
OVERALL CHARACTERISTICS
SINGLE RATE FILTER



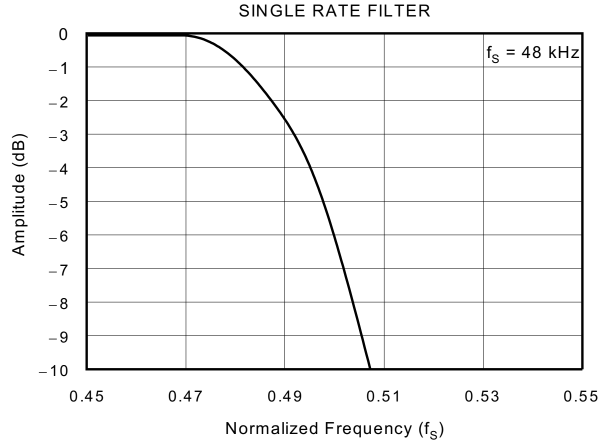
STOP BAND ATTENUATION CHARACTERISTICS
SINGLE RATE FILTER



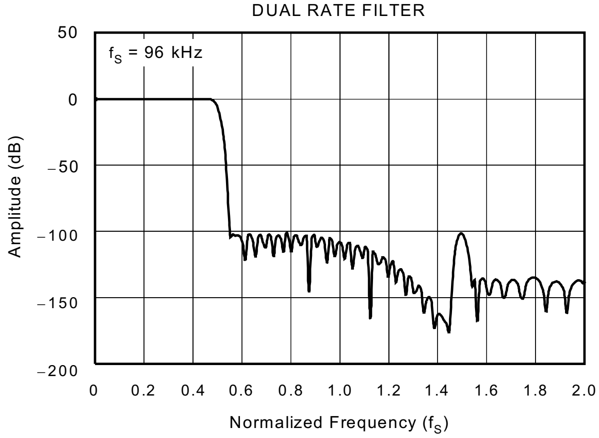
PASSBAND RIPPLE CHARACTERISTICS
SINGLE RATE FILTER



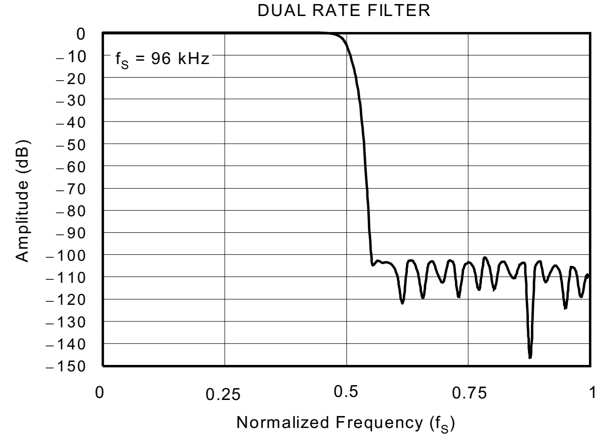
TRANSIENT BAND CHARACTERISTICS
SINGLE RATE FILTER



OVERALL CHARACTERISTICS
DUAL RATE FILTER



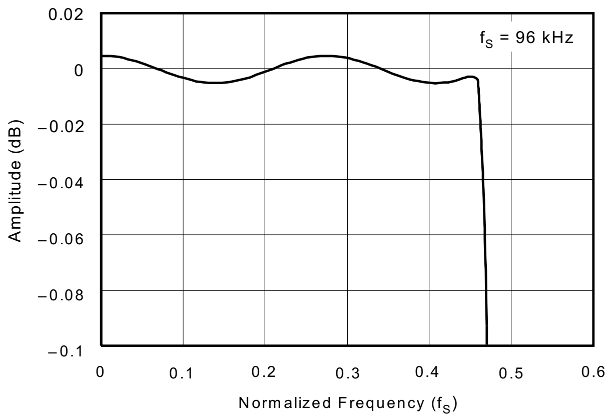
STOP BAND ATTENUATION CHARACTERISTICS
DUAL RATE FILTER



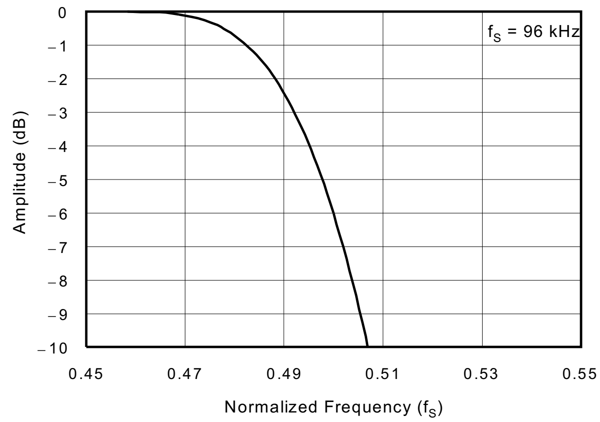
TYPICAL CHARACTERISTICS (continued)

All parameters are specified at T_A = 25°C with V_{CC} = 5 V, V_{DD} = 3.3 V, and a measurement bandwidth from 20 Hz to 20 kHz, unless otherwise noted.

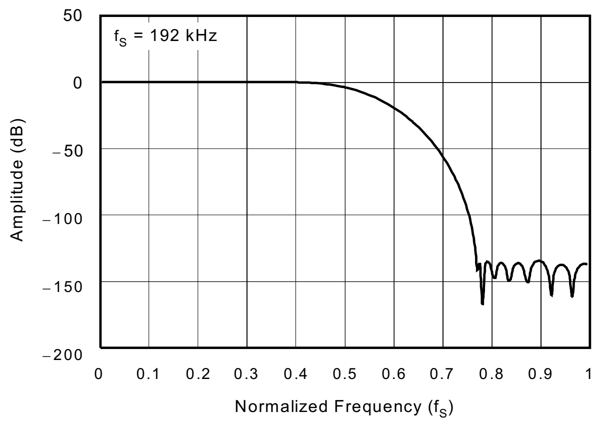
PASSBAND RIPPLE CHARACTERISTICS
DUAL RATE FILTER



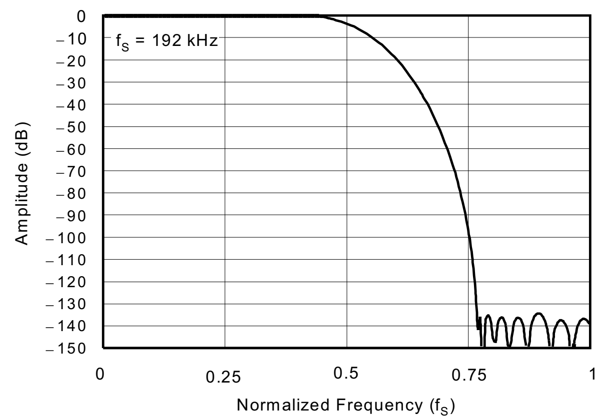
TRANSIENT BAND CHARACTERISTICS
DUAL RATE FILTER



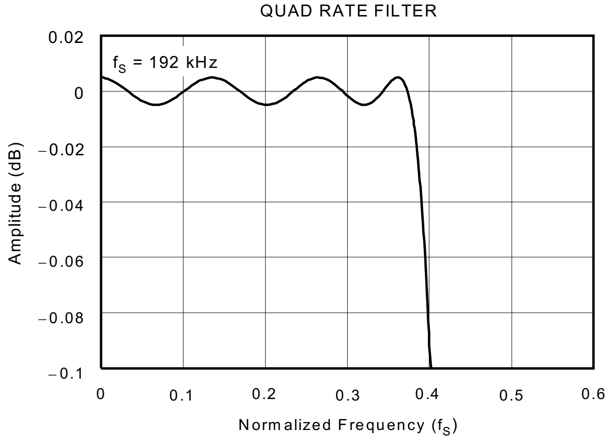
OVERALL CHARACTERISTICS
QUAD RATE FILTER



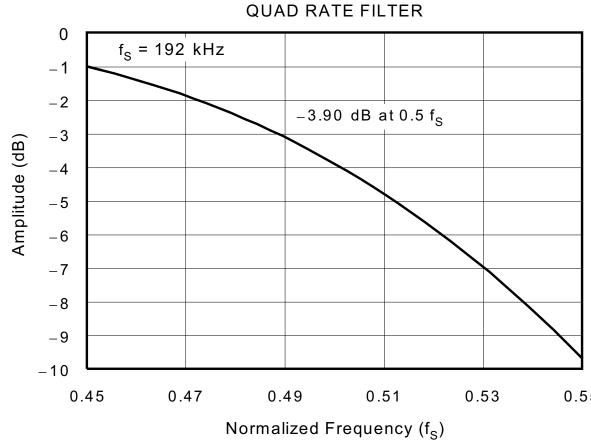
STOP BAND ATTENUATION CHARACTERISTICS
QUAD RATE FILTER



PASSBAND RIPPLE CHARACTERISTICS
QUAD RATE FILTER



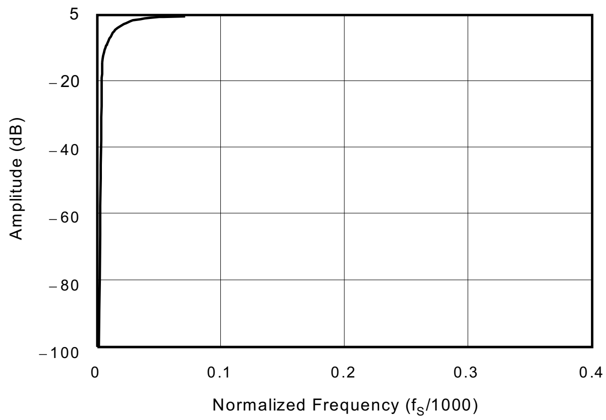
TRANSIENT BAND CHARACTERISTICS
QUAD RATE FILTER



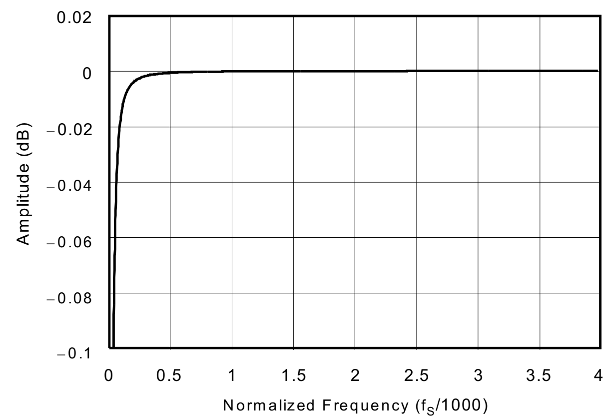
TYPICAL CHARACTERISTICS (continued)

All parameters are specified at T_A = 25°C with V_{CC} = 5 V, V_{DD} = 3.3 V, and a measurement bandwidth from 20 Hz to 20 kHz, unless otherwise noted.

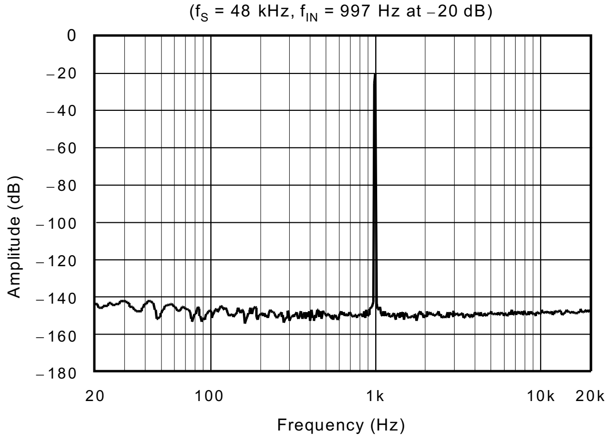
HIGH PASS FILTER
STOP BAND CHARACTERISTICS



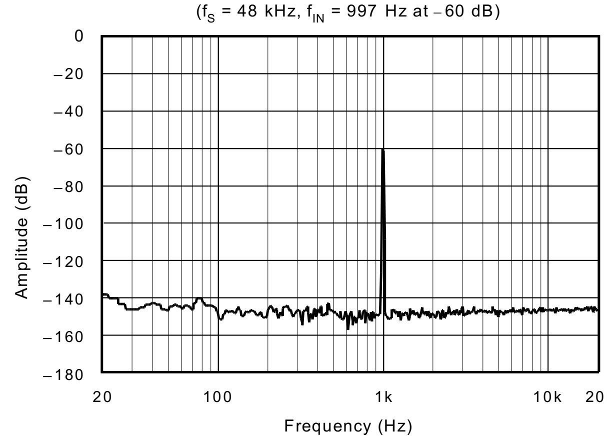
HIGH PASS FILTER
PASSBAND CHARACTERISTICS



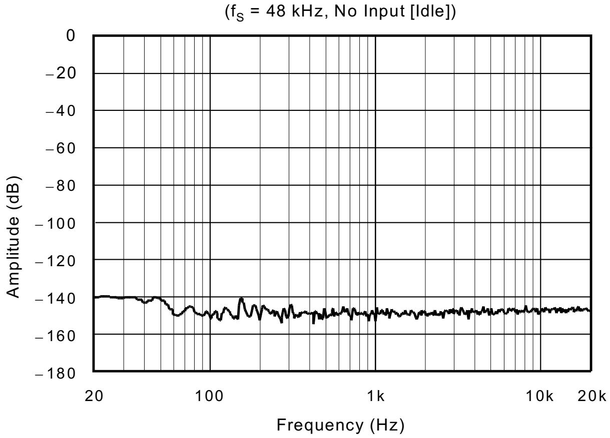
FFT PLOT
(f_S = 48 kHz, f_{IN} = 997 Hz at –20 dB)



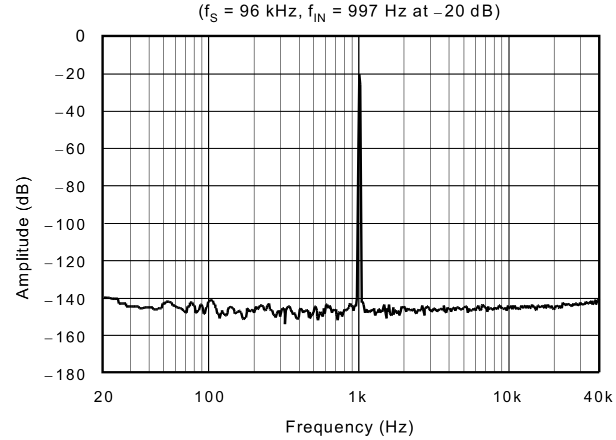
FFT PLOT
(f_S = 48 kHz, f_{IN} = 997 Hz at –60 dB)



FFT PLOT
(f_S = 48 kHz, No Input [Idle])



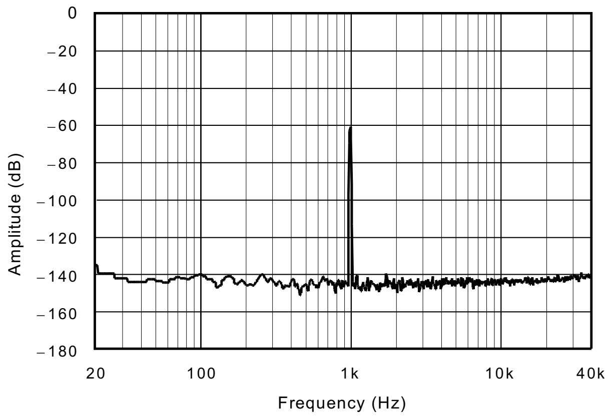
FFT PLOT
(f_S = 96 kHz, f_{IN} = 997 Hz at –20 dB)



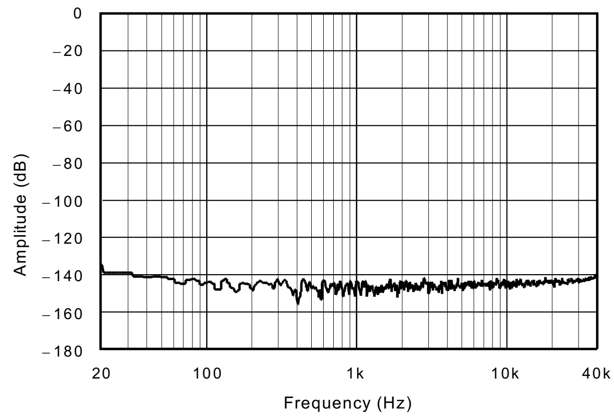
TYPICAL CHARACTERISTICS (continued)

All parameters are specified at T_A = 25°C with V_{CC} = 5 V, V_{DD} = 3.3 V, and a measurement bandwidth from 20 Hz to 20 kHz, unless otherwise noted.

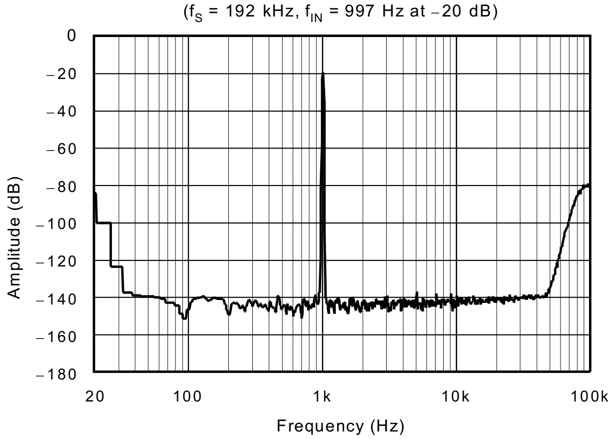
FFT PLOT
(f_S = 96 kHz, f_{IN} = 997 Hz at – 60 dB)



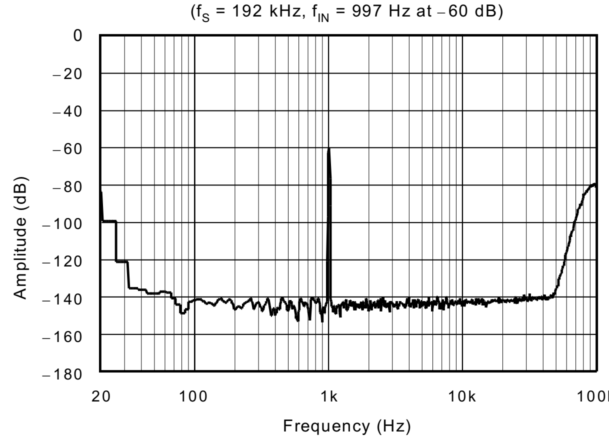
FFT PLOT
(f_S = 96 kHz, No Input [Idle])



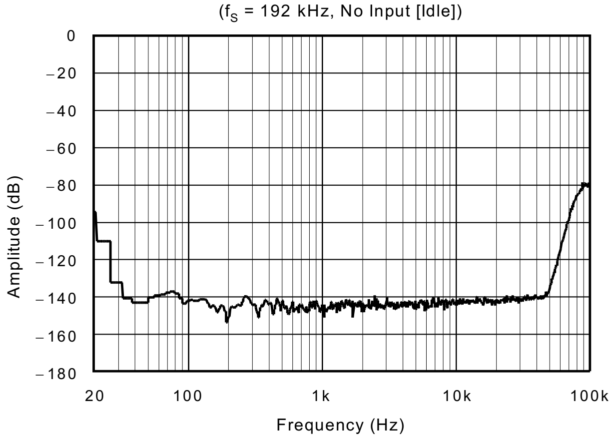
FFT PLOT
(f_S = 192 kHz, f_{IN} = 997 Hz at – 20 dB)



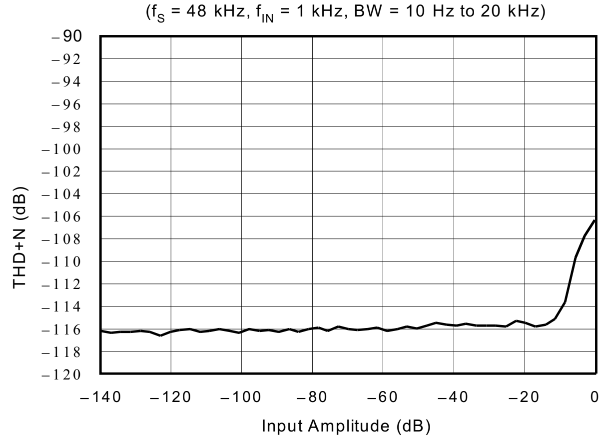
FFT PLOT
(f_S = 192 kHz, f_{IN} = 997 Hz at – 60 dB)



FFT PLOT
(f_S = 192 kHz, No Input [Idle])



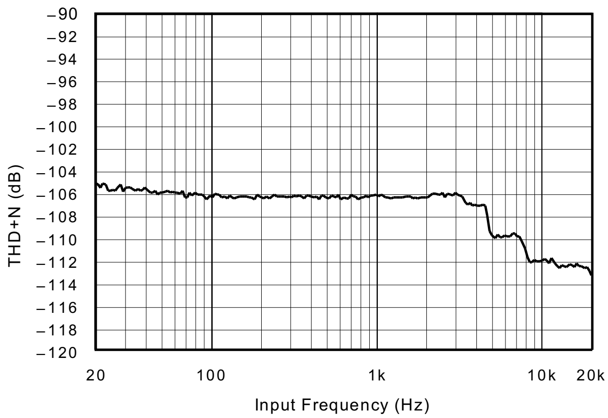
THD+N vs AMPLITUDE
(f_S = 48 kHz, f_{IN} = 1 kHz, BW = 10 Hz to 20 kHz)



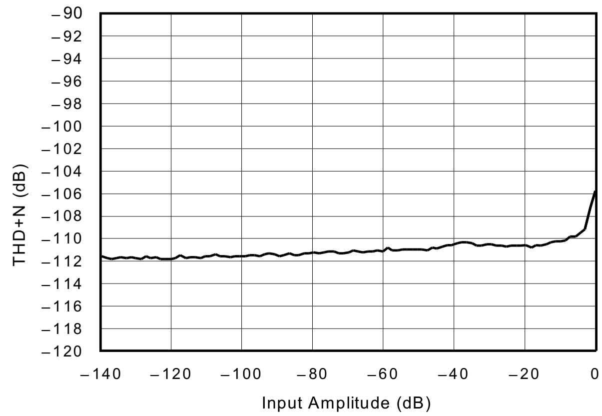
TYPICAL CHARACTERISTICS (continued)

All parameters are specified at T_A = 25°C with V_{CC} = 5 V, V_{DD} = 3.3 V, and a measurement bandwidth from 20 Hz to 20 kHz, unless otherwise noted.

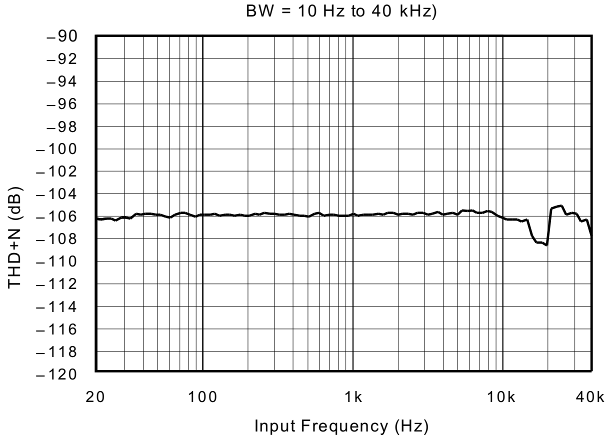
THD+N vs FREQUENCY
(f_S = 48 kHz, Input Amplitude = −0.5 dB, BW = 10 Hz to 20 kHz)



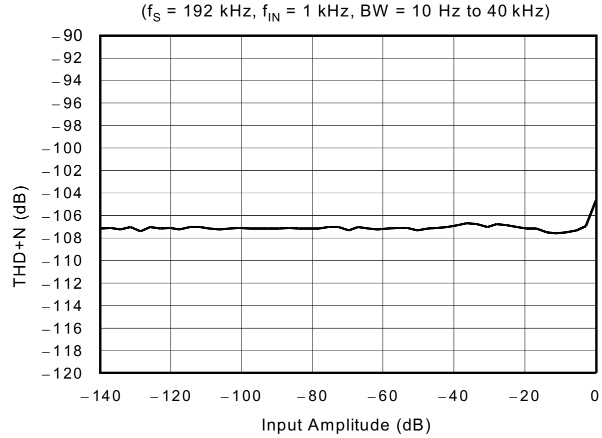
THD+N vs AMPLITUDE
(f_S = 96 kHz, f_{IN} = 1 kHz, BW = 10 Hz to 40 kHz)



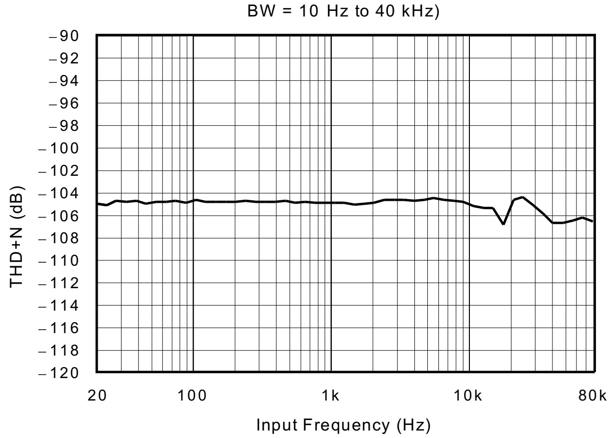
THD+N vs FREQUENCY
(f_S = 96 kHz, Input Amplitude = −0.5 dB, BW = 10 Hz to 40 kHz)



THD+N vs AMPLITUDE
(f_S = 192 kHz, f_{IN} = 1 kHz, BW = 10 Hz to 40 kHz)



THD+N vs FREQUENCY
(f_S = 192 kHz, Input Amplitude = −0.5 dB, BW = 10 Hz to 40 kHz)



PRODUCT OVERVIEW

The PCM4202 is a high-performance, stereo audio analog-to-digital (A/D) converter designed for use in professional and broadcast audio applications. The PCM4202 features 24 bit linear PCM or 1 bit Direct Stream Digital (DSD) data output capability for both channels. Sampling rates up to 216 kHz are supported for PCM output formats, while 64× or 128× oversampled 1 bit data is supported for DSD output mode. Native support for both PCM and DSD data formats makes the PCM4202 ideal for use in a wide variety of audio recording and processing applications.

The PCM4202 features 1 bit delta-sigma modulators employing density modulated dither for improved dynamic performance. Differential voltage inputs are utilized for the modulators, providing excellent common-mode rejection. On-chip voltage references are provided for the modulators, in addition to generating DC common-mode bias voltage outputs for use with external input circuitry. Linear phase digital decimation filtering is provided for the 24 bit PCM data outputs, with a minimum stop band attenuation of –100 dB for all sampling modes.

The PCM output mode features clipping flag outputs for each channel, as well as a digital high-pass filter for DC removal. The PCM4202 may be configured using dedicated input pins for sampling mode and audio data format selection, high-pass filter enable/disable, and reset/power-down operation.

A 5 V power supply is required for the analog section of the device, while a 3.3-V power supply is required for the digital circuitry. Figure 1 shows the functional block diagram for the PCM4202.

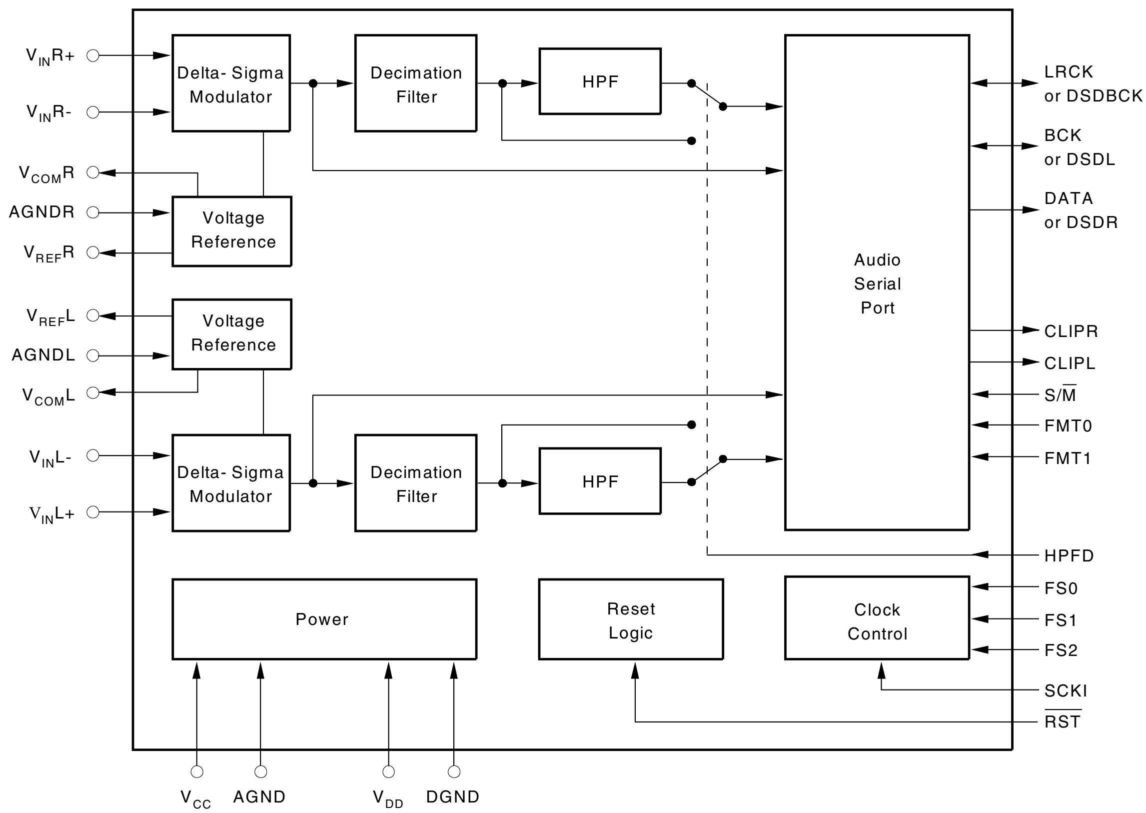


Figure 1. PCM4202 Functional Block Diagram

ANALOG OUTPUTS

The PCM4202 includes two channels of A/D conversion, each with its own pair of differential voltage input pins. The V_{IN}L+ (pin 4) and V_{IN}L– (pin 5) inputs correspond to Left channel input, while V_{IN}R+ (pin 25) and V_{IN}R– (pin 24) correspond to the Right channel input. The average input impedance of each input pin is 3 kΩ.

Each analog input pair accepts a full-scale input voltage of approximately 6 V_{PP} differential, which corresponds to a 2.12 V_{RMS} or 8.75 dBu input swing. The analog input should not swing below analog ground or above the V_{CC} power supply by more than 300 mV. Refer to the ***Applications Information*** section of this datasheet for an example input buffer circuit.

VOLTAGE REFERENCES AND COMMON MODE BIAS VOLTAGES OUTPUTS

The PCM4202 includes two on-chip voltage references, one each for the Left and Right channels. The V_{REF}L (pin 1) and V_{REF}R (pin 28) outputs correspond to high reference outputs for Left and Right channels, respectively. De-coupling capacitors are connected between each of these pins and the corresponding reference ground pin, either AGNDL (pin 2) for the V_{REF}L output or AGNDR (pin 27) for the V_{REF}R output. It is recommended to have at least a 0.1 µF X7R ceramic chip capacitor connected in parallel with a 33 µF low ESR tantalum chip capacitor for de-coupling purposes. The V_{REF}L and V_{REF}R outputs should not be utilized to bias external circuitry, because they are not buffered. Use the V_{COM}L (pin 3) and V_{COM}R (pin 26) outputs to bias external circuitry, as described in the following paragraphs.

Refer to the ***Applications Information*** section of this datasheet for the recommended voltage reference pin connections.

The PCM4202 analog inputs are internally biased to approximately V_{CC}/2. This bias voltage is referred to as the common mode voltage, and is output at V_{COM}L (pin 3) and V_{COM}R (pin 26), corresponding to the Left and Right channels, respectively. These outputs provide a level shifting voltage for biasing external input buffer circuitry. Although the V_{COM}L and V_{COM}R outputs are internally buffered, the output current is limited to a few hundred µA. It is recommended to connect these pins to external nodes with greater than 1 MΩ impedance, or to buffer the outputs with a voltage follower circuit when driving multiple external or low impedance nodes.

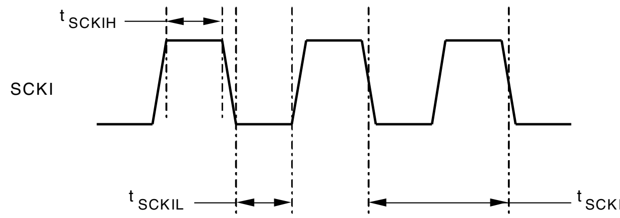
Refer to the ***Applications Information*** section of this datasheet for an example input buffer circuit that utilizes the common-mode bias voltage outputs.

SYSTEM CLOCK INPUT

The PCM4202 requires an external system clock, from which the modulator oversampling and digital sub-system clocks are derived. The system clock is applied at the SCKI input (pin 18). The frequency of the system clock is dependent upon the desired PCM output sampling frequency or DSD data rate, along with the sampling mode selection. Table 1 shows the corresponding system clock frequencies for common output sampling and data rates, along with the corresponding sampling modes. Timing requirements for the system clock are shown in Figure 2.

Table 1. System Clock Frequencies for Common Output Sampling and Data Rates

SAMPLING MODE	SAMPLING FREQUENCY, f_S (kHz)	SYSTEM CLOCK FREQUENCY (MHz)					
		128 f_S	192 f_S	256 f_S	384 f_S	512 f_S	768 f_S
Single Rate	32	n/a	n/a	8.192	12.288	16.384	24.576
Single Rate	44.1	n/a	n/a	11.2896	16.9344	22.5792	33.8688
Single Rate	48	n/a	n/a	12.288	18.432	24.576	36.864
Dual Rate	88.2	n/a	n/a	22.5792	33.8688	n/a	n/a
Dual Rate	96	n/a	n/a	24.576	36.864	n/a	n/a
Quad Rate	176.4	22.5792	33.8688	n/a	n/a	n/a	n/a
Quad Rate	192	24.576	36.864	n/a	n/a	n/a	n/a
DSD Output	128 f_S Data (Single Rate)	n/a	n/a	11.2896	16.9344	22.5792	33.8688
DSD Output	64 f_S Data (Dual Rate)	n/a	n/a	11.2896	16.9344	n/a	n/a



PARAMETER	DESCRIPTION	MIN	MAX	UNITS
t_{SCKI}	System Clock Period	26		ns
t_{SCKIH}	System Clock High Pulse Time	12		ns
t_{SCKIL}	System Clock Low Pulse Time	12		ns

Figure 2. System Clock Timing Requirements

SAMPLING MODES

The PCM4202 may be operated in one of three PCM sampling modes, or at one of two DSD output data rates. The PCM sampling modes are referred to as Single Rate, Dual Rate, and Quad Rate.

Single Rate mode is utilized for sampling rates up to 54 kHz. The delta-sigma modulator oversamples the analog input signal by a rate equal to 128 times the desired output sampling rate.

Dual Rate mode is utilized for sampling rates higher than 54 kHz and up to 108 kHz. The delta-sigma modulator oversamples the analog input signal by a rate equal to 64 times the desired output sampling rate.

Quad Rate mode is utilized for sampling frequencies higher than 108 kHz and up to 216 kHz. The delta-sigma modulator oversamples the analog input signal by a rate equal to 32 times the desired output sampling rate.

For DSD output data, the user may select either 64 f_S or 128 f_S oversampled data rates, where f_S is the base sampling rate, which is 44.1 kHz for Super Audio CD (SACD) applications. The 64 f_S data rate is analogous to the Dual Rate PCM sampling mode, where the analog input signal is oversampled by a rate equal to 64 times the base sampling rate. The 128 f_S data rate corresponds to the Single Rate PCM sampling mode, where the analog input signal is oversampled by a rate equal to 128 times the base sampling rate.

Table 1 indicates the sampling mode utilized for common system clock and sampling rate combinations. The FS0 (pin 9), FS1 (pin 10), and FS2 (pin 11) inputs are utilized to select the sampling mode for the PCM4202. If the state of the sampling mode pins is changed any time after power-up reset initialization, the user should issue an external forced reset to re-initialize the PCM4202. Table 2, Table 3, and Table 4 indicate the sampling mode selections for PCM Master and Slave mode operation, as well as the DSD Output mode.

Table 2. Sampling Mode Selection for PCM Master Mode Operation

FS2	FS1	FS0	SAMPLING MODE WITH SYSTEM CLOCK RATE
0	0	0	Single Rate with f_{SCKI} = 768 f_S
0	0	1	Single Rate with f_{SCKI} = 512 f_S
0	1	0	Single Rate with f_{SCKI} = 384 f_S
0	1	1	Single Rate with f_{SCKI} = 256 f_S
1	0	0	Dual Rate with f_{SCKI} = 384 f_S
1	0	1	Dual Rate with f_{SCKI} = 256 f_S
1	1	0	Quad Rate with f_{SCKI} = 192 f_S
1	1	1	Quad Rate with f_{SCKI} = 128 f_S

Table 3. Sampling Mode Selection for PCM Slave Mode Operation

FS2	FS1	FS0	SAMPLING MODE
0	0	0	Single Rate with Clock Auto-Detection
0	0	1	Dual Rate with Clock Auto-Detection
0	1	0	Quad Rate with Clock Auto-Detection
0	1	1	Reserved
1	0	0	Reserved
1	0	1	Reserved
1	1	0	Reserved
1	1	1	Reserved

Table 4. Sampling Mode Selection for DSD Output Mode Operation

FS2	FS1	FS0	SAMPLING MODE
0	0	0	128 f_S DSD Output Rate with f_{SCKI} = 768 f_S
0	0	1	128 f_S DSD Output Rate with f_{SCKI} = 512 f_S
0	1	0	128 f_S DSD Output Rate with f_{SCKI} = 384 f_S
0	1	1	128 f_S DSD Output Rate with f_{SCKI} = 256 f_S
1	0	0	64 f_S DSD Output Rate with f_{SCKI} = 384 f_S
1	0	1	64 f_S DSD Output Rate with f_{SCKI} = 256 f_S
1	1	0	Reserved
1	1	1	Reserved

AUDIO DATA FORMATS

As mentioned previously, the PCM4202 supports 24 bit linear PCM output data, as well as 1 bit DSD output data. The available data formats are dependent upon whether the PCM4202 is configured in Slave or Master mode. The S/$\overline{M}$ (pin 8), FMT0 (pin 6), and FMT1 (pin 7) inputs are utilized to select either Slave or Master mode and the corresponding audio data format.

In Slave mode, the PCM bit and left/right clocks (BCK and LRCK) are configured as input pins. DSD data formats are not supported in Slave mode. Slave mode supports commonly used PCM audio data formats, including Left Justified, Right Justified, and Philips I^2S.

In Master mode, the PCM bit and left/right clocks (BCK and LRCK respectively) are configured as output pins, and are derived from the system clock input (SCKI). Alternatively, the DSD output data may be provided at the port output.

Table 5 shows the available data format selections. Figure 3 and Figure 4 illustrate the PCM and DSD data formats.

Table 5. Audio Data Format Selection

FMT1	FMT0	AUDIO DATA FORMAT
0	0	24 bit Left Justified
0	1	24 bit I^2S
1	0	24 bit Right Justified
1	1	1 bit DSD (Master Mode Only)

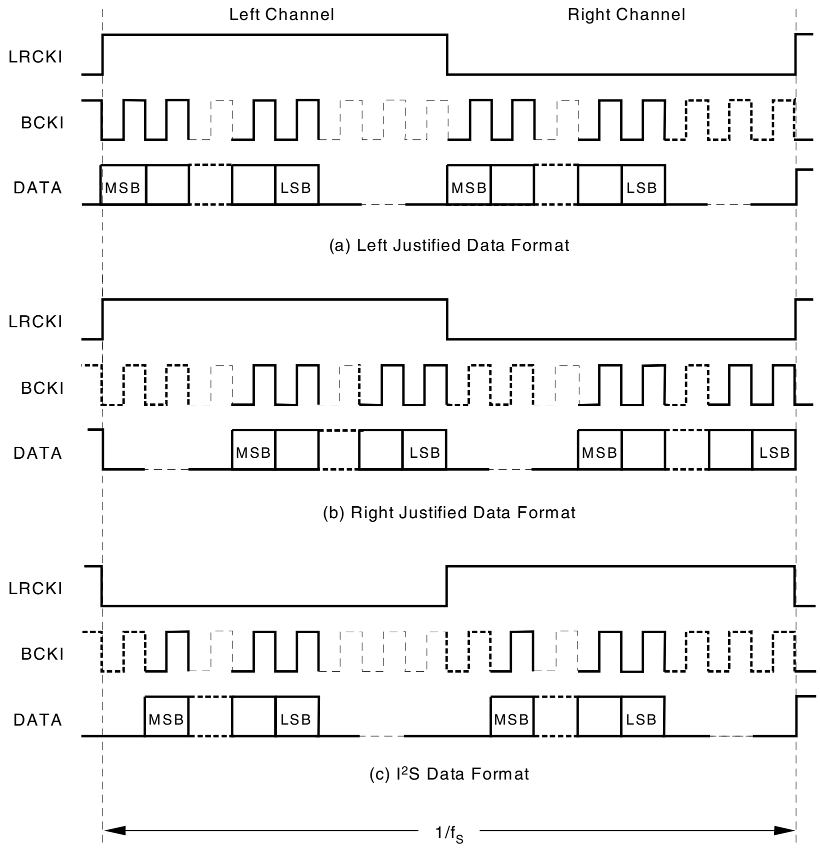


Figure 3. PCM Data Formats: Left Justified, Right Justified, and Philips I²S

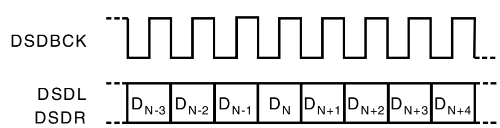


Figure 4. DSD Output Data Format

AUDIO SERIAL PORT OPERATION

This section provides additional details regarding the PCM4202 audio serial port, utilized for 24 bit linear PCM or 1 bit DSD output data. PCM output operation will be described in this section, while DSD output mode operation will be described in the following section.

For PCM data formats, the serial port is comprised of three signals: BCK (pin 16), LRCK (pin 17), and DATA (pin 15). The BCK signal functions as the data (or bit) clock for the serial audio data. The LRCK is the left/right word clock for the audio serial port. The LRCK and BCK clocks must be synchronous. The DATA signal is the serial audio data output, with data being clocked out on the falling edge of the BCK signal. DATA carries audio data for both the Left and Right channels.

As mentioned in the Audio Data Format section of this datasheet, the audio serial port can operate in Master or Slave mode. In Master mode, the BCK and LRCK clock signals are outputs, derived from the system clock input, SCKI. The BCK clock is fixed at 128 f_S for Single Rate sampling mode, and at 64 f_S for Dual or Quad Rate sampling modes. The LRCK clock operates at f_S, the output sampling rate (that is, 48 kHz, 96 kHz, etc.).

In Slave mode, the BCK and LRCK signals are inputs, with the clocks being generated by a master timing source, such as a DSP serial port, PLL clock synthesizer, or a crystal oscillator/divider circuit. The BCK rate is typically equal to 128 f_S in Single Rate sampling mode, and 64 f_S in Dual or Quad Rate sampling modes. Although other BCK clock rates are possible, they are not recommended as a result if potential clock phase sensitivity issues, which can degrade the dynamic performance of the PCM4202. The LRCK clock must be operated at f_S, the output sampling rate.

Figure 5 illustrates the typical audio serial port connections between a PCM4202 and an audio signal processor when using the PCM output data formats. Figure 6 illustrates the audio serial port timing for both the Master and Slave modes of operation.

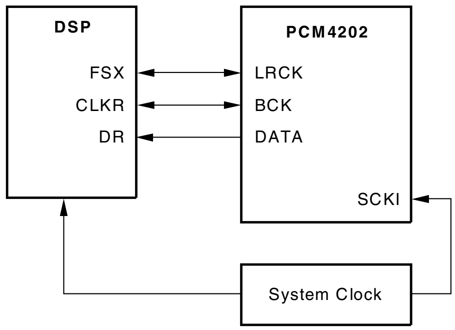
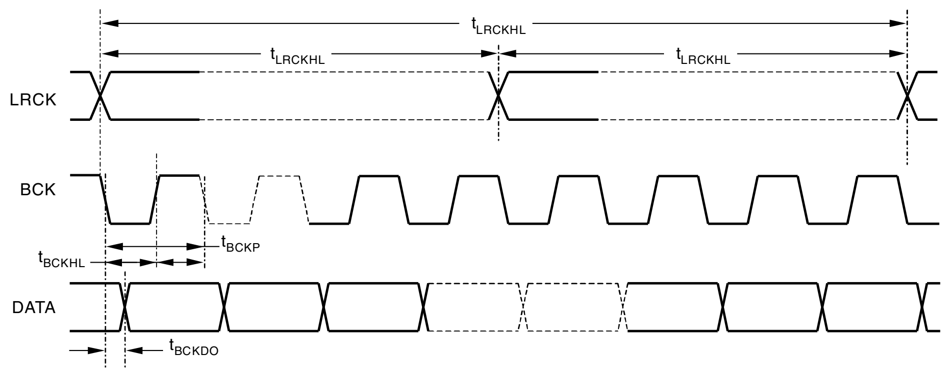


Figure 5. Typical Audio Serial Port Connections for Left Justified, Right Justified, and I²S Data Formats



PARAMETER	DESCRIPTION	MIN	MAX	UNITS
t_{LRCKP}	LRCK Period	5		µs
t_{LRCKHL}	LRCK High/Low Time	2.25		µs
t_{BCKP}	BCK Period	78		ns
t_{BCKHL}	BCK High/Low Time	35		ns
t_{BCKDO}	SDOUT Data Output Delay from BCK Falling Edge		10	ns

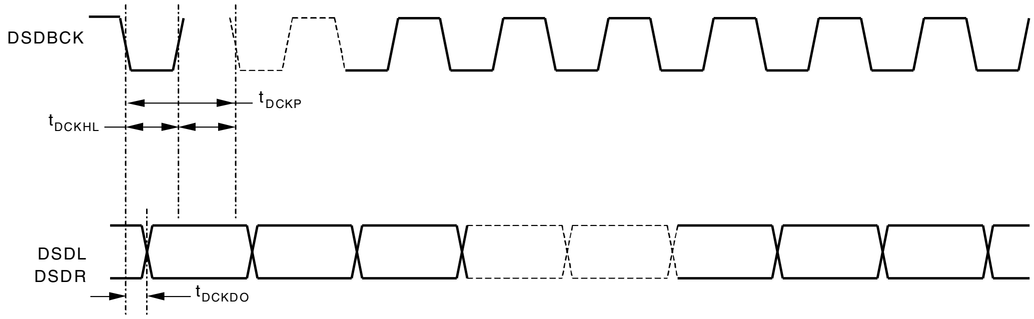
Figure 6. Master and Slave Mode Audio Serial Port Timing: Left Justified, Right Justified, and Philips I²S

DSD OUTPUT MODE OPERATION

The output port DSD mode operation consists of a single DSD data clock signal, DSDBCK (pin 17), along with two synchronous DSD data lines, DSDR (pin 15) and DSDL (pin 16). The data lines correspond to Right and Left channels, respectively. The DSD output rate is determined by the sampling mode settings for the device, discussed in the ***Sampling Modes*** section of this datasheet.

For DSD output data, the serial port is configured in Master mode, with the DSDBCK derived from the system clock input, SCKI. The DSDBCK is equivalent to the oversampling clock supplied to the delta-sigma modulators. The DSD data outputs, DSDR through DSDL, are synchronous to the DSDBCK. The clock and data lines are then connected to a data capture or processing device.

Figure 7 illustrates the DSD port timing for both the DSD output mode.



PARAMETER	DESCRIPTION	MIN	MAX	UNITS
t_{DCKP}	LRCK pulse width	156		ns
t_{DCKP}	LRCK active edge to BCK sampling edge delay	70		ns
t_{DCKP}	Data setup time		10	ns

Figure 7. DSD Data Port Timing

HIGH-PASS FILTER

A digital high-pass filter is available for removing the DC component of the digitized input signal. The filter is located at the output of the digital decimation filter, and is available only when using PCM output data formats. The high-pass filter can be enabled or disabled for both the Left and Right channels using the HPFD input (pin 12). Driving the HPFD input low enables the high-pass filter. Driving the HPFD input high disables the high-pass filter.

The –3 dB corner frequency for the high-pass filter scales with the output sampling rate, where $f_{-3\ dB} = f_S/48000$, where f_S is the output sampling rate.

CLIPPING FLAGS

The PCM4202 includes a clipping flag output for each channel. The outputs are designated CLIPL (pin 21) and CLIPR (pin 20), corresponding to the Left and Right channels, respectively. The clipping flags are only available when using PCM output data formats.

A clipping flag is forced high as soon as the digital output of the decimation filter exceeds the full-scale range for the corresponding channel. The clipping flag output is held high for a maximum of $(256 \times N) / f_S$ seconds, where N = 128 for Single Rate sampling mode, 256 for Dual Rate sampling mode, and 512 for Quad Rate sampling mode. If the decimation filter output does not exceed the full-scale range during the initial hold period, the output returns to a low state upon termination of the hold period.

RESET OPERATION

The PCM4202 includes two reset functions: power-on and externally controlled. This section describes the operation of each of these functions.

On power-up, the internal reset signal is forced low, forcing the PCM4202 into a reset state. The power-on reset circuit monitors the V_{DD} (pin 14) and V_{CC} (pin 22) power supplies. When the V_{DD} supply exceeds 2 V (±400 mV) and the V_{CC} supply exceeds 4 V (±400 mV), the internal reset signal is forced high. The PCM4202 then waits for the system clock input (SCKI) to become active. Once the system clock has been detected, the initialization sequence begins. The initialization sequence requires 1024 system clock periods for completion. During the initialization sequence, the ADC output data pins are forced low. Once the initialization sequence is completed, the PCM4202 output is enabled. Figure 8 shows the power-on reset sequence timing.

The user may force a reset initialization sequence at any time while the system clock input is active by utilizing the $\overline{RST}$ input (pin 19). The $\overline{RST}$ input is active low, and requires a minimum low pulse width of 40 ns. The low-to-high transition of the applied reset signal forces an initialization sequence to begin. As in the case of the power-on reset, the initialization sequence requires 1024 system clock periods for completion. Figure 9 illustrates the reset sequence initiated when using the $\overline{RST}$ input.

Figure 10 shows the state of the audio data outputs for the PCM4202 before, during and after the reset operations.

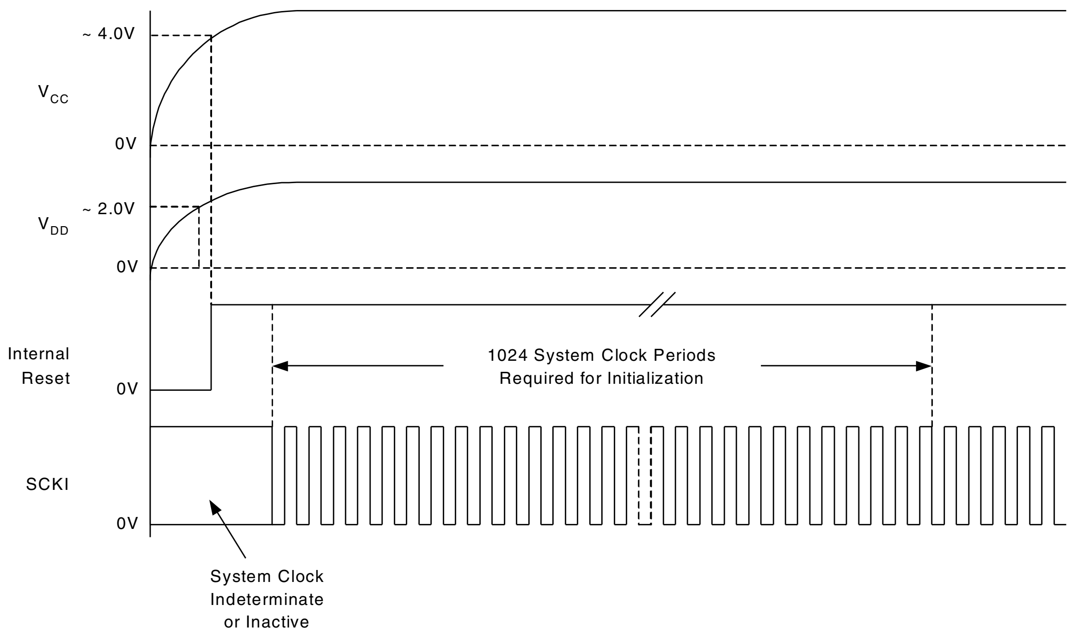


Figure 8. Power-Up Reset Timing

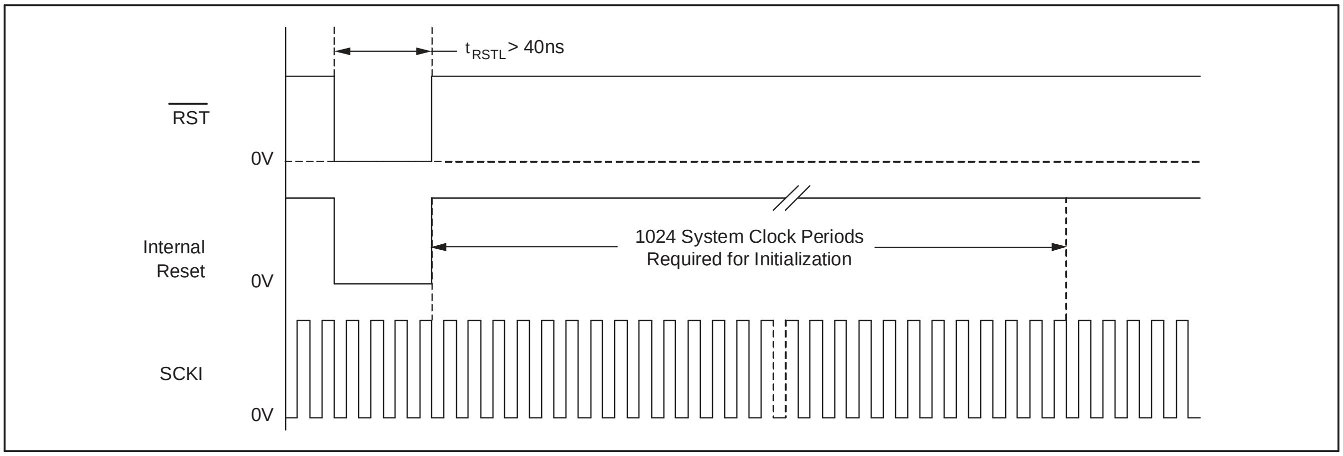


Figure 9. External Reset Timing

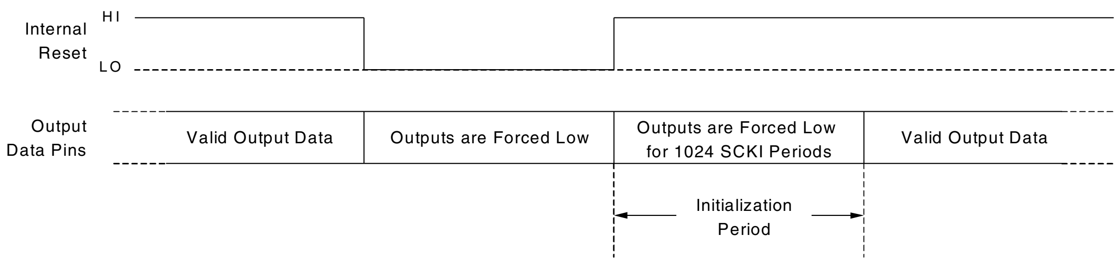


Figure 10. ADC Digital Output State for Reset Operations

POWER-DOWN OPERATION

The PCM4202 can be forced to a power-down state by applying a low level to the $\overline{RST}$ input (pin 19) for a minimum of 65,536 system clock cycles. In power-down mode, all internal clocks are stopped, and output data pins are forced low. The system clock may then be removed to conserve additional power. Before exiting power-down mode, the system and audio clocks should be restarted. Once the clocks are active, the $\overline{RST}$ input may be driven high, which initiates a reset initialization sequence. Figure 11 illustrates the state of the output data pins during before, during, and upon exiting the power-down state.

APPLICATIONS INFORMATION

A typical connection diagram for the PCM4202 is shown in Figure 12. Capacitors for power supply and reference bypassing are shown with recommended values. Bypass capacitors should be located as close as possible to the power supply and reference pins of the PCM4202. Due to its small size, the 0.1 μF capacitor can be located on the component (top) side of the board, while the larger 33 μF capacitor can be located on the solder (bottom) side of the board.

A single ground plane is utilized for the analog and digital ground connections. This approach ensures a low impedance connection between the analog and digital ground pins. The 5 V analog and 3.3 V digital power connections are provided from separate supplies.

Figure 13 illustrates an example input buffer circuit, designed for balanced differential input signals. This circuit is utilized on the PCM4202EVM evaluation board. The 2.7 nF and 100 pF capacitors shown at the output of the buffer should be located as close as possible to the analog input pins of the PCM4202. The buffer shown in Figure 13 can be easily made to function as a single ended to differential converter by simply grounding the (–) input terminal of the buffer circuit.

The input impedance for the V_{COM}IN pin of the OPA1632 is relatively low and will load down the V_{COM}L or V_{COM}R outputs from the PCM4202. A voltage follower circuit is required to buffer these outputs, with a typical circuit configuration shown in Figure 14. An OPA227 is utilized as the buffer for the PCM4202EVM evaluation board. However, alternative op amps with comparable performance may be substituted.

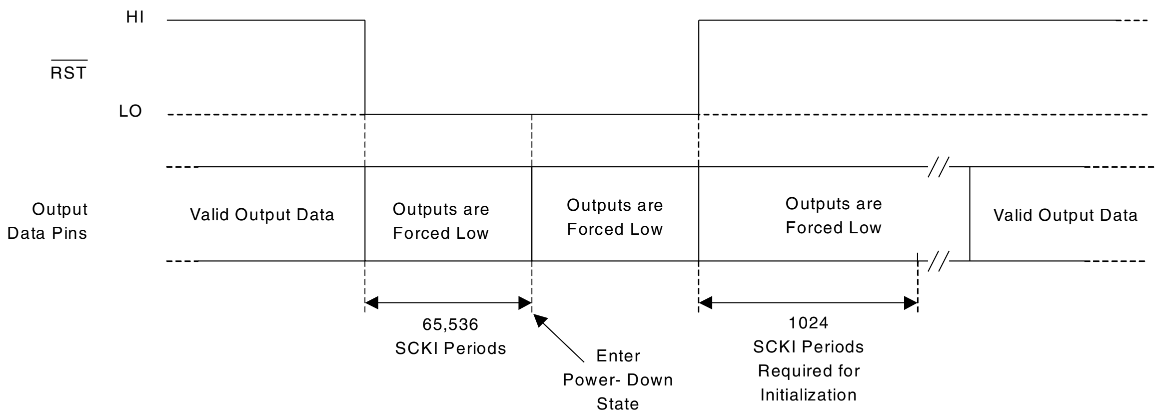


Figure 11. ADC Digital Output State for Power-Down Operations

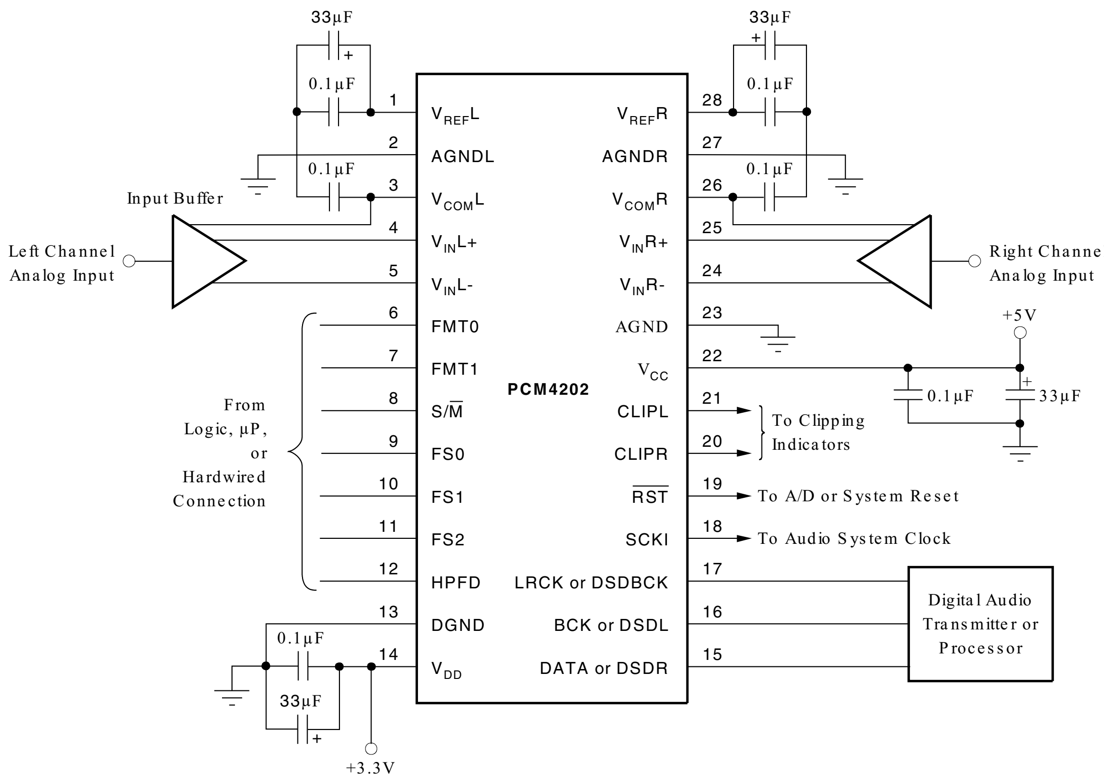


Figure 12. Typical Connection Diagram

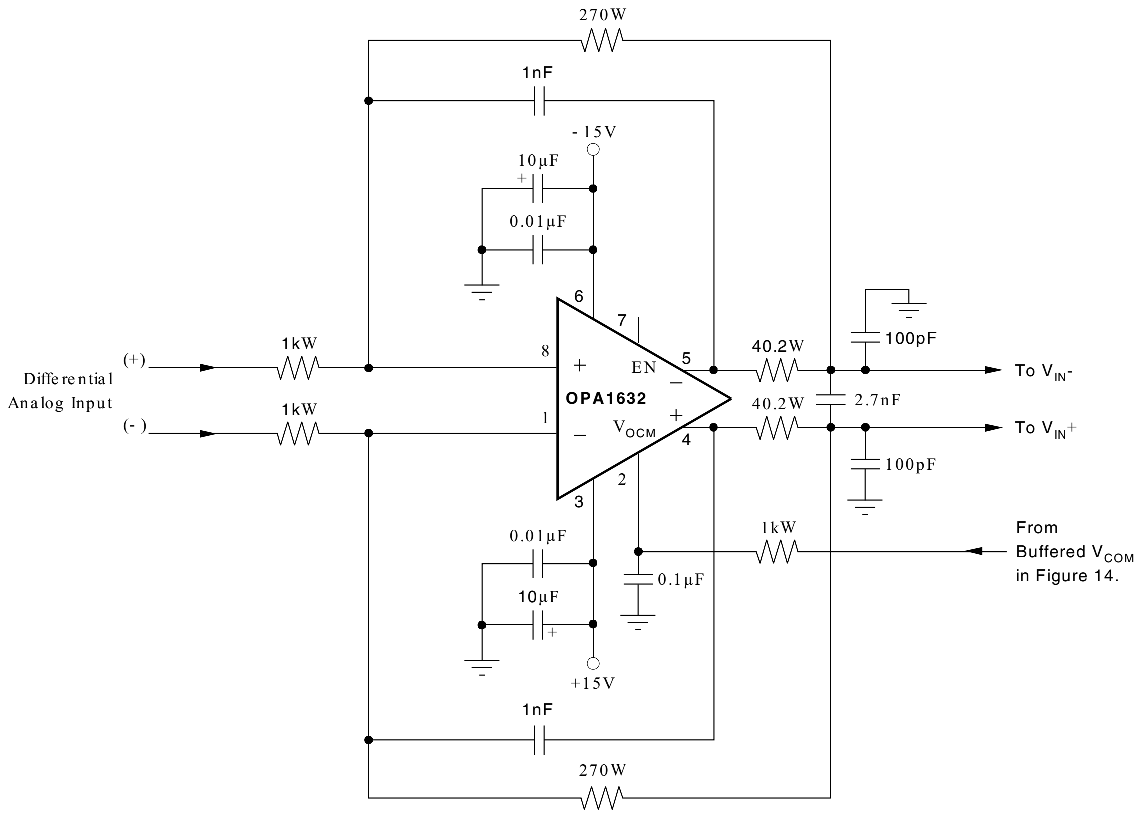


Figure 13. Example Input Buffer Circuit

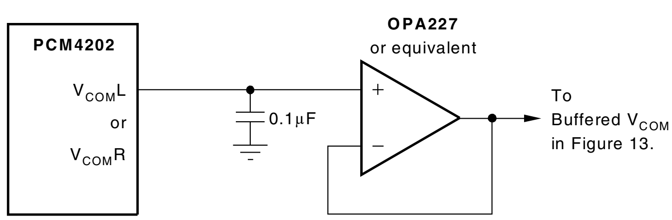


Figure 14. Example Buffer Circuit for V_{COM}L and V_{COM}R

COMPATIBILITY WITH THE PCM1804

Although the PCM4202 and PCM1804 are pin- and function-compatible, there are a few differences between the two devices that the designer should be aware of. These differences are noted here for clarity.

- The full-scale input of the PCM4202 is 6 V_{PP} differential, while it is 5 V_{PP} for the PCM1804. This is a result of the PCM4202 having an internal 3-V voltage reference, and the PCM1804 having an internal 2.5-V voltage reference.
- The PCM1804 includes 5-V tolerant digital inputs. The PCM4202 does not include these because the digital inputs are designed for interfacing to 3.3 V logic.
- The reset pin ($\overline{RST}$) pin of the PCM4202 has an internal pull-up resistor. For the PCM1804, this pin has an internal pull-down resistor.
- When operating in Master mode with Single Rate sampling selected, the audio serial port bit clock (BCK) is equal to 64 f_S for the PCM1804, while the BCK rate is equal to 128 f_S for the PCM4202.
- The following pins on the PCM4202 and PCM1804 have different names, but they perform the same functions.

Table 6. PINS

TERMINAL NUMBER	PCM4202 TERMINAL NAME	PCM1804 TERMINAL NAME
9	FS0	OSR0
10	FS1	OSR1
11	FS2	OSR2
12	HPFD	BYPAS
20	CLIPR	OVFR
21	CLIPL	OVFL

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
PCM4202IDBREP	LIFEBUY	SSOP	DB	28	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PCM4202EP	
V62/07642-01XE	LIFEBUY	SSOP	DB	28	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PCM4202EP	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF PCM4202-EP :

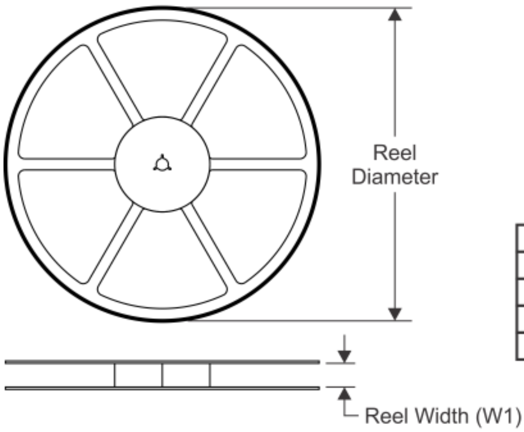
- Catalog: PCM4202

NOTE: Qualified Version Definitions:

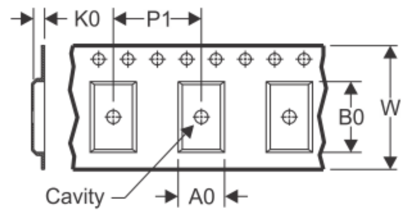
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

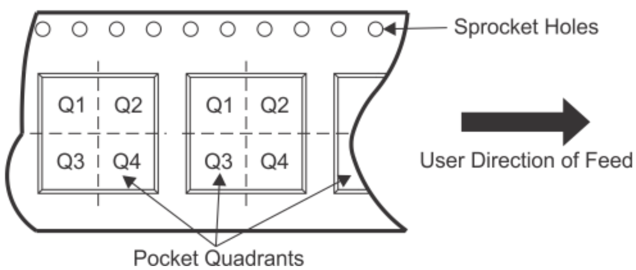


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

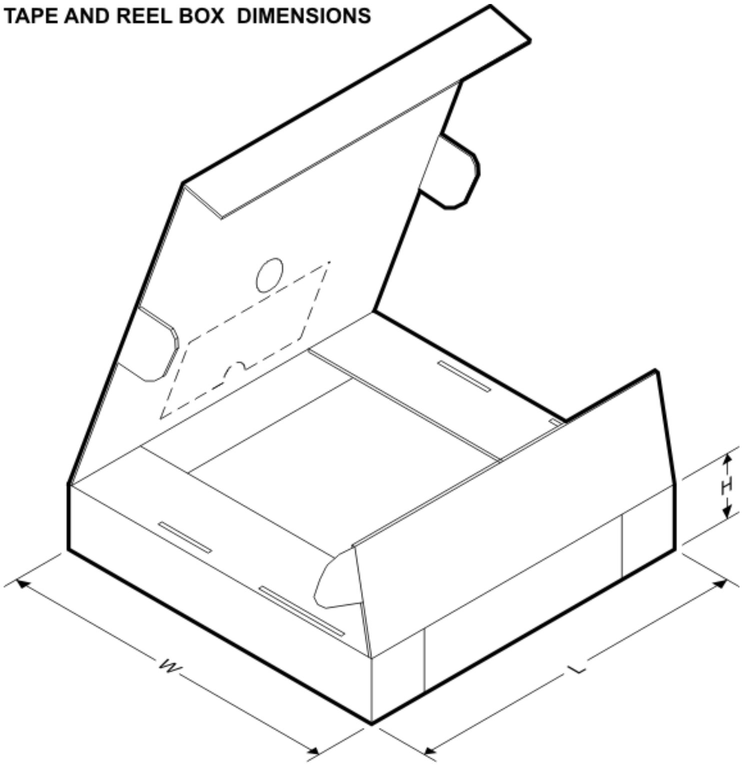
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
PCM4202IDBREP	SSOP	DB	28	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS

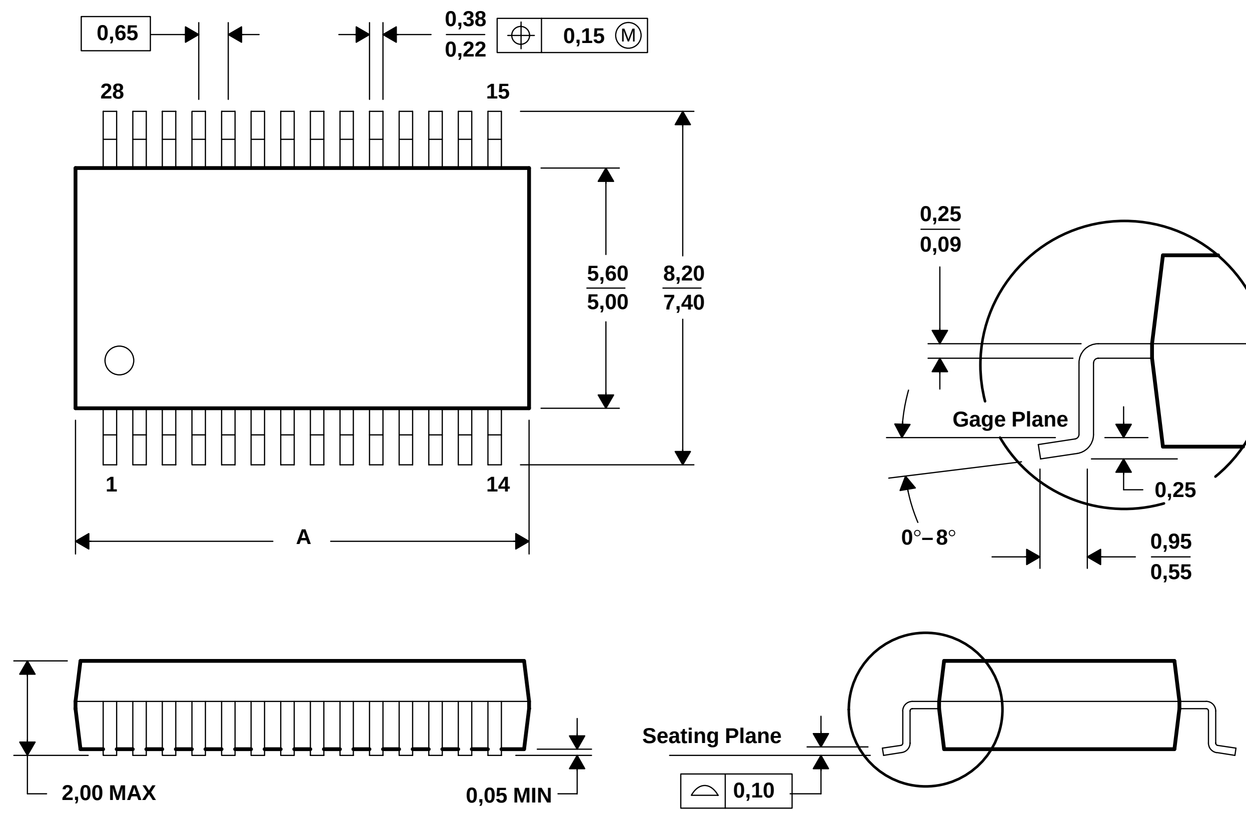


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
PCM4202IDBREP	SSOP	DB	28	2000	367.0	367.0	38.0

DB (R-PDSO-G)** **PLASTIC SMALL-OUTLINE**

28 PINS SHOWN



DIM \ PINS **	14	16	20	24	28	30	38
A MAX	6,50	6,50	7,50	8,50	10,50	10,50	12,90
A MIN	5,90	5,90	6,90	7,90	9,90	9,90	12,30

4040065 /E 12/01

NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
- D. Falls within JEDEC MO-150