

# NLSV4T3144

## 4-Bit Dual-Supply Non-Inverting Level Translator

The NLSV4T3144 is a 4-bit configurable dual-supply bus buffer level translator. The input (IN<sub>xn</sub>) and output (OUT<sub>xn</sub>) ports are designed to track two different power supply rails, V<sub>CCA</sub> and V<sub>CCB</sub> respectively. Both supply rails are configurable from 1.6 V to 3.6 V allowing low-voltage translation from the input to the output port.

### Features

- Wide V<sub>CCA</sub> and V<sub>CCB</sub> Operating Range: 1.6 V to 3.6 V
- High-Speed w/ Balanced Propagation Delay
- Inputs and Outputs have OVT Protection to 5.5 V
- Outputs at 3-State until Active V<sub>CCA</sub> and V<sub>CCB</sub> are Reached
- Power-Off Protection
- Ultra-Small Packaging: 1.7 mm x 2.0 mm UQFN-12
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

### Typical Applications

- Mobile Phones, PDAs, Other Portable Devices
- SPI™ Bus Voltage Translation

### Important Information

- ESD Protection for All Pins:  
HBM (Human Body Model) > 3000 V

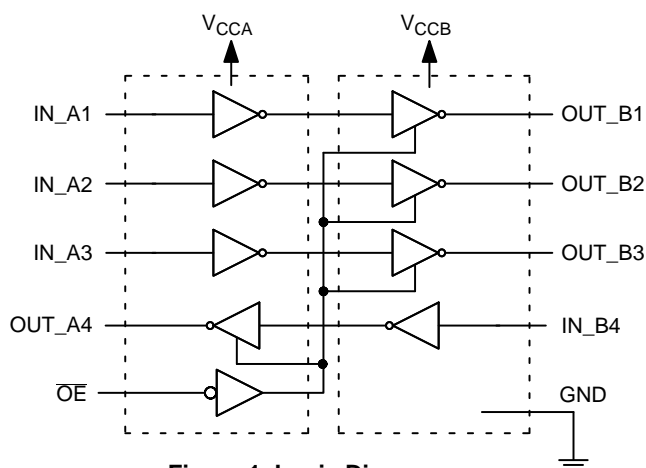
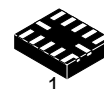


Figure 1. Logic Diagram



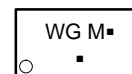
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UQFN12  
MU SUFFIX  
CASE 523AE

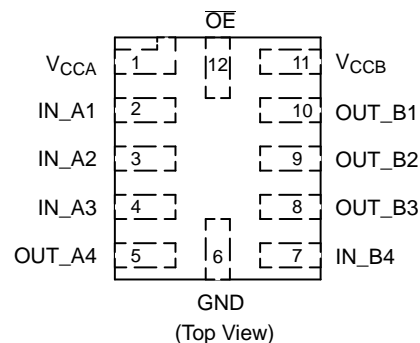
### MARKING DIAGRAM



WG = Specific Device Code  
M = Date Code  
▪ = Pb-Free Package

(Note: Microdot may be in either location)

### PIN ASSIGNMENTS



### ORDERING INFORMATION

Device	Package	Shipping†
NLSV4T3144MUTAG	UQFN-12 (Pb-Free)	3000/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

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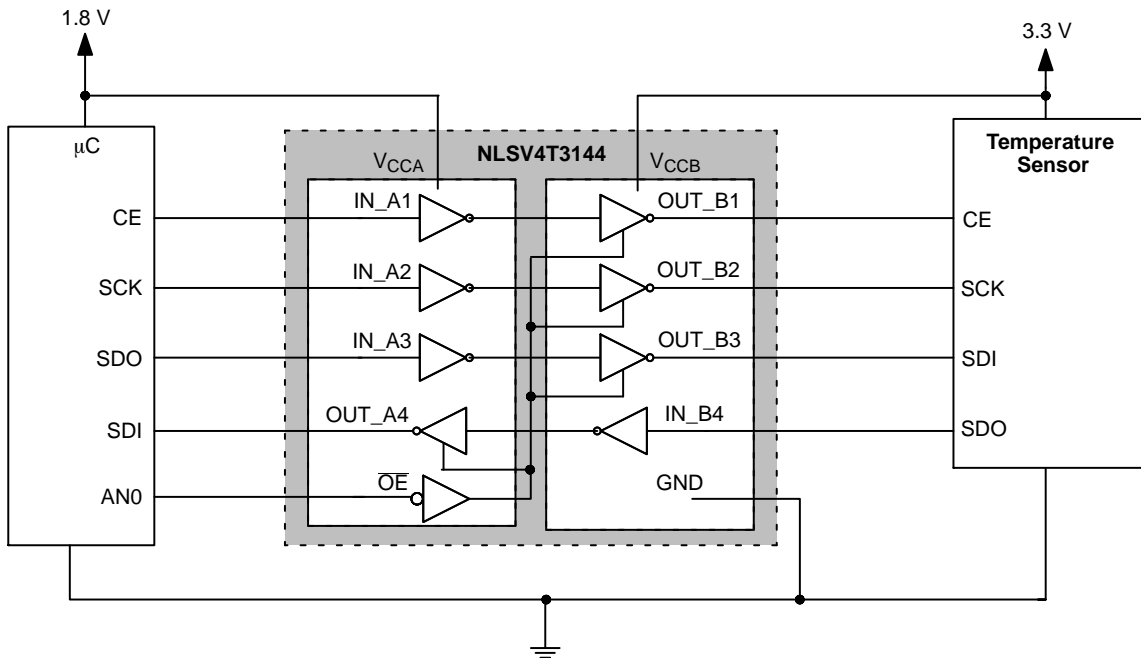


Figure 2. Typical Application: SPI Bus Voltage Translator

## PIN NAMES

Pins	Description
V <sub>CCA</sub>	'A' DC Power Supply
V <sub>CCB</sub>	'B' DC Power Supply
GND	Ground
IN_A1, IN_A2, IN_A3	Input (Referenced to V <sub>CCA</sub> )
IN_B4	Input (Referenced to V <sub>CCB</sub> )
OUT_B1, OUT_B2, OUT_B3	Output (Referenced to V <sub>CCB</sub> )
OUT_A4	Output (Referenced to V <sub>CCA</sub> )
OE	Output Enable (Referenced to V <sub>CCA</sub> )

## TRUTH TABLE

Inputs		Outputs
OE	IN_A1, IN_A2, IN_A3, IN_B4	OUT_B1, OUT_B2, OUT_B3, OUT_A4
H	X	3-State
L	L	L
	H	H

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## MAXIMUM RATINGS

Symbol	Parameter	Value	Condition	Unit
$V_{CCA}, V_{CCB}$	DC Supply Voltage, $V_{CCA} \leq V_{CCB}$	-0.5 to +5.5		V
$V_I$	DC Input Voltage $IN_{x_n}$	-0.5 to +5.5		V
$V_C$	Control Input $\overline{OE}$	-0.5 to +5.5		V
$V_O$	DC Output Voltage (Power Down) $OUT_{x_n}$	-0.5 to +5.5	$V_{CCA} = V_{CCB} = 0$	V
	(Active Mode) $OUT_{x_n}$	-0.5 to +5.5		
	(Tri-State Mode) $OUT_{x_n}$	-0.5 to +5.5		
$I_{IK}$	DC Input Diode Current	-20	$V_I < GND$	mA
$I_{OK}$	DC Output Diode Current	-50	$V_O < GND$	mA
$I_O$	DC Output Source/Sink Current	$\pm 50$		mA
$I_{CCA}, I_{CCB}$	DC Supply Current Per Supply Pin	$\pm 100$		mA
$I_{GND}$	DC Ground Current per Ground Pin	$\pm 100$		mA
$T_{STG}$	Storage Temperature	-65 to +150		°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

## RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
$V_{CCA}, V_{CCB}$	Positive DC Supply Voltage, $V_{CCA} \leq V_{CCB}$	1.6	3.6	V
$V_I$	Bus Input Voltage	GND	3.6	V
$V_C$	Control Input $\overline{OE}$	GND	3.6	V
$V_{IO}$	DC Output Voltage (Power Down) $OUT_{x_n}$	GND	3.6	V
	(Active Mode) $OUT_{x_n}$			
	(Tri-State Mode) $OUT_{x_n}$			
$T_A$	Operating Temperature Range	-40	+85	°C
$\Delta t / \Delta V$	Input Transition Rise or Rate $V_I$ , from 30% to 70% of $V_{CCA}$ and $V_{CCB}$ ; $V_{CCA} = V_{CCB} = 3.3 \text{ V} \pm 0.3 \text{ V}$	0	10	ns

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## DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Conditions	V <sub>CCA</sub> (V)	V <sub>CCB</sub> (V)	-40°C to + 85°C		Unit
					Min	Max	
V <sub>IH</sub> (IN_A1, IN_A2, IN_A3, OE)	Input HIGH Voltage		2.7 – 3.6	≥ V <sub>CCA</sub>	2.0	–	V
			2.3 – 2.7		1.6	–	
			1.6 – 2.3		0.65 * V <sub>CCA</sub>	–	
V <sub>IH</sub> (IN_B4)	Input HIGH Voltage		≤ V <sub>CCB</sub>	2.7 – 3.6	2.0	–	V
			2.3 – 2.7	1.6	–		
			1.6 – 2.3	0.65 * V <sub>CCB</sub>	–		
V <sub>IL</sub> (IN_A1, IN_A2, IN_A3, OE)	Input LOW Voltage		2.7 – 3.6	≥ V <sub>CCA</sub>	–	0.8	V
			2.3 – 2.7		–	0.7	
			1.6 – 2.3		–	0.35 * V <sub>CCA</sub>	
V <sub>IL</sub> (IN_B4)	Input LOW Voltage		≤ V <sub>CCB</sub>	2.7 – 3.6	–	0.8	V
			2.3 – 2.7	–	0.7		
			1.6 – 2.3	–	0.35 * V <sub>CCB</sub>		
V <sub>OH</sub> (OUT_B1, OUT_B2, OUT_B3)	Output HIGH Voltage	I <sub>OH</sub> = –100 μA; V <sub>I</sub> = V <sub>IH</sub>	≤ V <sub>CCB</sub>	1.6 – 3.6	V <sub>CCB</sub> – 0.2	–	V
		I <sub>OH</sub> = –6 mA; V <sub>I</sub> = V <sub>IH</sub>	1.6	1.6	1.25	–	
			2.3	2.3	2.0	–	
		I <sub>OH</sub> = –12 mA; V <sub>I</sub> = V <sub>IH</sub>	2.3	2.3	1.8	–	
			2.7	2.7	2.2	–	
		I <sub>OH</sub> = –18 mA; V <sub>I</sub> = V <sub>IH</sub>	2.3	2.3	1.7	–	
	3.0	3.0	2.4	–			
	I <sub>OH</sub> = –24 mA; V <sub>I</sub> = V <sub>IH</sub>	3.0	3.0	2.2	–	–	
V <sub>OH</sub> (OUT_A4)	Output HIGH Voltage	I <sub>OH</sub> = –100 μA; V <sub>I</sub> = V <sub>IH</sub>	1.6 – 3.6	≥ V <sub>CCA</sub>	V <sub>CCA</sub> – 0.2	–	V
		I <sub>OH</sub> = –6 mA; V <sub>I</sub> = V <sub>IH</sub>	1.6	1.6	1.25	–	
			2.3	2.3	2.0	–	
		I <sub>OH</sub> = –12 mA; V <sub>I</sub> = V <sub>IH</sub>	2.3	2.3	1.8	–	
			2.7	2.7	2.2	–	
		I <sub>OH</sub> = –18 mA; V <sub>I</sub> = V <sub>IH</sub>	2.3	2.3	1.7	–	
	3.0	3.0	2.4	–			
	I <sub>OH</sub> = –24 mA; V <sub>I</sub> = V <sub>IH</sub>	3.0	3.0	2.2	–	–	
V <sub>OL</sub> (OUT_B1, OUT_B2, OUT_B3)	Output LOW Voltage	I <sub>OL</sub> = 100 μA; V <sub>I</sub> = V <sub>IH</sub>	≤ V <sub>CCB</sub>	1.6 – 3.6	–	0.2	V
		I <sub>OL</sub> = 6 mA; V <sub>I</sub> = V <sub>IH</sub>	1.6	1.6	–	0.3	
		I <sub>OL</sub> = 12 mA; V <sub>I</sub> = V <sub>IH</sub>	2.3	2.3	–	0.4	
			2.7	2.7	–	0.4	
		I <sub>OL</sub> = 18 mA; V <sub>I</sub> = V <sub>IH</sub>	2.3	2.3	–	0.6	
			3.0	3.0	–	0.5	
	I <sub>OL</sub> = 24 mA; V <sub>I</sub> = V <sub>IH</sub>	3.0	3.0	–	0.6		
V <sub>OL</sub> (OUT_A4)	Output LOW Voltage	I <sub>OL</sub> = 100 μA; V <sub>I</sub> = V <sub>IH</sub>	1.6 – 3.6	≥ V <sub>CCA</sub>	–	0.2	V
		I <sub>OL</sub> = 6 mA; V <sub>I</sub> = V <sub>IH</sub>	1.6	1.6	–	0.3	
		I <sub>OL</sub> = 12 mA; V <sub>I</sub> = V <sub>IH</sub>	2.3	2.3	–	0.4	
			2.7	2.7	–	0.4	
		I <sub>OL</sub> = 18 mA; V <sub>I</sub> = V <sub>IH</sub>	2.3	2.3	–	0.6	
			3.0	3.0	–	0.5	
	I <sub>OL</sub> = 24 mA; V <sub>I</sub> = V <sub>IH</sub>	3.0	3.0	–	0.6		

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## DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Conditions	V <sub>CCA</sub> (V)	V <sub>CCB</sub> (V)	-40°C to +85°C		Unit
					Min	Max	
I <sub>IN</sub>	Input Leakage Current	V <sub>IN_A1</sub> = V <sub>IN_A2</sub> = V <sub>IN_A3</sub> = V <sub>CCA</sub> or GND; V <sub>IN_B4</sub> = V <sub>CCB</sub> or GND	≤ V <sub>CCB</sub>	1.6 – 3.6	-1.0	+1.0	μA
I <sub>OZ</sub>	I/O Tri – State Output Leakage Current	T <sub>A</sub> = 25°C, $\overline{OE}$ = V <sub>CCA</sub>	≤ V <sub>CCB</sub>	1.6 – 3.6	–	1.0	μA
I <sub>CCA</sub>	Quiescent Supply Current	V <sub>IN_A1</sub> = V <sub>IN_A2</sub> = V <sub>IN_A3</sub> = V <sub>CCA</sub> or GND; V <sub>IN_B4</sub> = V <sub>CCB</sub> or GND $\overline{OE}$ = GND, I <sub>O</sub> = 0	≤ V <sub>CCB</sub>	1.6 – 3.6	–	3.0	μA
I <sub>CCB</sub>	Quiescent Supply Current	V <sub>IN_A1</sub> = V <sub>IN_A2</sub> = V <sub>IN_A3</sub> = V <sub>CCA</sub> or GND; V <sub>IN_B4</sub> = V <sub>CCB</sub> or GND $\overline{OE}$ = GND, I <sub>O</sub> = 0	≤ V <sub>CCB</sub>	1.6 – 3.6	–	3.0	μA
I <sub>CCA</sub> + I <sub>CCB</sub>	Quiescent Supply Current	V <sub>IN_A1</sub> = V <sub>IN_A2</sub> = V <sub>IN_A3</sub> = V <sub>CCA</sub> or GND; V <sub>IN_B4</sub> = V <sub>CCB</sub> or GND $\overline{OE}$ = GND, I <sub>O</sub> = 0	≤ V <sub>CCB</sub>	1.6 – 3.6	–	6.0	μA

NOTE: Connect ground before applying supply voltage V<sub>CCA</sub> or V<sub>CCB</sub>. This device is designed with the feature that the power-up sequence of V<sub>CCA</sub> and V<sub>CCB</sub> will not damage the IC.

## AC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	V <sub>CCA</sub> (V)	-40°C to +85°C						Unit
			V <sub>CCB</sub> (V)						
			3.6		2.8		1.6		
			Min	Max	Min	Max	Min	Max	
t <sub>PLH</sub> , t <sub>PHL</sub>	Propagation Delay, Input to Output	3.6		3				ns	
		2.8		3.1		3.3			
		1.6		4.3		4.5			6.1
t <sub>PZH</sub> , t <sub>PZL</sub>	Output Enable, $\overline{OE}$ to Output	3.6		8.7				ns	
		2.8		10.3		10.7			
		1.6		17.2		18			20
t <sub>PHZ</sub> , t <sub>PLZ</sub>	Output Disable, $\overline{OE}$ to Output	3.6		7.8				ns	
		2.8		8.2		8.4			
		1.6		9.5		9.8			10.5
t <sub>OSHL</sub> , t <sub>OSLH</sub>	Output to Output Skew	3.6		0.25				ns	
		2.8		0.25		0.25			
		1.6		0.25		0.25			0.25

NOTE: Propagation delays defined per Figure 3.

## CAPACITANCE

Symbol	Parameter	Test Conditions	Typ (Note 1)	Unit
C <sub>I</sub>	Control Pin ( $\overline{OE}$ ) Input Capacitance	V <sub>CCA</sub> = V <sub>CCB</sub> = 3.3 V, V <sub>I</sub> = 0 V or V <sub>CCA/B</sub>	3.5	pF
C <sub>IN</sub>	Input Pin Capacitance	V <sub>CCA</sub> = V <sub>CCB</sub> = 3.3 V, V <sub>I</sub> = 0 V or V <sub>CCA/B</sub>	5.0	pF
C <sub>OUT</sub>	Output Pin Capacitance	V <sub>CCA</sub> = V <sub>CCB</sub> = 3.3 V, V <sub>I</sub> = 0 V or V <sub>CCA/B</sub>	5.0	pF
C <sub>PD</sub>	Power Dissipation Capacitance	V <sub>CCA</sub> = V <sub>CC2</sub> = 3.3 V, V <sub>I</sub> = 0 V or 3.3 V, f = 10 MHz	10	pF

1. Typical values are at T<sub>A</sub> = +25°C.

# NLSV4T3144

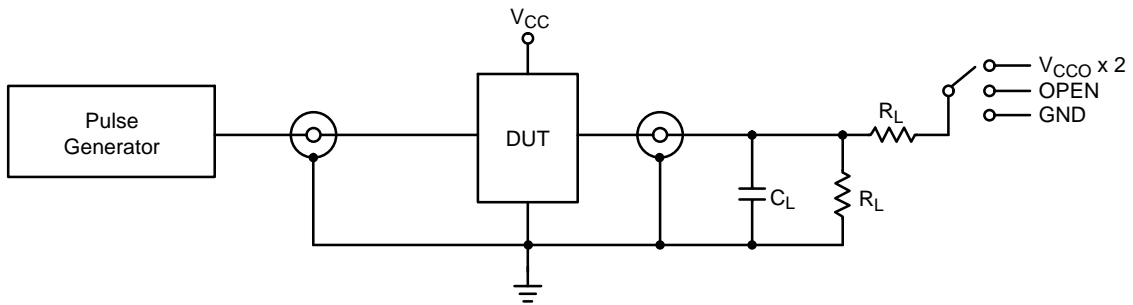
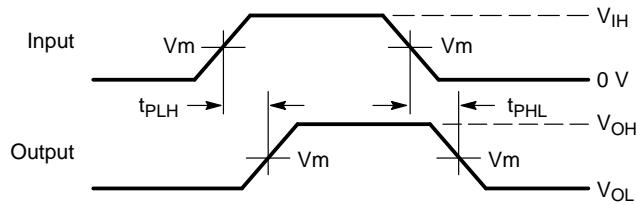


Figure 3. AC (Propagation Delay) Test Circuit

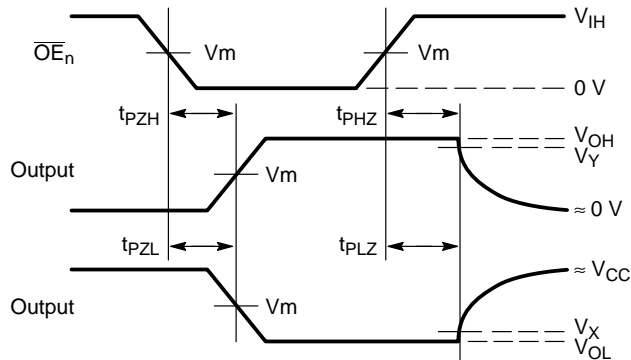
Test	Switch
$t_{PLH}$ , $t_{PHL}$	OPEN
$t_{PLZ}$ , $t_{PZL}$	$V_{CCO} \times 2$ at $V_{CCO} = 3.0\text{ V} - 3.6\text{ V}, 2.3\text{ V} - 2.7\text{ V}, 1.65\text{ V} - 1.95\text{ V}, 1.4\text{ V} - 1.6\text{ V}$
$t_{PHZ}$ , $t_{PZH}$	GND

$C_L = 15\text{ pF}$  or equivalent (includes probe and jig capacitance)  
 $R_L = 2\text{ k}\Omega$  or equivalent  
 $Z_{OUT}$  of pulse generator =  $50\ \Omega$   
 $V_{CCO}$  is the supply voltage referenced to by the output being tested



Waveform 1 - Propagation Delays

$t_R = t_F = 2.0\text{ ns}$ , 10% to 90%;  $f = 1\text{ MHz}$ ;  $t_W = 500\text{ ns}$



Waveform 2 - Output Enable and Disable Times

$t_R = t_F = 2.0\text{ ns}$ , 10% to 90%;  $f = 1\text{ MHz}$ ;  $t_W = 500\text{ ns}$

Figure 4. AC (Propagation Delay) Test Circuit Waveforms

Symbol	Input Pin Output Pin
$V_m$	$V_{CCX}/2$
$V_X$	$V_{OL} \times 0.1$
$V_Y$	$V_{OH} \times 0.9$

# MECHANICAL CASE OUTLINE

## PACKAGE DIMENSIONS

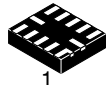
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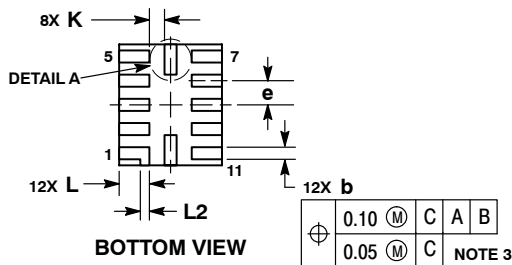
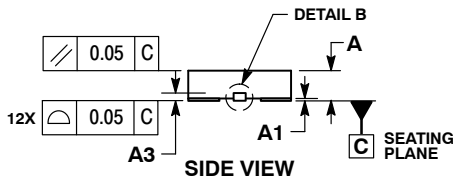
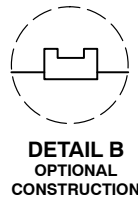
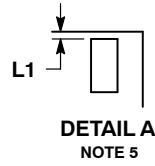
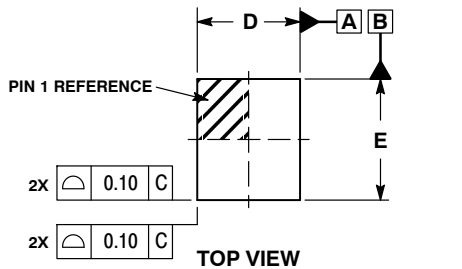
### UQFN12 1.7x2.0, 0.4P

CASE 523AE-01  
ISSUE A

DATE 11 JUN 2007



SCALE 4:1



NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 MM FROM TERMINAL TIP.
4. MOLD FLASH ALLOWED ON TERMINALS ALONG EDGE OF PACKAGE. FLASH 0.03 MAX ON BOTTOM SURFACE OF TERMINALS.
5. DETAIL A SHOWS OPTIONAL CONSTRUCTION FOR TERMINALS.

DIM	MILLIMETERS	
	MIN	MAX
A	0.45	0.55
A1	0.00	0.05
A3	0.127 REF	
b	0.15	0.25
D	1.70 BSC	
E	2.00 BSC	
e	0.40 BSC	
K	0.20	---
L	0.45	0.55
L1	0.00	0.03
L2	0.15 REF	

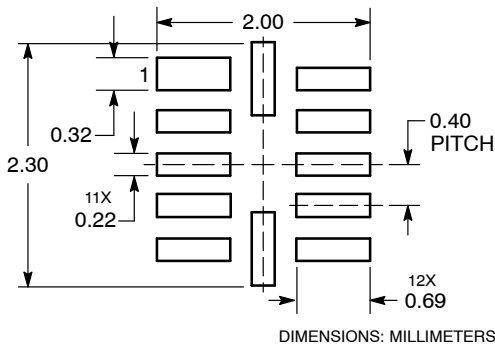
### GENERIC MARKING DIAGRAM\*



- XX = Specific Device Code
- M = Date Code
- = Pb-Free Package

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present.

### MOUNTING FOOTPRINT SOLDERMASK DEFINED



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