Never stop thinking

TC1791

AP32162

Design Guideline for TC1791 Microcontroller Board Layout

Application Note

V1.2 2012-02

Microcontrollers

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Device1

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Page	Subjects (major changes since last revision)
10	Fig-4 changed.

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1 Overview

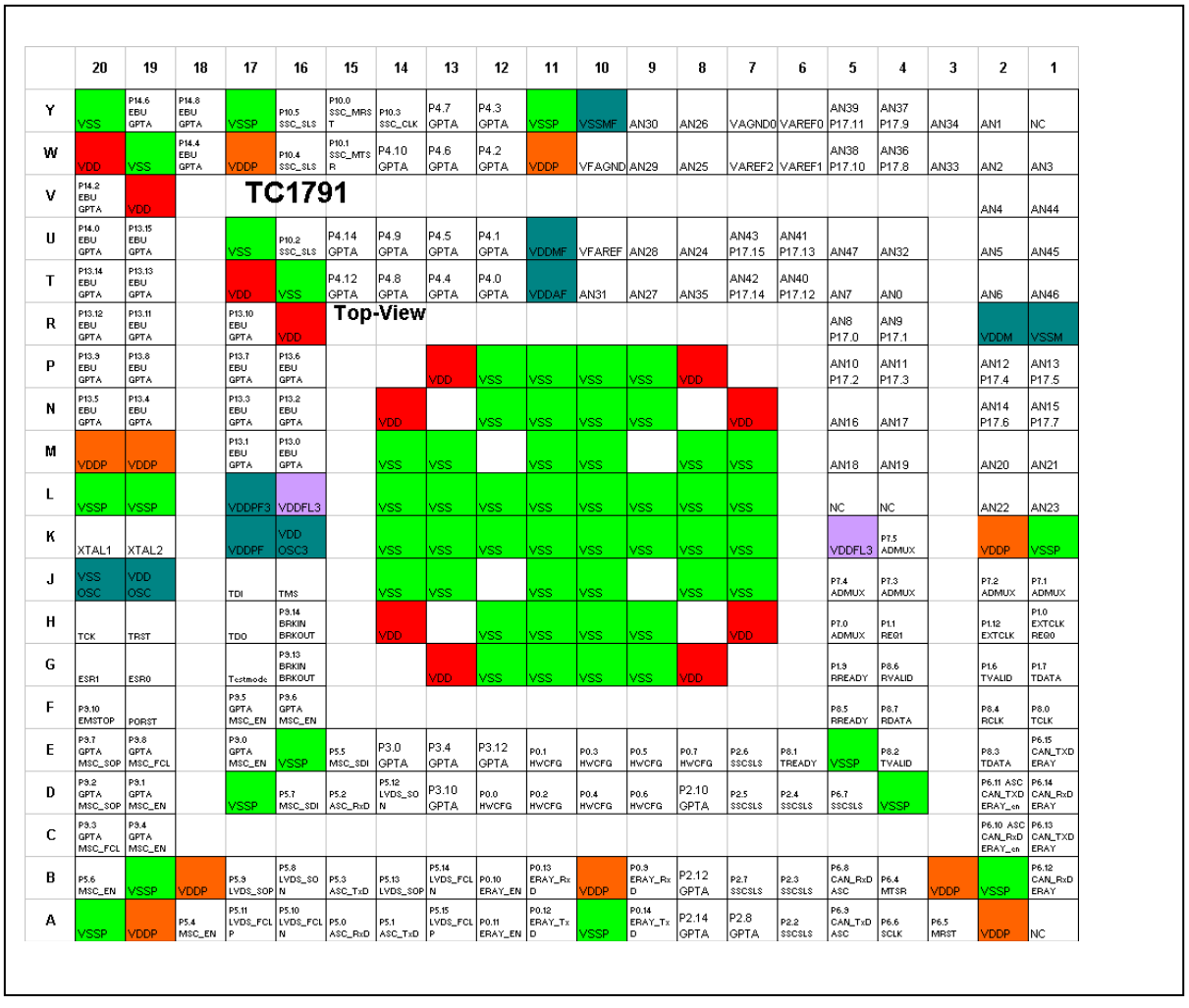
The TC1791 is a 32-Bit microcontroller in a LFBGA-292 package, which requires a PCB carefully designed for electromagnetic compatibility. In addition to the Infineon PCB Design Guidelines for Microcontrollers (AP24026), which gives general design rule informations for PCB design, some product-specific recommendations and guidelines for the TC1791 are discussed here.

1.1 General Information

The microcontroller has three supply domains (VDD=1.3V for Core, VDDP=3.3V for I/O Pad, VDDM=3.3V or 5V for ADC), which should be decoupled individually.

The power supply feeding from the regulator outputs to each domain can be made on a supply layer (POWER).

1.2 Pinout of TC1791



	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
Y	VSS	P14.6 EBU GPTA	P14.8 EBU GPTA	VSSP	P10.5 SSC_SLS	P10.0 SSC_MRST	P10.3 SSC_CLK	P4.7 GPTA	P4.3 GPTA	VSSP	VSSMF	AN30	AN26	VAGND0	VAREF0	AN39 P17.11	AN37 P17.9	AN34	AN1	NC
W	VDD	VSS	P14.4 EBU GPTA	VDDP	P10.4 SSC_SLS	P10.1 SSC_MTSR	P4.10 GPTA	P4.6 GPTA	P4.2 GPTA	VDDP	VFAGND	AN29	AN25	VAREF2	VAREF1	AN38 P17.10	AN36 P17.8	AN33	AN2	AN3
V	P14.2 EBU GPTA	VDD																	AN4	AN44
U	P14.0 EBU GPTA	P13.15 EBU GPTA		VSS	P10.2 SSC_SLS	P4.14 GPTA	P4.9 GPTA	P4.5 GPTA	P4.1 GPTA	VDDMF	VFAREF	AN28	AN24	AN43 P17.15	AN41 P17.13	AN47	AN32		AN5	AN45
T	P13.14 EBU GPTA	P13.13 EBU GPTA		VDD	VSS	P4.12 GPTA	P4.8 GPTA	P4.4 GPTA	P4.0 GPTA	VDDAF	AN31	AN27	AN35	AN42 P17.14	AN40 P17.12	AN7	AN0		AN6	AN46
R	P13.12 EBU GPTA	P13.11 EBU GPTA		P13.10 EBU GPTA	VDD											AN8 P17.0	AN9 P17.1		VDDM	VSSM
P	P13.9 EBU GPTA	P13.8 EBU GPTA		P13.7 EBU GPTA	P13.6 EBU GPTA			VDD	VSS	VSS	VSS	VSS	VDD			AN10 P17.2	AN11 P17.3		AN12 P17.4	AN13 P17.5
N	P13.5 EBU GPTA	P13.4 EBU GPTA		P13.3 EBU GPTA	P13.2 EBU GPTA		VDD		VSS	VSS	VSS	VSS		VDD		AN16	AN17		AN14 P17.6	AN15 P17.7
M	VDDP	VDDP		P13.1 EBU GPTA	P13.0 EBU GPTA		VSS	VSS		VSS	VSS		VSS	VSS		AN18	AN19		AN20	AN21
L	VSSP	VSSP		VDDPF3	VDDFL3		VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS		NC	NC		AN22	AN23
K	XTAL1	XTAL2		VDDPF	VDD OSC3		VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS		VDDFL3	P7.5 ADMUX		VDDP	VSSP
J	VSS OSC	VDD OSC		TDI	TMS		VSS	VSS		VSS	VSS		VSS	VSS		P7.4 ADMUX	P7.3 ADMUX		P7.2 ADMUX	P7.1 ADMUX
H	TCK	TRST		TDO	P9.14 BRKIN BRKOUT		VDD		VSS	VSS	VSS	VSS		VDD		P7.0 ADMUX	P1.1 REQ1		P1.12 EXTCLK	P1.0 EXTCLK REQ0
G	ESR1	ESR0		Testmode	P9.13 BRKIN BRKOUT			VDD	VSS	VSS	VSS	VSS	VDD			P1.9 RREADY	P8.6 RVALID		P1.6 TVALID	P1.7 TDATA
F	P9.10 EMSTOP	PORST		P9.5 GPTA MSC_EN	P9.6 GPTA MSC_EN											P8.5 RREADY	P8.7 RDATA		P8.4 RCLK	P8.0 TCLK
E	P9.7 GPTA MSC_SOP	P9.8 GPTA MSC_FCL		P9.0 GPTA MSC_EN	VSSP	P5.5 MSC_SDI	P3.0 GPTA	P3.4 GPTA	P3.12 GPTA	P0.1 HWCFG	P0.3 HWCFG	P0.5 HWCFG	P0.7 HWCFG	P2.6 SSCSLS	P8.1 TREADY	VSSP	P8.2 TVALID		P8.3 TDATA	P6.15 CAN_TXD ERAY
D	P9.2 GPTA MSC_SOP	P9.1 GPTA MSC_EN		VSSP	P5.7 MSC_SDI	P5.2 ASC_RxD	P5.12 LVDS_SON	P3.10 GPTA	P0.0 HWCFG	P0.2 HWCFG	P0.4 HWCFG	P0.6 HWCFG	P2.10 GPTA	P2.5 SSCSLS	P2.4 SSCSLS	P6.7 SSCSLS	VSSP		P6.11 ASC CAN_TXD ERAY_en	P6.14 CAN_RxD ERAY
C	P9.3 GPTA MSC_FCL	P9.4 GPTA MSC_EN																	P6.10 ASC CAN_RxD ERAY_en	P6.13 CAN_TXD ERAY
B	P5.6 MSC_EN	VSSP	VDDP	P5.9 LVDS_SOP	P5.8 LVDS_SON	P5.3 ASC_TxD	P5.13 LVDS_SOP	P5.14 LVDS_FCLN	P0.10 ERAY_EN	P0.13 ERAY_RxD	VDDP	P0.9 ERAY_RxD	P2.12 GPTA	P2.7 SSCSLS	P2.3 SSCSLS	P6.8 CAN_RxD ASC	P6.4 MTSR	VDDP	VSSP	P6.12 CAN_RxD ERAY
A	VSSP	VDDP	P5.4 MSC_EN	P5.11 LVDS_FCLP	P5.10 LVDS_FCLN	P5.0 ASC_RxD	P5.1 ASC_TxD	P5.15 LVDS_FCLP	P0.11 ERAY_EN	P0.12 ERAY_TxD	VSSP	P0.14 ERAY_TxD	P2.14 GPTA	P2.8 GPTA	P2.2 SSCSLS	P6.9 CAN_TxD ASC	P6.6 SCLK	P6.5 MRST	VDDP	NC

Figure 1 Pinout of TC1791 (BGA-292):

2 PCB Design Recommendations

- To minimize the EMI radiation on the PCB the following signals have to be considered as critical:
  - LVDS Pins
  - MLI Pins

- MSC Pins
- ERAY Pins
- Supply Pins

Route these signals with adjacent ground reference and avoid signal and reference layer changes.

Route them as short as possible.

Routing ground on each side can help to reduce coupling to other signals.

- For unused **"Output, Supply, Input and I/O "** pins following points must be considered:

1. Supply Pins (Modules)	• See the User´s Manual.
2. I/O-Pins	• Should be configured as output and driven to static low in the weakest driver mode in order to improve EMI behaviour. Confuguration of the I/O as input with pullup is also possible. • Solderpad should be left open and not be connected to any other net (layout isolated PCB-pad only for soldering).
3. Output Pins including LVDS	• Should be driven static in the weakest driver mode. • If static output level is not possible, the output driver should be disabled. • Solderpad should be left open and not be connected to any other net (layout isolated PCB-pad only for soldering).
4.Input Pins without internal pull device	• For pins with alternate function see product target specification to define the necessary logic level. • Should be connected with high-ohmic resistor to GND (range 10k – 1Meg) wherever possible. No impact on design is however expected if a direct connection to GND is made. • Groups of 8 pins can be used to reduce number of external pull-up/down devices (keep in mind leakage current).
5. Input Pins with internal pull device	• For pins with alternate function see product specification to define the necessary logic level • Should be configured as pull-down and should be activated static low (exception: if the User´s Manual requires high level for alternate functions). No impact on design is expected if static high level is activated. • Solderpad should not be connected to any other net (isolated PCB-pad only for soldering)

- The ground system must be designed as follows:

  - Separate analog and digital grounds.

  - The analog ground must be separated into two groups:

    1. Ground for OSC and PLL (VSSOSC for VDDOSC, VDDOSC3, VDDPF and VDDPF3) as common star point.

    2. Ground for ADC (VSSM for VDDM, VSSMF for VDDMF/VDDAF) as common star point.

- To reduce the radiation / coupling from the oscillator circuit, a separated ground island on the GND layer should be made. This ground island can be connected at one point to the GND layer. This helps to keep noise generated by the oscillator circuit locally on this separated island. The ground connections

of the load capacitors and VSSOSC should also be connected to this island. Traces for the load capacitors and Xtal should be as short as possible.

- The power distribution from the regulator to each power plane should be made over filters (see Figure 2).
- RC Filters can be inserted in the supply paths at the regulator output and at the branchings to other module supply pins like VDDOSC, VDDOSC3, VDDFL3, VDDPF, VDDPF3, VDDM, VDDMF, VDDAF (see Figure 2). Using inductance or ferrite beads (5 – 10 µH) instead of the resistors can improve the EME behaviour of the circuit and reduce the radiation up to ~10dBµV on the related supply net.
- OCDS must be disabled.
- Select weakest possible driver strengths and slew rates for all I/Os (see Scalable Pads AppNote AP32111).
- Use lowest possible frequency for SYSCLK.
- Avoid cutting the GND plane by via groups. A solid GND plane must be designed.

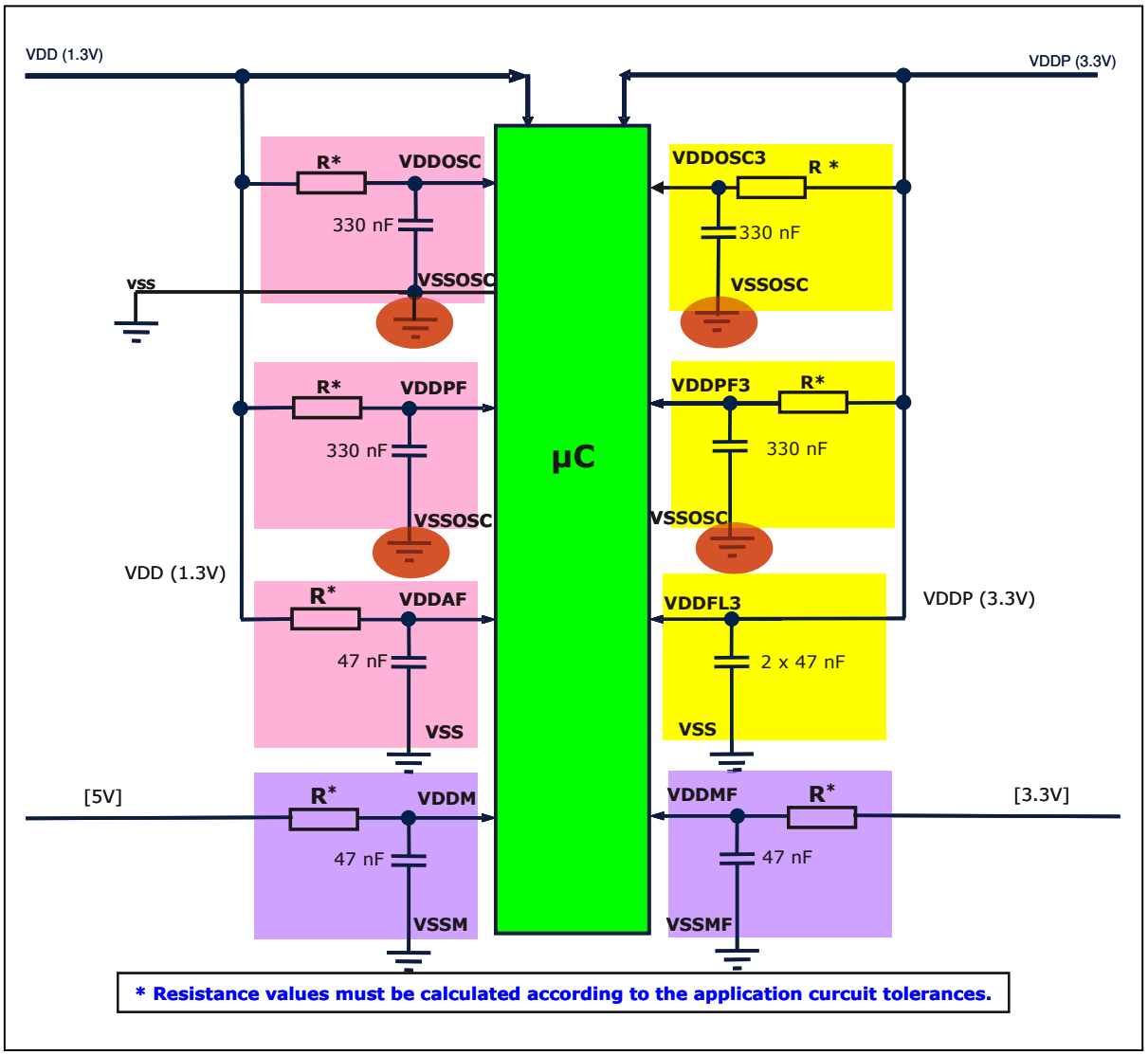


Figure 2 Filtering of VDDOSC, VDDOSC3, VDDFL3, VDDPF, VDDPF3, VDDM, VDDMF, VDDAF supply pins

2.1 Decoupling

- All supply domains of TC1791 should be decoupled separately (see decoupling placement example in Figure 3).
- Type of capacitors:
  - Values: 47 nF, 100 nF, 330 nF
  - X7R Ceramic Multilayer (low ESR and low ESL)
- All supply pins should be connected first to the dedicated decoupling capacitor and then from the capacitors over vias to the power planes.
- All VSS pins should be connected to the GND.
- The decoupling capacitors should be placed directly under the IC or if necessary, some capacitors can be placed on top layer close to the supply pins of the IC.
- Ground plane on bottom layer can be used to connect the capacitors. If no plane is used, they should be connected with vias to the GND layer.
- Multiple vias should be used at capacitors to get a low impedance connection between capacitors and POWER/GND planes or pins.
- All capacitors must be placed as close as possible to the related supply pin group.

In Figure 3 shown examples are based on device power supply concept and implementation. Alternative implementations are also acceptable and must be evaluated within application by customer.

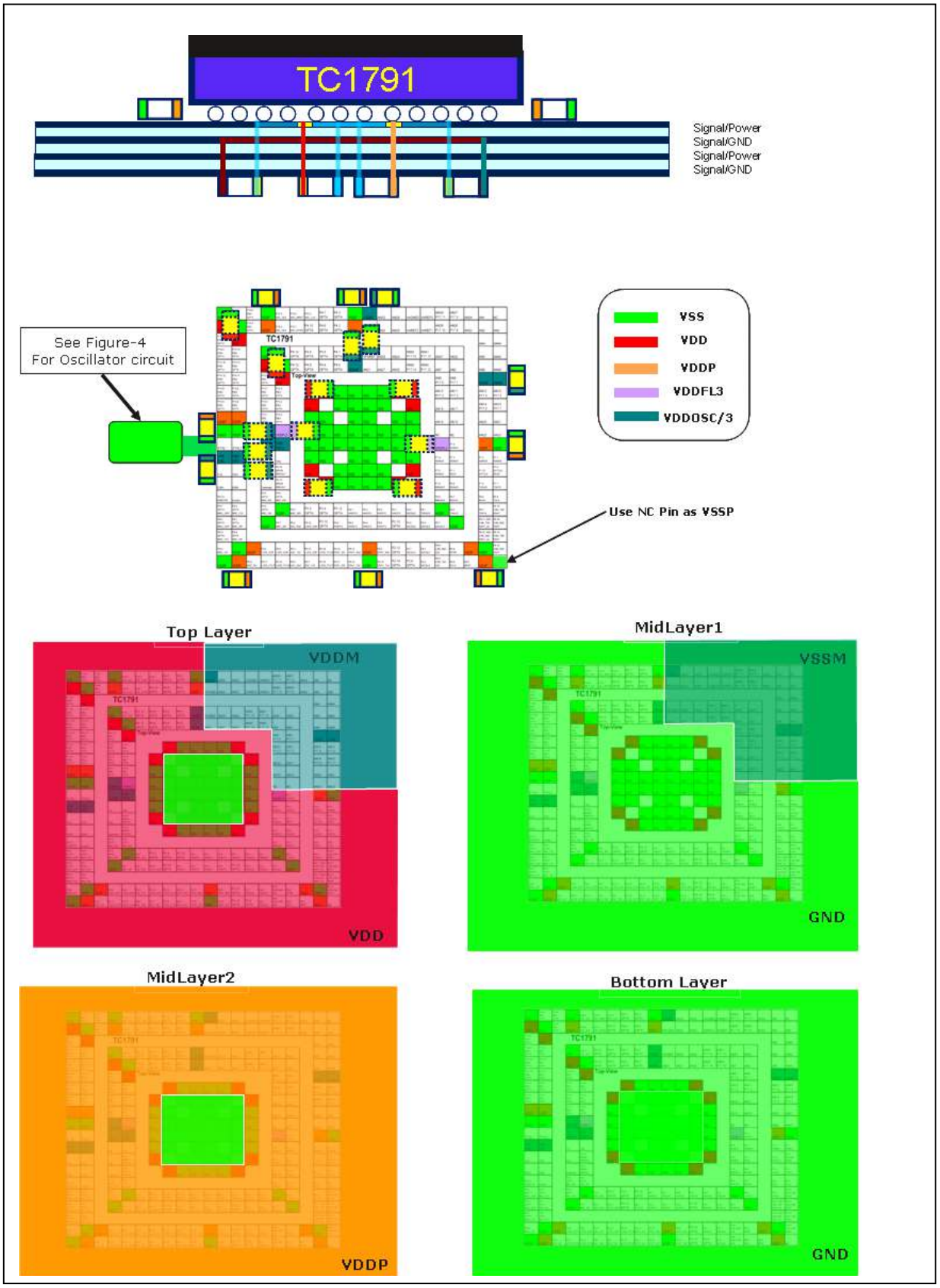


Figure 3 Capacitor Placement Example for Decoupling of TC1791 (LFBGA-292) on a four layer board

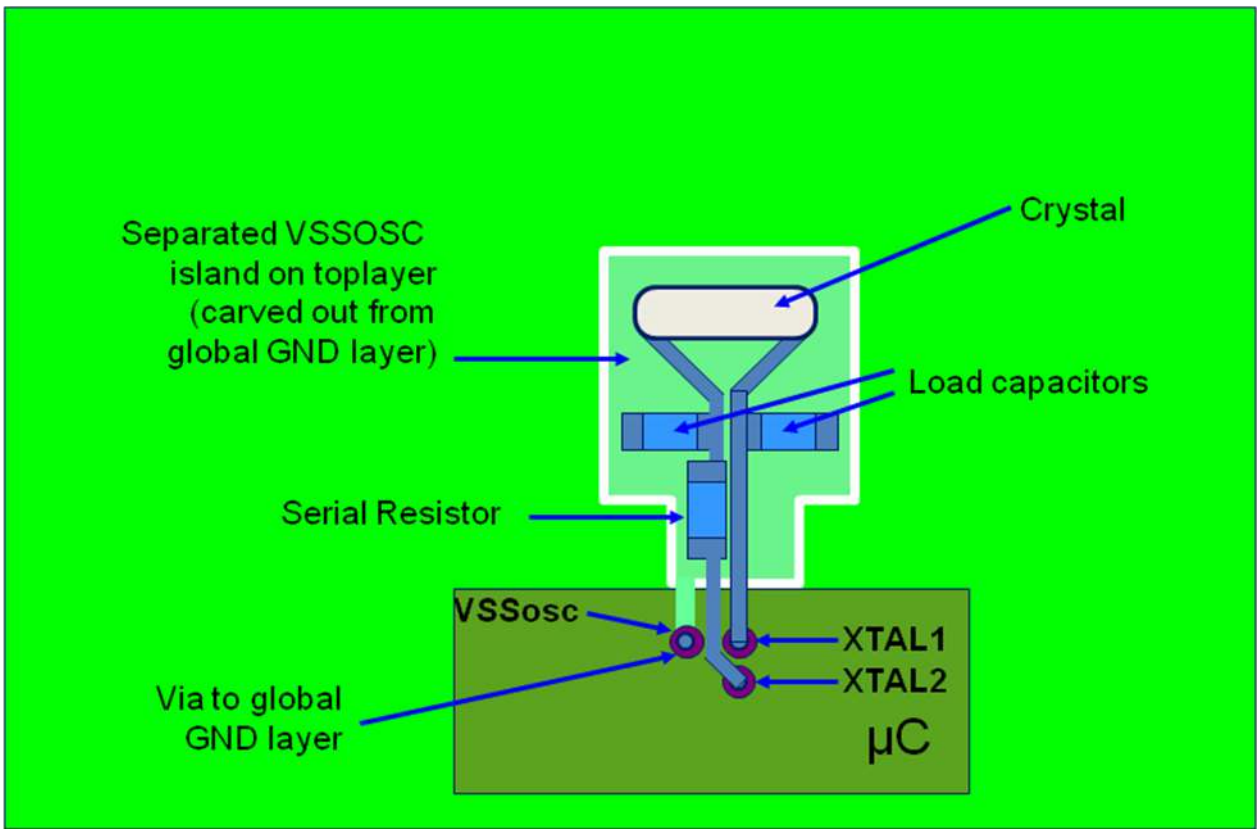


Figure 4 Layout Proposal Oscillator Circuit

2.2 Decoupling Capacitor List:

Capacitor	Supply	Pins(BGA-292)
47 nF	VDD	G8/H7
47 nF	VDD	G13/H14
47 nF	VDD	N7/P8
47 nF	VDD	N14/P13
47 nF	VDD	R16/T17
47 nF	VDD	V19/W20
47 nF	VDDP	A2/B3
47 nF	VDDP	B10
47 nF	VDDP	A19/B18
47 nF	VDDP	K2
47 nF	VDDP	M19/M20
47 nF	VDDP	W11
47 nF	VDDP	W17
330 nF	VDDOSC	J19
330 nF	VDDOSC3	K16
47 nF	VDDFL3	K5
47 nF	VDDFL3	L16
330 nF	VDDPF	K17
330 nF	VDDPF3	L17
47 nF	VDDM	R2
47 nF	VDDMF	U11
47 nF	VDDAF	T11

Note: This application note contains design recommendations from Infineon Technologies point of view. Effectiveness and performance of the final application implementation must be validated by customer, based on dedicated implementation choices.

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