AMC7820

SBAS231B – MARCH 2002

ANALOG MONITORING AND CONTROL

FEATURES

- 100kHz SAMPLING RATE 12-BIT ADC
- 8 ANALOG INPUT CHANNELS
- THREE 12-BIT DACS
- NINE OPERATIONAL AMPLIFIERS
- THERMISTOR CURRENT SOURCE
- INTERNAL 2.5V REFERENCE
- SPI SERIAL INTERFACE
- 3V LOGIC COMPATIBLE
- SINGLE +5V SUPPLY
- LOW POWER: 40mW
- TQFP-48 PACKAGE

APPLICATIONS

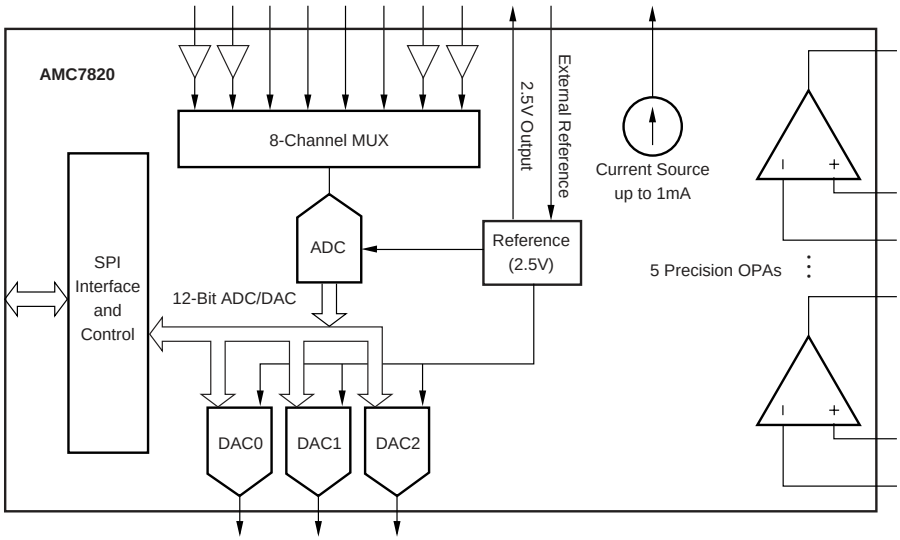
- CW LASER AND PUMP LASER CURRENT CONTROL IN DWDM
- TEC COOLER CURRENT CONTROL IN DWDM
- OPTICAL POWER MONITORING
- TUNABLE LASER

DESCRIPTION

The AMC7820 is a complete analog monitoring and control circuit that includes an 8-channel, 12-bit Analog-to-Digital Converter (ADC), three 12-bit Digital-to-Analog Converters (DACs), nine operational amplifiers, a thermistor current source, an internal +2.5V reference, and an SPI™ serial interface. External reference may be applied. Typical power dissipation is 40mW. For the ADC, the unbuffered analog input range is 0V to +5.0V, and the buffered analog common-mode input range is 0V to +3.8V. For the DACs, the analog output range is 0V to +2.5V or 0V to +5.0V.

The AMC7820 is ideal for multichannel applications where low power and small size are critical. The AMC7820 is available in a TQFP-48 package and is fully specified and tested over the –40°C to +85°C temperature range.

SPI is a trademark of Motorola.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

ABSOLUTE MAXIMUM RATINGS[1]

AV_{DD}, DV_{DD}, BV_{DD} to GND	–0.3V to +6V
Digital Input Voltage to GND	–0.3V to BV_{DD} + 0.3V
Analog Input Voltage to GND	–0.3V to AV_{DD} + 0.3V
Input Current: Continuous	±20mA
Momentary	±100mA
Operating Temperature Range	–40°C to +105°C
Storage Temperature Range	–65°C to +150°C
Junction Temperature (T_J Max)	+150°C
TQFP Package	
Power Dissipation	$(T_J$ Max – $T_A)/\theta_{JA}$
θ_{JC} Thermal Impedance	15°C/W
θ_{JA} Thermal Impedance	60°C/W
Lead Temperature (soldering)	
Vapor Phase (60s)	+220°C
Infrared (15s)	+220°C

NOTE: (1) Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability.

ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGE/ORDERING INFORMATION

PRODUCT	PACKAGE-LEAD	PACKAGE DESIGNATOR[1]	SPECIFIED TEMPERATURE RANGE	SPECIFIED PACKAGE MARKING	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
AMC7820Y	TQFP-48	PFB	–40°C to +85°C	AMC7820Y	AMC7820Y/250	Tape and Reel, 250
AMC7820Y	"	"	"	AMC7820Y	AMC7820Y/2K	Tape and Reel, 2000

NOTE: (1) For the most current specifications and package information, refer to our web site at www.ti.com.

ELECTRICAL CHARACTERISTICS

At –40°C to +85°C, AV_{DD}, DV_{DD}, BV_{DD} = +5V, using external 2.5V reference, unless otherwise noted.

PARAMETER	CONDITION	AMC7820 MIN	AMC7820 TYP	AMC7820 MAX	UNITS
ADC ANALOG INPUTS[1]	Channels 2-5				
Input Voltage Range		0		2 • V_{REF}	V
Input Impedance			5		MΩ
Input Capacitance			15		pF
Input Leakage Current			±1		µA
ADC					
Resolution				12	Bits
No Missing Codes		12			Bits
Integral Linearity			±1	±2	LSB[2]
Differential Linearity			±1		LSB
Offset Error			±2	±5	LSB
Offset Error Drift			±4		ppm/°C
Offset Error Match	Channels 2-5		0.5	1	LSB
Gain Error			±0.3	±1.5	%
Gain Error Match	Channels 2-5		0.3	1	LSB
Noise			150		µVrms
Power-Supply Rejection	+AV_{DD}, +DV_{DD} = +5V ±5%		1.2		LSB
Throughput Rate			100		kHz
Total Conversion Time	Scan All 8 Channels		80		µs
DAC[3]					
Output Voltage Range	DAC_OUT_SET Connected to DAC_OUT	0		V_{REF}	V
	DAC_OUT_SET = AGND	0		2 • V_{REF}	V
Output Current	Refer to the Characteristic Curves		±1		mA
Resolution				12	Bits
Integral Linearity[4]			±4	±8	LSB
Monotonicity		12			Bits
Differential Linearity			±0.1	±1	LSB
Offset Error	Output Range 0 – V_{REF}		±0.5	±5	mV
	Output Range 0 – 2 • V_{REF}		±1	±10	mV
Offset Error Drift			±4		ppm/°C
Gain Error	Output Range = 0V to 2 • V_{REF} or 0V to V_{REF}		±0.3	±1.5	%
Settling Time	Step Between Codes 1024 and 2048		3		µs
Code Change Glitch Impulse	1LSB Change Around Major Carry		20		nV-s
THERMISTOR CURRENT SOURCE					
Output Current Range		10	100	1000	µA
Output Current Accuracy	R_{ISET} = 100kΩ	98		102	µA
Output Impedance	R_{ISET} = 100kΩ		500		MΩ
Compliance Voltage		0		3	V
Power-Supply Rejection Ratio			60		dB

ELECTRICAL CHARACTERISTICS (Cont.)

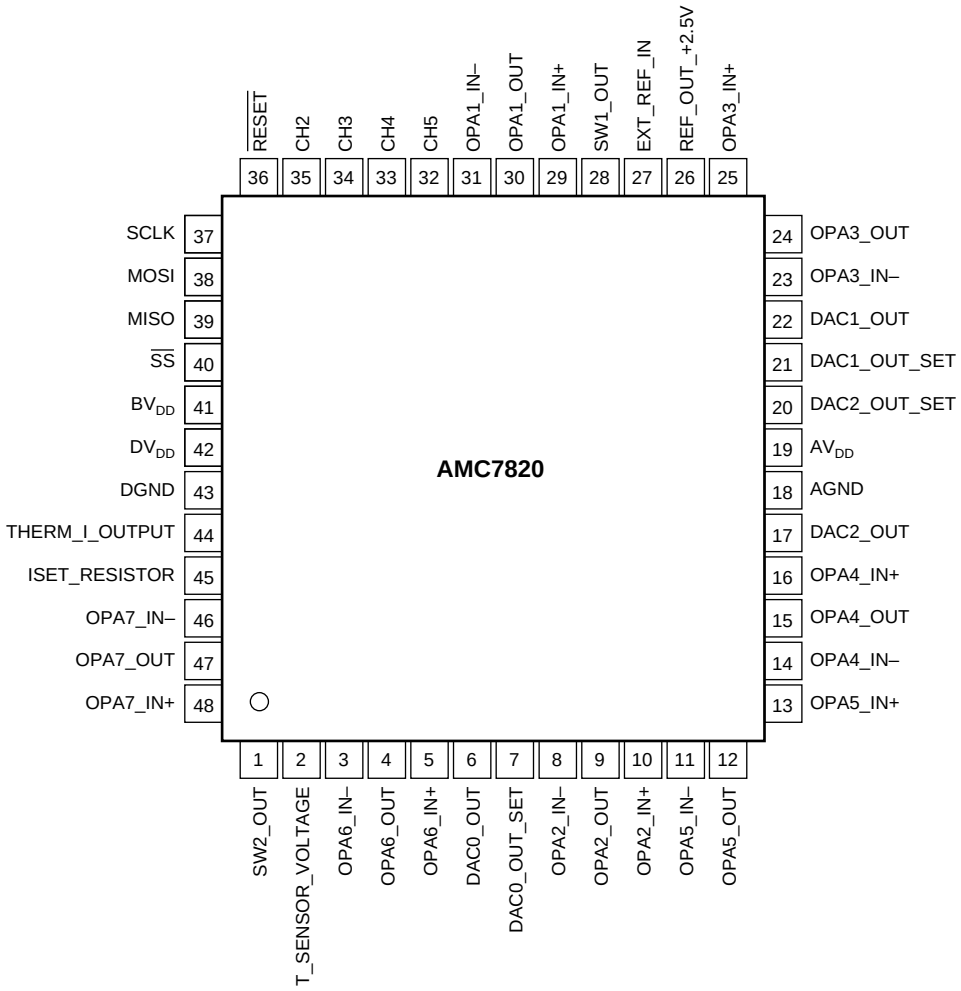
At –40°C to +85°C, AV_{DD}, DV_{DD}, BV_{DD} = +5V, using external 2.5V reference, unless otherwise noted.

PARAMETER	CONDITION	AMC7820 MIN	AMC7820 TYP	AMC7820 MAX	UNITS
VOLTAGE REFERENCE (V_{REF})					
Internal Reference Voltage		2.45	2.50	2.55	V
Internal Reference Drift[5]	0°C to +85°C		±10		ppm/°C
	–40°C to +85°C		±30		ppm/°C
2.5V Output Impedance (pin 26)			0.5		Ω
2.5V Output Current (pin 26)			±1		mA
Short-Circuit Current (pin 26)			±15		mA
External Reference Voltage Range (pin 27)		2.45	2.50	2.55	V
External Reference Input Resistance			10		kΩ
External Reference Input Capacitance			5		pF
OP AMP CHARACTERISTICS[6]					
Input Offset Voltage			±0.5	±4	mV
vs Temperature			±2		µV/°C
vs Power Supply			50		µV/V
Input Bias Current[7]	T_A = +25°C		±2	±50	pA
	T_A = –40°C to +85°C	See [redacted]istics			
Input Offset Current[7]	T_A = +25°C		±1	±50	pA
Input Voltage Noise	f = 0.1Hz to 10Hz		6		µVp-p
Input Voltage Noise Density	f = 1kHz		26		nV/√Hz
Current Noise Density	f = 1kHz		0.6		fA/√Hz
Common-Mode Voltage Range		–0.2		AV_{DD} – 1.2	V
Common-Mode Rejection Ratio[8]	–0.2V < V_{CM} < AV_{DD} – 1.2V	74	90		dB
Open-Loop Gain[8]	R_L = 25kΩ, 125mV < V_O < AV_{DD} – 125mV	100	120		dB
Gain-Bandwidth Product	G = 1		3		MHz
Slew Rate	G = 1		1.2		V/µs
Settling Time: 0.1%	2V Step, C_L = 100pF, G = 1, R_L = 10kΩ		3		µs
Voltage Output Swing from Rail	R_L = 25kΩ		40		mV
Closed-Loop Output Impedance			0.4		Ω
Output Current	See Typical Characteristics		±1		mA
Short-Circuit Current			±18		mA
DIGITAL INPUT/OUTPUT					
Logic Level:					
V_{IH}	BV_{DD} = 5V, $\|I_{IH}\| \leq 10\mu A$	3.5		BV_{DD} + 0.3	V
V_{IL}	BV_{DD} = 5V, $\|I_{IL}\| \leq 10\mu A$	0		0.8	V
V_{OH}	BV_{DD} = 5V, I_{OH} = –3mA	4.0		BV_{DD}	V
V_{OL}	BV_{DD} = 5V, I_{OL} = 3mA	0		0.4	V
Logic Level:					
V_{IH}	BV_{DD} = 3V, $\|I_{IH}\| \leq 10\mu A$	2.1		BV_{DD} + 0.3	V
V_{IL}	BV_{DD} = 3V, $\|I_{IL}\| \leq 10\mu A$	0		0.6	V
V_{OH}	BV_{DD} = 3V, I_{OH} = –3mA	2.4		BV_{DD}	V
V_{OL}	BV_{DD} = 3V, I_{OL} = 3mA	0		0.4	V
Input Capacitance			5		pF
POWER-SUPPLY REQUIREMENTS					
Power-Supply Voltage					
AV_{DD}, DV_{DD}	Specified Performance	4.75	5	5.25	V
BV_{DD}	Specified Performance	2.7		5.25	V
Quiescent Current of AV_{DD}			8	12	mA
Quiescent Current of DV_{DD}			0.3	0.75	mA
Quiescent Current of BV_{DD}			0.01	0.1	mA
Power Dissipation			40		mW
TEMPERATURE RANGE					
Specified Performance		–40		+85	°C
Storage		–65		+150	°C

NOTES: (1) For channels 2-5, fed into MUX directly. (2) LSB means Least Significant Bit. (3) DACs are tested without output load. (4) Measured from code 010 to FFF. (5) Internal reference voltage has been optimized for lowest drift from 0°C to +85°C. (6) Applies to all amplifiers; see Figure 2. (7) Offset current will double for each 10°C of temperature increase. See Operational Amplifier section. (8) Ensured by design.

PIN CONFIGURATION

Top View **TQFP**



PIN DESCRIPTIONS (Refer to Figure 1, Block Diagram)

PIN	DESIGNATOR	DESCRIPTION
1	SW2_OUT	Output from SW2. This pin connects to OPA7_OUT when SW2 is enabled; connects to the output of SW3 when SW2 is disabled.
2	T_SENSOR_VOLTAGE	Output of temperature sensor (Thermistor) voltage buffer.
3	OPA6_IN–	Inverting Input of OPA6
4	OPA6_OUT	Output of OPA6
5	OPA6_IN+	Noninverting Input of OPA6
6	DAC0_OUT	Output of DAC0
7	DAC0_OUT_SET	This pin determines the full-scale output of DAC0. When tied to DAC0_OUT, the full-scale output equals V_{REF}. When connected to AGND, full-scale output equals 2 • V_{REF}.
8	OPA2_IN–	Inverting Input of OPA2
9	OPA2_OUT	Output of OPA2
10	OPA2_IN+	Noninverting Input of OPA2
11	OPA5_IN–	Inverting Input of OPA5
12	OPA5_OUT	Output of OPA5
13	OPA5_IN+	Noninverting Input of OPA5
14	OPA4_IN–	Inverting Input of OPA4
15	OPA4_OUT	Output of OPA4
16	OPA4_IN+	Noninverting Input of OPA4
17	DAC2_OUT	Output of DAC2
18	AGND	Analog Ground
19	AV_{DD}	Analog Power Supply (+5V)
20	DAC2_OUT_SET	This pin determines the full-scale output of DAC2. When tied to DAC2_OUT, the full-scale output equals V_{REF}. When connected to AGND, full-scale output equals 2 • V_{REF}.
21	DAC1_OUT_SET	This pin determines the full-scale output of DAC1. When tied to DAC1_OUT, the full-scale output equals V_{REF}. When connected to AGND, full-scale output equals 2 • V_{REF}.
22	DAC1_OUT	Output of DAC1
23	OPA3_IN–	Inverting Input of OPA3
24	OPA3_OUT	Output of OPA3
25	OPA3_IN+	Noninverting Input of OPA3
26	REF_OUT_+2.5V	$+2.5V_{OUT}$
27	EXT_REF_IN	An external reference can be connected here. Also can be used as a filter for internal reference.
28	SW1_OUT	Output from SW1. This pin connects to DAC2_OUT when SW1 is enabled; connects to AGND when SW1 is disabled.
29	OPA1_IN+	Noninverting Input of OPA1
30	OPA1_OUT	Output of OPA1
31	OPA1_IN–	Inverting Input of OPA1
32	CH5	Analog Input of Channel 5
33	CH4	Analog Input of Channel 4
34	CH3	Analog Input of Channel 3
35	CH2	Analog Input of Channel 2
36	$\overline{\text{RESET}}$	Reset Input. Logic LOW on this pin will cause the part to perform a hardware reset.
37	SCLK	Serial Clock Input
38	MOSI	Master Out, Slave In. Digital data input for the serial interface.
39	MISO	Master In, Slave Out. Digital data output for the serial interface.
40	$\overline{\text{SS}}$	Slave Select Input (active LOW). Data will not be clocked into MOSI unless $\overline{\text{SS}}$ is LOW. When $\overline{\text{SS}}$ is HIGH, MISO is high impedance.
41	BV_{DD}	Interface Power Supply. Connects to 3V for 3V logic; connects to 5V for 5V logic.
42	DV_{DD}	Digital Power Supply (+5V)
43	DGND	Digital Ground
44	THERM_I_OUTPUT	Current source output to drive the thermistor.
45	ISET_RESISTOR	The resistor connected to this pin sets the current output from the pin THERM_I_OUTPUT.
46	OPA7_IN–	Inverting Input of OPA7
47	OPA7_OUT	Output of OPA7
48	OPA7_IN+	Noninverting Input of OPA7

TIMING CHARACTERISTICS

At –40°C to +85°C, $+AV_{DD}$ = $+DV_{DD}$ = +5V, V_{REF} = +2.5V, $+BV_{DD}$ = +5V, unless otherwise noted.

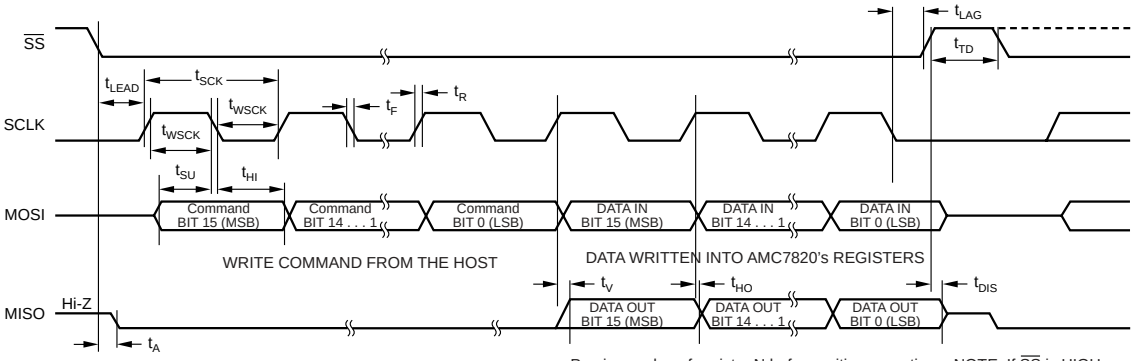
PARAMETER	SYMBOL	MIN	MAX	UNITS
SCLK Period	t_{SCK}	30		ns
SCLK HIGH or LOW Time	t_{WSCK}	15		ns
Rise Time	t_R		30	ns
Fall Time	t_F		30	ns
Enable Lead Time	t_{LEAD}	15		ns
Enable Lag Time	t_{LAG}	15		ns
Sequential Transfer Delay	t_{TD}	30		ns
Data Setup Time	t_{SU}	10		ns
Data Hold Time (inputs)	t_{HI}	10		ns
Slave Access Time	t_A		15	ns
Data Valid	t_V		10	ns
Data Hold Time (outputs)	t_{HO}	0		ns
Slave MISO Disable Time	t_{DIS}		15	ns

TIMING CHARACTERISTICS

At –40°C to +85°C, $+AV_{DD}$ = $+DV_{DD}$ = +5V, V_{REF} = +2.5V, $+BV_{DD}$ = +3V, unless otherwise noted.

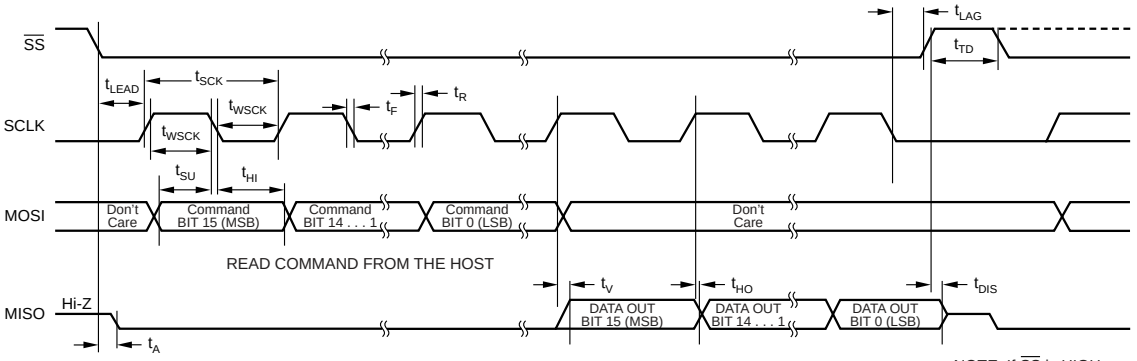
PARAMETER	SYMBOL	MIN	MAX	UNITS
SCLK Period	t_{SCK}	40		ns
SCLK HIGH or LOW Time	t_{WSCK}	20		ns
Rise Time	t_R		30	ns
Fall Time	t_F		30	ns
Enable Lead Time	t_{LEAD}	15		ns
Enable Lag Time	t_{LAG}	15		ns
Sequential Transfer Delay	t_{TD}	30		ns
Data Setup Time	t_{SU}	10		ns
Data Hold Time (inputs)	t_{HI}	10		ns
Slave Access Time	t_A		15	ns
Data Valid	t_V		15	ns
Data Hold Time (outputs)	t_{HO}	0		ns
Slave MISO Disable Time	t_{DIS}		15	ns

TIMING DIAGRAM



WRITE OPERATION

Previous value of register N before writing operation. NOTE: If $\overline{SS}$ is HIGH, MISO is in Hi-Z.



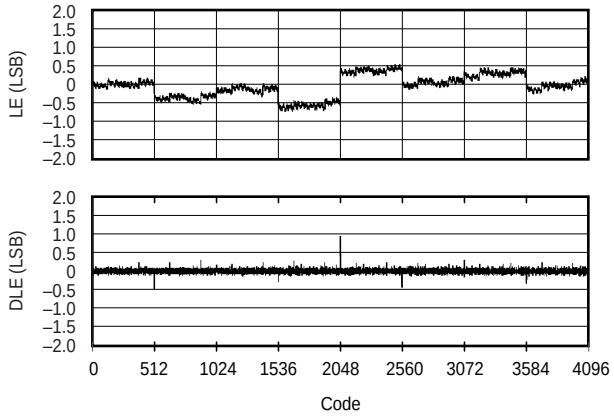
READ OPERATION

DATA READ FROM AMC7820's REGISTERS NOTE: If $\overline{SS}$ is HIGH, MISO is in Hi-Z.

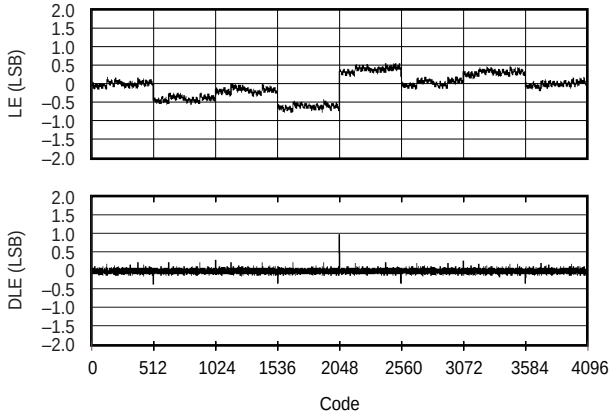
TYPICAL CHARACTERISTICS: ADC

At T_A = +25°C, $+AV_{DD}$, BV_{DD} = +5.0V, V_{REF} = Internal +2.5V, unless otherwise noted.

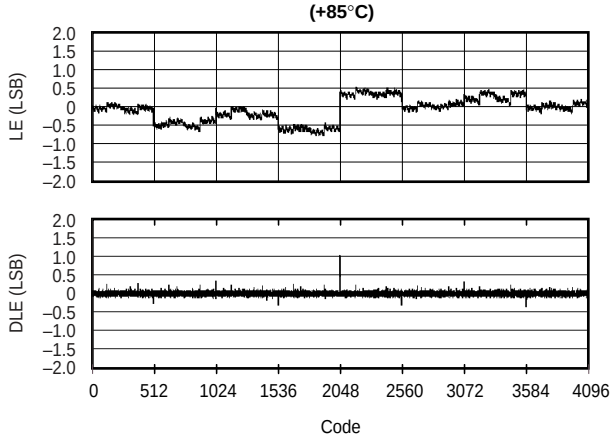
LINEARITY ERROR vs CODE
(–40°C)



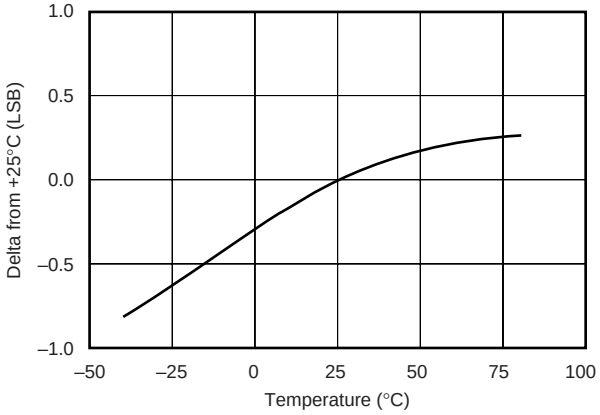
LINEARITY ERROR vs CODE
(+25°C)



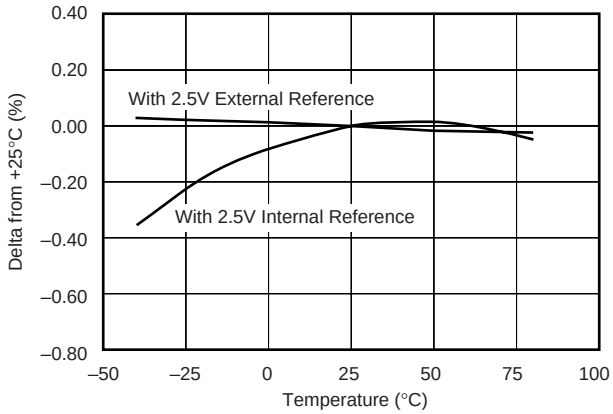
LINEARITY ERROR vs CODE
(+85°C)



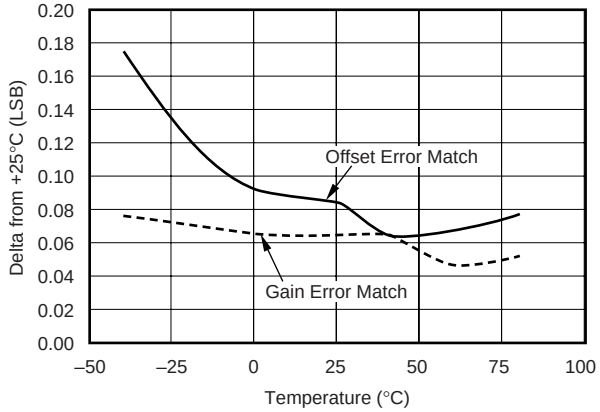
OFFSET vs TEMPERATURE
(Internal or External Reference)



GAIN ERROR vs TEMPERATURE



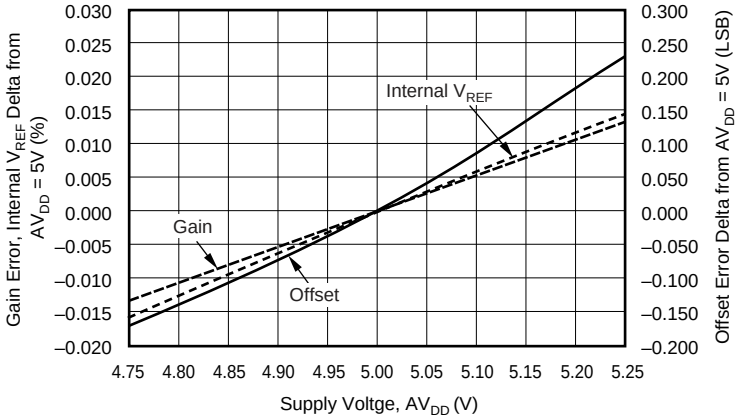
CHANNEL-TO-CHANNEL MATCH vs TEMPERATURE
(Unbuffered Channels 2, 3, 4, 5)



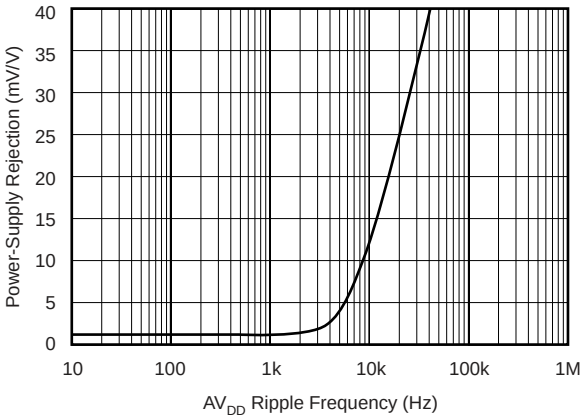
TYPICAL CHARACTERISTICS: ADC (Cont.)

At T_A = +25°C, $+AV_{DD}$, BV_{DD} = +5.0V, V_{REF} = Internal +2.5V, unless otherwise noted.

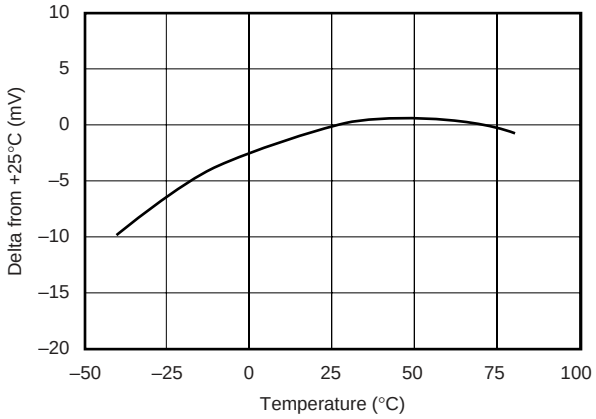
GAIN ERROR, OFFSET ERROR, INTERNAL V_{REF} vs AV_{DD} SUPPLY VOLTAGE (Unbuffered Channels)



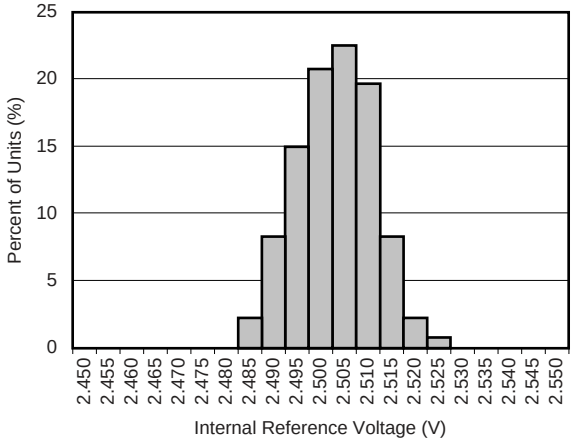
POWER-SUPPLY REJECTION vs FREQUENCY



INTERNAL REFERENCE VOLTAGE vs TEMPERATURE



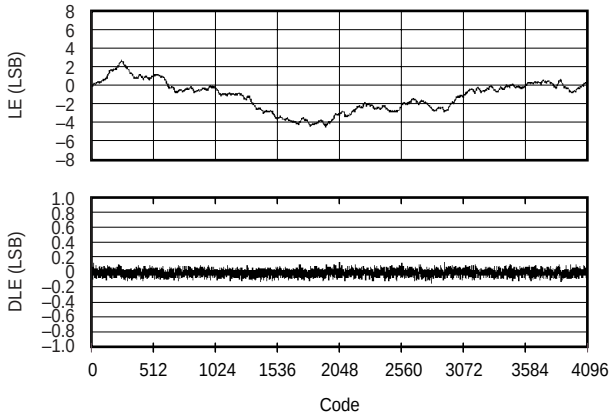
INTERNAL 2.5V REFERENCE DISTRIBUTION



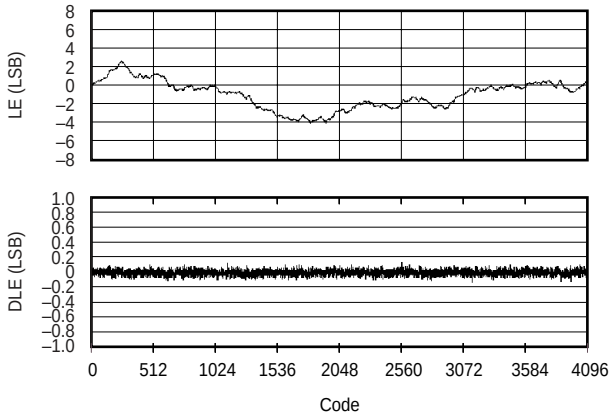
TYPICAL CHARACTERISTICS: DACs (DAC0, DAC1, DAC2)

At T_A = +25°C, $+AV_{DD}$, BV_{DD} = +5.0V, V_{REF} = Internal +2.5V, unless otherwise noted.

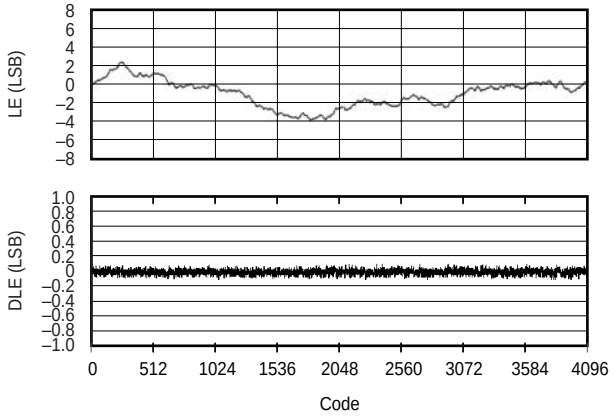
LINEARITY ERROR vs CODE
(–40°C)



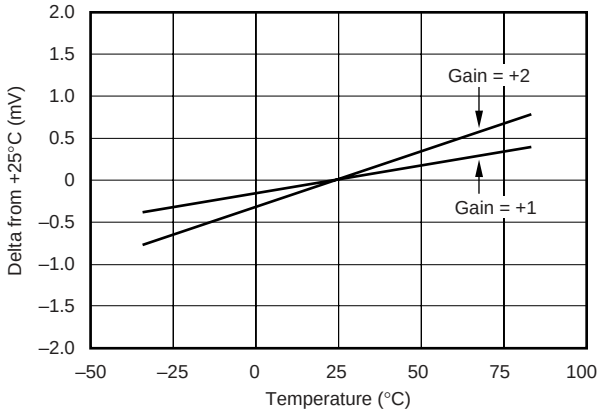
LINEARITY ERROR vs CODE
(+25°C)



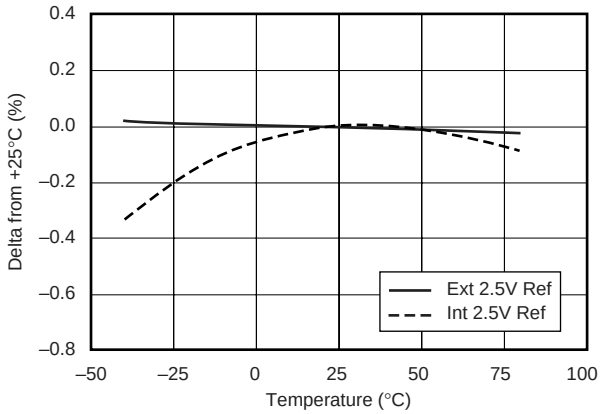
LINEARITY ERROR vs CODE
(+85°C)



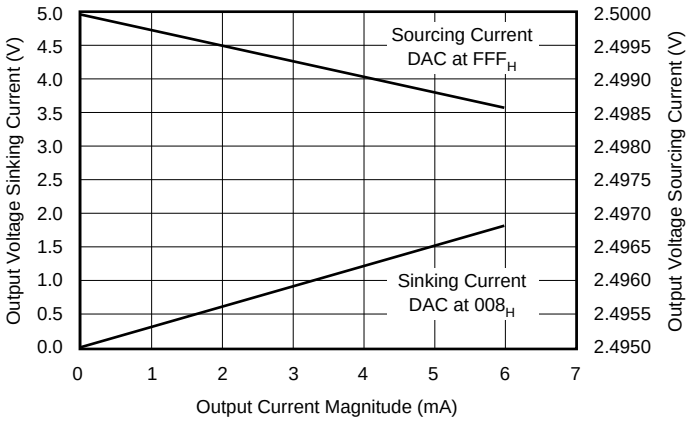
OFFSET ERROR vs TEMPERATURE



GAIN ERROR vs TEMPERATURE
(DAC Gain = +1 or +2)



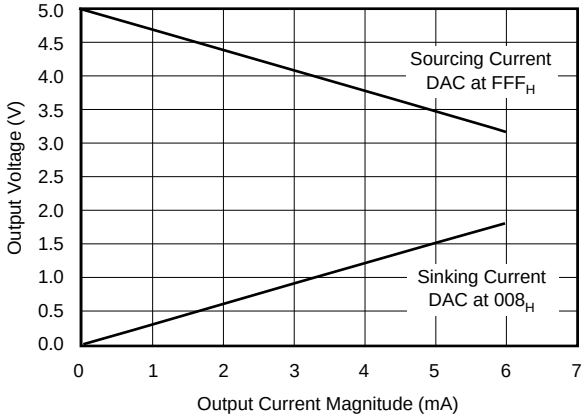
OUTPUT VOLTAGE
vs OUTPUT CURRENT, GAIN = +1



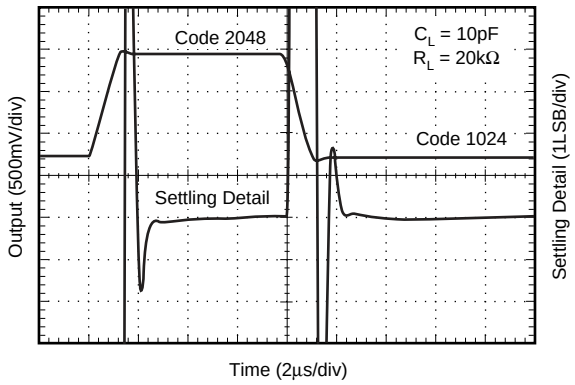
TYPICAL CHARACTERISTICS: DACs (DAC0, DAC1, DAC2) (Cont.)

At T_A = +25°C, $+AV_{DD}$, BV_{DD} = +5.0V, V_{REF} = Internal +2.5V, unless otherwise noted.

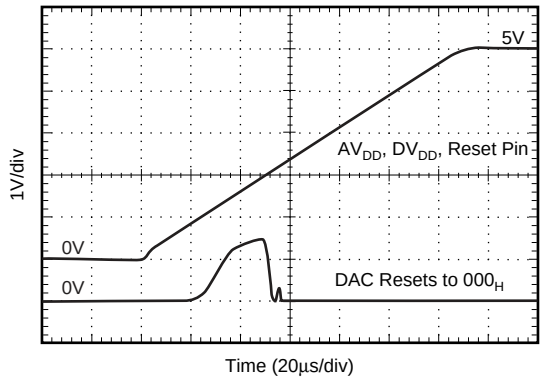
OUTPUT VOLTAGE
vs OUTPUT CURRENT, GAIN = +2



SETTLING TIME, GAIN = +2



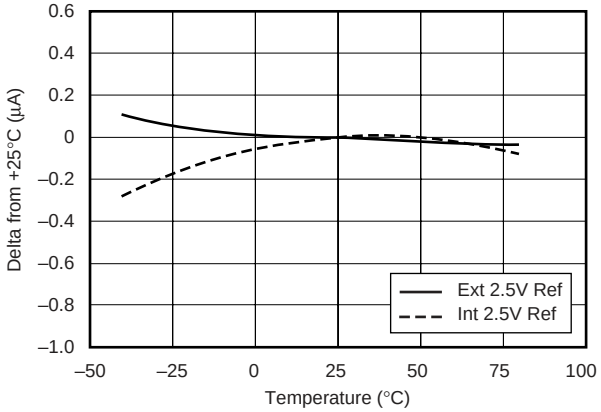
POWER-ON RESET TO 0V



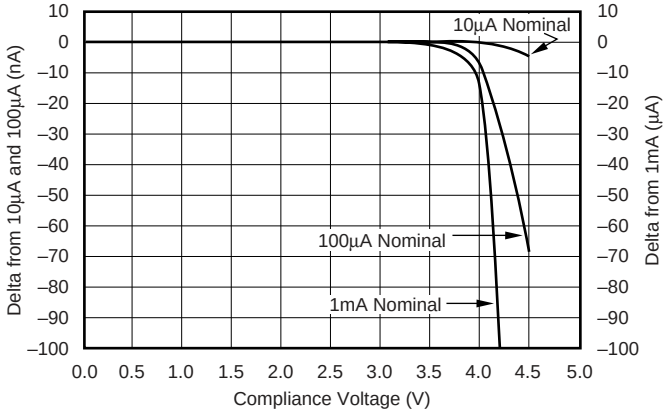
TYPICAL CHARACTERISTICS: Thermistor Current Source (THERM IOUT, Pin 2)

At T_A = +25°C, $+AV_{DD}$, BV_{DD} = +5.0V, V_{REF} = Internal +2.5V, unless otherwise noted.

THERM_I_OUTPUT vs TEMPERATURE

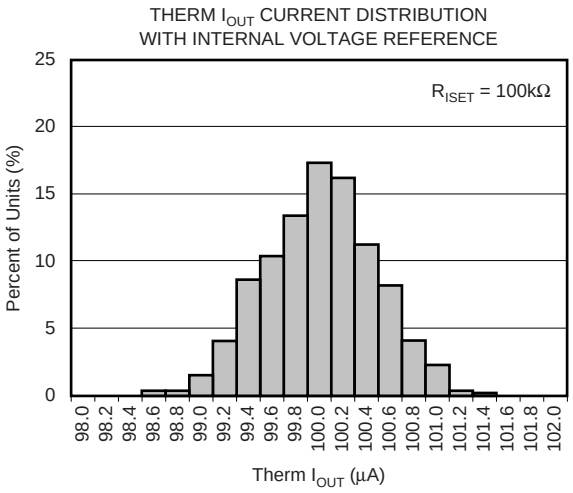


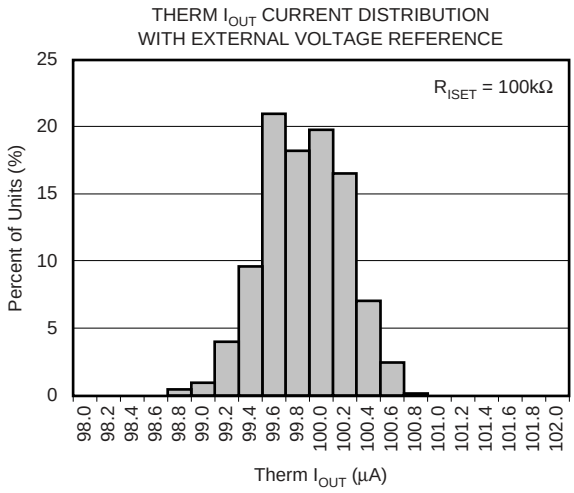
THERM_I_OUTPUT vs COMPLIANCE VOLTAGE



TYPICAL CHARACTERISTICS: Thermistor Current Source (THERM IOUT, Pin 2) (Cont.)

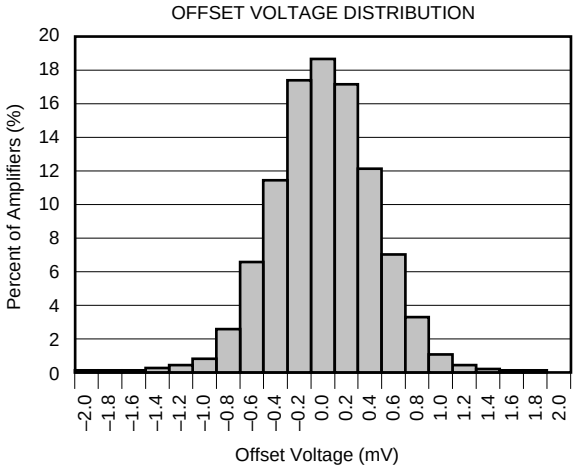
At T_A = +25°C, $+AV_{DD}$, BV_{DD} = +5.0V, V_{REF} = Internal +2.5V, unless otherwise noted.

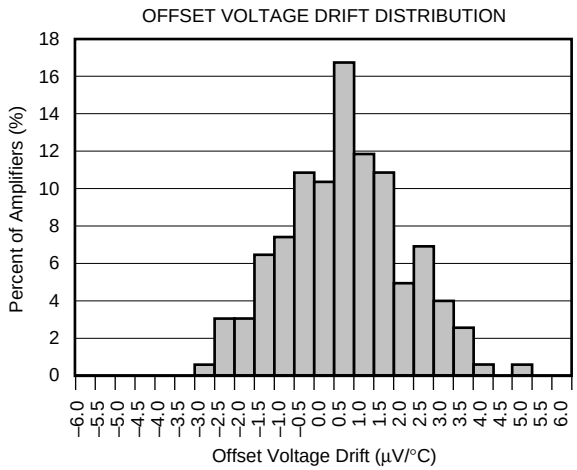


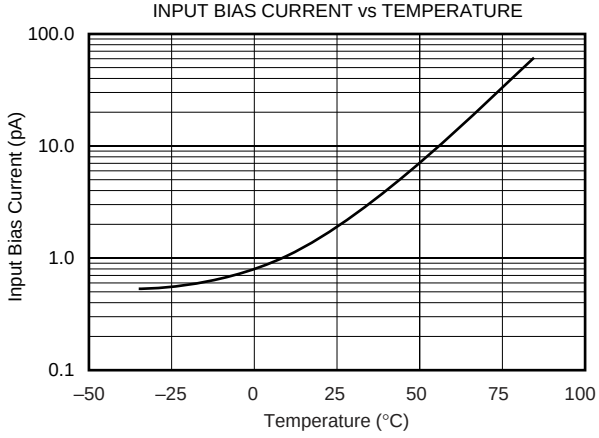


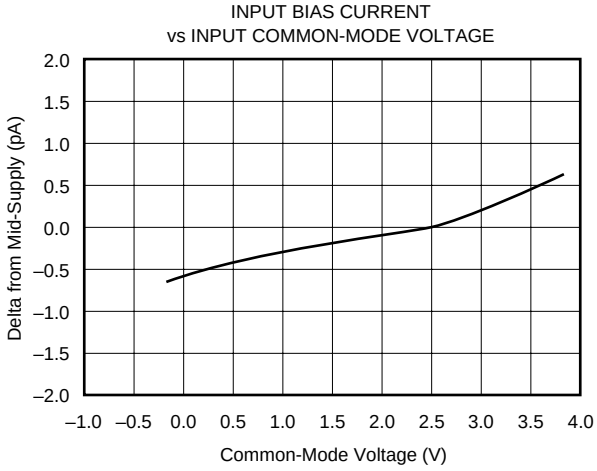
TYPICAL CHARACTERISTICS: Operational Amplifiers

At T_A = +25°C, $+AV_{DD}$, BV_{DD} = +5.0V, V_{REF} = Internal +2.5V, unless otherwise noted.





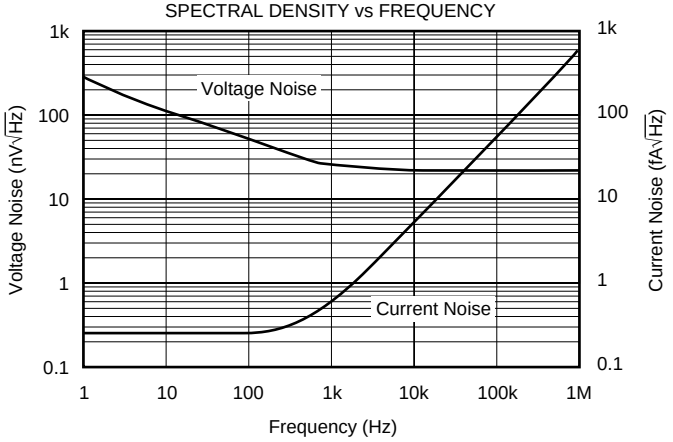




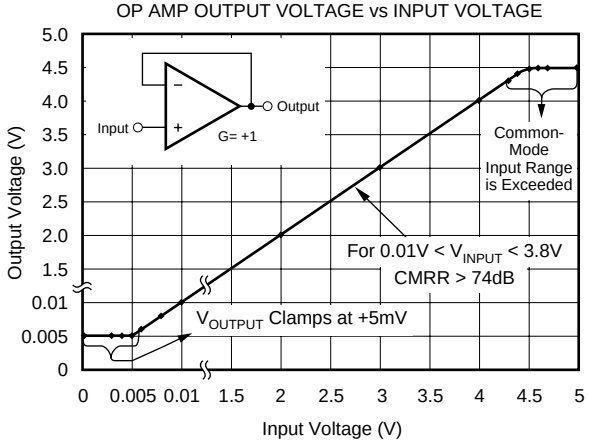
TYPICAL CHARACTERISTICS: Operational Amplifiers (Cont.)

At T_A = +25°C, $+AV_{DD}$, BV_{DD} = +5.0V, V_{REF} = Internal +2.5V, unless otherwise noted.

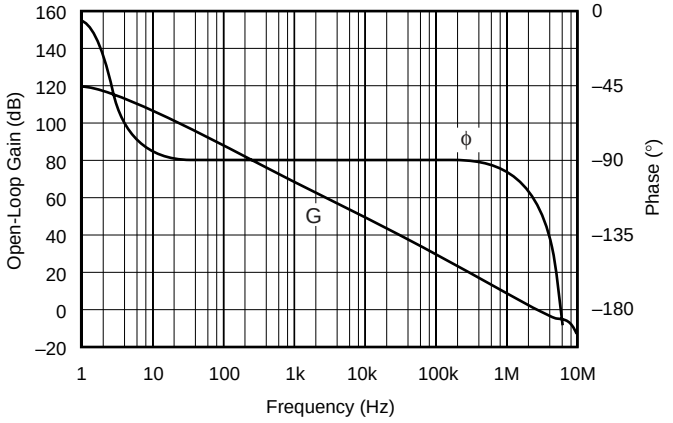
INPUT VOLTAGE AND CURRENT NOISE SPECTRAL DENSITY vs FREQUENCY



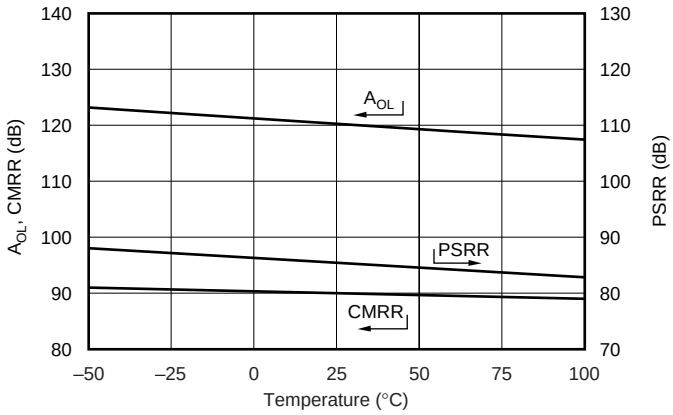
OP AMP OUTPUT VOLTAGE vs INPUT VOLTAGE



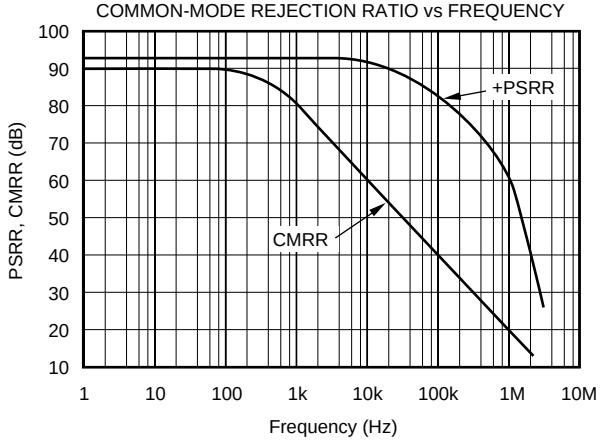
OPEN-LOOP GAIN/PHASE vs FREQUENCY



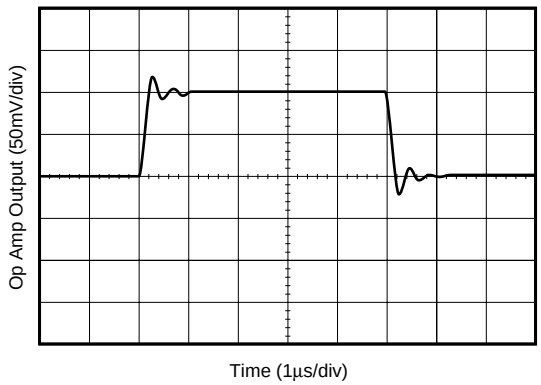
A_{OL}, CMRR, PSRR vs TEMPERATURE



POWER-SUPPLY REJECTION RATIO AND COMMON-MODE REJECTION RATIO vs FREQUENCY



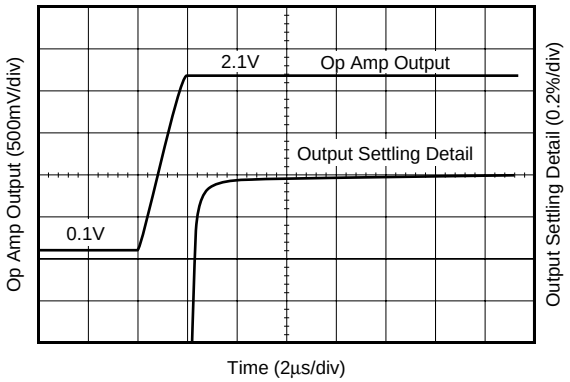
SMALL-SIGNAL STEP RESPONSE
G = 1, C_L = 100pF



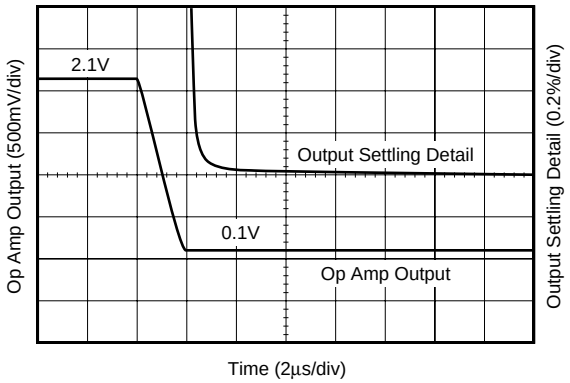
TYPICAL CHARACTERISTICS: Operational Amplifiers (Cont.)

At T_A = +25°C, $+AV_{DD}$, BV_{DD} = +5.0V, V_{REF} = Internal +2.5V, unless otherwise noted.

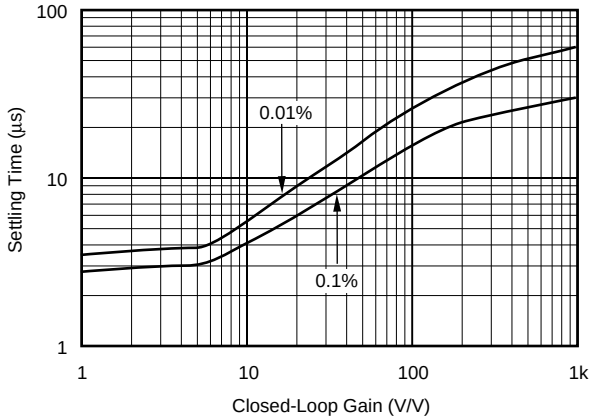
LARGE-SIGNAL STEP RESPONSE AND SETTLING TIME
C_L = 100pF, Gain = +1



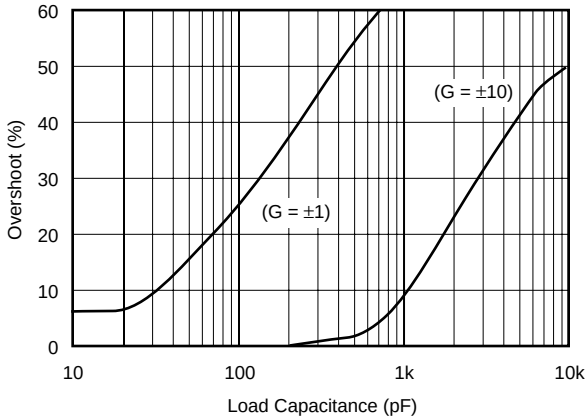
LARGE-SIGNAL STEP RESPONSE AND SETTLING TIME
C_L = 100pF, Gain = +1



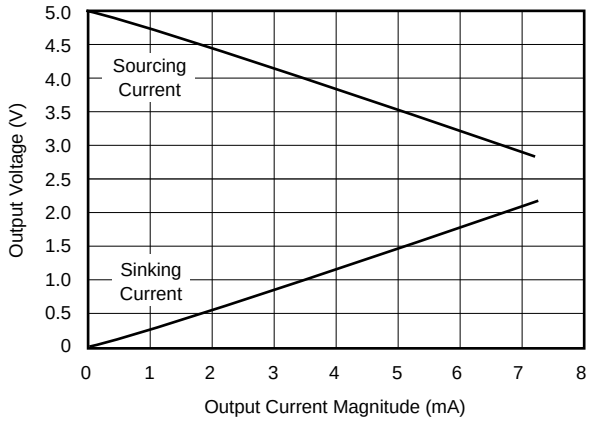
SETTLING TIME vs CLOSED-LOOP GAIN



SMALL-SIGNAL OVERSHOOT vs LOAD CAPACITANCE



OUTPUT VOLTAGE SWING FROM SUPPLY RAILS
vs OUTPUT CURRENT



OVERVIEW

The AMC7820 is an analog monitoring and control circuit for control of laser diodes and TEC coolers in DWDM applications. A register-based architecture eases integration with DSP-based (or microprocessor-based) systems through a standard SPI bus. All peripheral functions are controlled through the registers and onboard state machines.

The AMC7820 consists of the following blocks (refer to the block diagram of Figure 2):

- 8-Channel, 12-Bit ADC
- Three 12-Bit DACs
- Nine Operational Amplifiers
- +2.5V Reference
- TEC Soft Start Controller

Communication to the AMC7820 is via a standard SPI serial interface. This interface requires that $\overline{SS}$, the Slave Select signal, be driven LOW to communicate with the AMC7820. The data is then shifted into and out of the AMC7820 under control of the host DSP or microprocessor, which also provides the serial data clock.

Control of the AMC7820 and its functions is accomplished by writing to different registers in the AMC7820. A simple command protocol is used to address the 16-bit registers. Registers control the operation of the ADC, DACs, and device configuration. The results of measurements made are placed in the memory map and can be read by the host at any time.

All pins have ESD protection circuitry as the first active element on the chip. All input and output pins have protection diodes connected to supply and ground that remain reverse biased under normal operation. If the input voltages exceed the absolute maximum voltage range, it is necessary to add resistance in series with the input to limit the current to 10mA or less.

ADC

The analog inputs are provided via a multiplexer to the Successive Approximation Register (SAR) ADC. The ADC architecture is based on capacitive redistribution architecture that inherently includes a sample-and-hold function.

The multiplexer provides eight analog input channels to the ADC. Channels 0, 1, 6, and 7 are buffered by amplifiers OPA3, OPA4, OPA5, and OPA6, respectively. Channels 2, 3, 4, and 5 connect directly to external pins. The multiplexer connects each analog input to the ADC sequentially. Analog current into the device must charge the internal sample-and-hold capacitor during the sampling period. When the converter is in Hold mode, and the sampling capacitor has been fully charged, the input impedance of the analog input is greater than 1GΩ.

The on resistance of each multiplexer switch is typically 150Ω. In order to charge the internal sample-and-hold capacitor completely during the acquisition time, the source impedance of the analog input should be no more than 1kΩ.

The ADC runs continuously upon start-up, scanning through each channel. The results of conversions made are stored in the appropriate ADC registers.

Since the input range of the ADC is $2 \cdot V_{REF}$, codes near FFF will be missing if the output range of the signal source driving an ADC input channel is limited to less than $2 \cdot V_{REF}$. This is the case for channels 0, 1, 6, and 7 which are driven from internal op amps which have an output range limit of AV_{DD}. If all codes including FFF are required, the value of the reference voltage must be reduced or the value of AV_{DD} must be increased.

Data Format

The AMC7820 output data is in Straight Binary format, as shown in Figure 1. This figure shows the ideal output code for the given input voltage and does not include the effects of offset, gain, or noise.

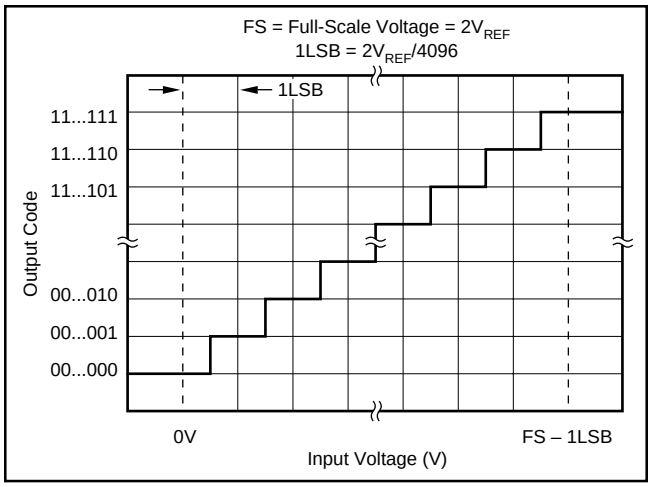


FIGURE 1. Ideal Input Voltage and Output Codes.

DACS

The three 12-bit DACs of the AMC7820 use a resistor-string architecture with switchable taps that are buffered by an operational amplifier (see DAC0 in Figure 4). Each op amp buffer can be configured for a gain of +1 or +2, which sets the output range to 0V to +2.5V or 0V to +5.0V, respectively. This architecture is inherently monotonic, a critical requirement for any system requiring “smooth” setpoint control.

The op amp buffer has a rail-to-rail output stage that has limitations on sinking or sourcing current when the output voltage is near AGND or AV_{DD}, respectively (see the typical characteristics). For example, if a DAC (Gain = +1) is set to code 010_H (+10mV) and is required to sink 1mA of current, the DAC output voltage will be approximately 250mV instead of the desired value of +10mV.

This problem is solved by restricting the DAC output voltage to values greater than +250mV or by reducing the required sink current. This restriction does not apply for the case of sourcing current for gain set at +1. When the gain is set at +2, there is a limitation on sourcing current with the output voltage near the positive supply rail.

The slope of the DAC output voltage curve for sinking or sourcing current is due to an increase in the inherent closed-loop output impedance of the operational amplifier buffer, when operating near a supply rail. Refer to the typical characteristic curves.

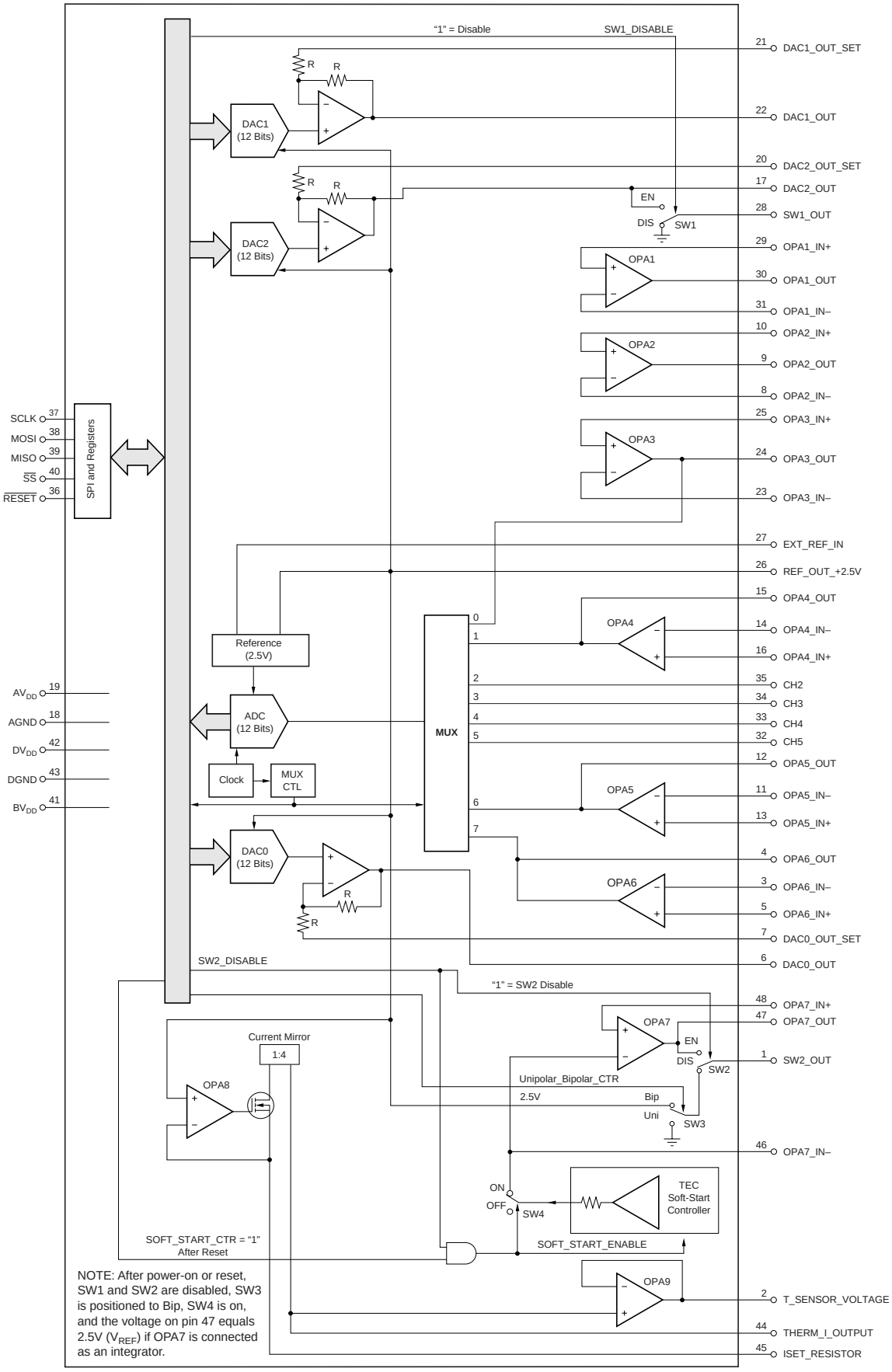


FIGURE 2. AMC7820 Block Diagram.

There are three other limitations when operating a DAC output near the supply rails, even if the load current is very small. 1) The output stage of the DAC buffer amplifier clamps at about +5mV above AGND. See the typical characteristics curves in the Operational Amplifier section for an illustration of this behavior. 2) If a DAC buffer amplifier has a negative input offset voltage, the output cannot increase until the input digital code is sufficient to overcome this negative offset. 3) When DAC gain is set at +2, swing near the AV_{DD} (+5.0V) rail will be clamped if the value of V_{REF} is greater than +2.50V and/or if the matching of the output buffer gain setting resistors gives a GAIN that is greater than +2.0.

OPERATIONAL AMPLIFIER

The AMC7820 has nine operational amplifiers. OPA8 is used to set the current source output. OPA9 buffers the temperature sensor voltage. All others can be configured for signal conditioning or control function.

The outputs of OPA3, OPA4, OPA5, and OPA6 connect to the ADC analog input channels 0, 1, 6, and 7, respectively.

The output of OPA7 connects to SW2_OUT when SW2 is enabled. Therefore, SW2 enables or disables OPA7 if SW2_OUT is used as the output of OPA7.

All amplifiers use a PMOS differential input stage that allows the common-mode input to extend from 200mV below ground up to AV_{DD} – 1.2V while maintaining very good CMRR, low offset voltage, low noise, and good PSRR. High open-loop gain provides excellent signal linearity and low closed-loop output impedance.

The rail-to-rail output stage can swing to within a few millivolts of the supply rails provided the sink and source currents are small (see the typical characteristics). Refer to the DAC section for more information regarding swinging close to the supply rails.

The input bias currents are very low, typically ranging from less than 1pA to a few pA. This current is almost entirely due to the leakage current of ESD diodes which are connected from each op amp input to AGND and AV_{DD}. For each 10°C rise in temperature, the leakage current will double, following classic diode leakage current versus temperature. Input offset current is the difference between the +IN and –IN bias current. In other words, the offset current is a measurement of the matching of the two input bias currents. Refer to the typical characteristics for more detail.

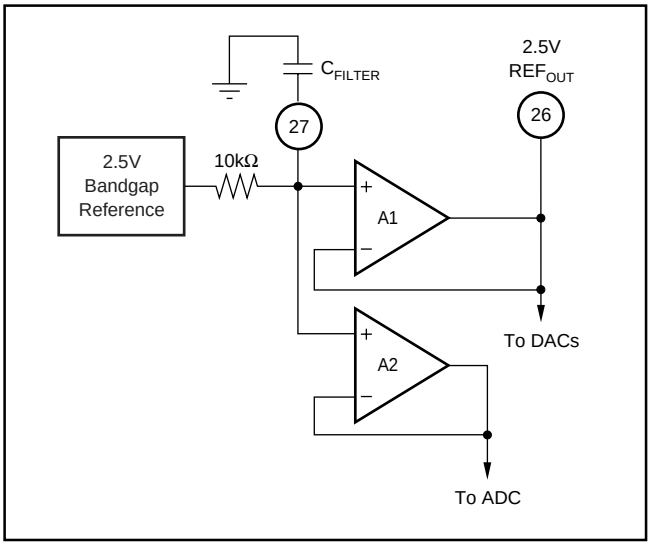


FIGURE 3. Reference Circuitry.

REFERENCE

The AMC7820 has an internal +2.5V bandgap voltage reference, as shown in Figure 3. Buffered by A1, the reference voltage is available on pin 26. The reference circuit can be overdriven by an external reference on pin 27. This pin also provides a point for filtering the internal reference, if desired a capacitor may be placed from pin 27 to analog ground to decrease reference noise. The time constant of this filter is (10K) • (C_{FILTER}).

The internal reference voltage can be adjusted by providing a small current into or out of pin 27. This current can be generated by a large resistor (e.g. 300kΩ) connected from pin 27 to an adjustable voltage source, such as the wiper of a potentiometer or the output of a DAC.

THERMISTOR CURRENT SOURCE AND TEMPERATURE SENSOR VOLTAGE

The thermistor current source output is set by the resistor connected from the ISET_RESISTOR, pin 45, to ground. The +2.5V reference voltage is forced on pin 45 by the closed-loop action of OPA8. The actual thermistor current is provided by a 1:4 current mirror that provides a current drive of 4 times the current flowing through the R_{ISET} resistor (see Figure 7). Thus, the thermistor current from pin THERM_I_OUTPUT (pin 44), I_{THERM}, is given by:

$$I_{THERM} = \frac{2.5V}{R_{ISET}} \bullet 4$$

The thermistor is driven by the current coming out of THERM_I_OUTPUT. The voltage developed across the thermistor is then buffered by the unity-gain buffer amplifier (OPA9). The voltage on pin T_SENSOR_VOLTAGE represents the actual TEC temperature.

For best performance, R_{ISET} should have a TCR of 10ppm/°C or less, and a tolerance of 0.1%. Using a current source preserves the full sensitivity of the thermistor (typically 50mV/°C). If a resistor were used to power the thermistor, the sensitivity would be reduced to approximately 25mV/°C, due to the voltage divider created by such an arrangement.

Because the thermistor current source has high output impedance and wide voltage compliance, it is possible for two separate laser modules to be controlled by connecting their thermistors in series with the output of this current source.

Since the THERM_I_OUTPUT and DAC0 reference are derived from the same reference, they track independently of any reference voltage drift, as shown in Figure 4. This can be viewed as a bridge arrangement common in instrumentation. When the temperature measured by the thermistor is equal to the temperature represented by the DAC's output voltage, the voltages at pin 2 and pin 6 are equal regardless of the reference drift caused by the change of the ambient temperature or other conditions. Figure 5 shows the typical performance of pin 2 minus pin 6 voltage tracking over –40°C to +85°C. The error is +0.75mV at –40°C and –0.4mV at +85°C, which, out of a 50mV/°C sensitivity for the thermistor, is equivalent to 0.015°C and 0.008°C, respectively.

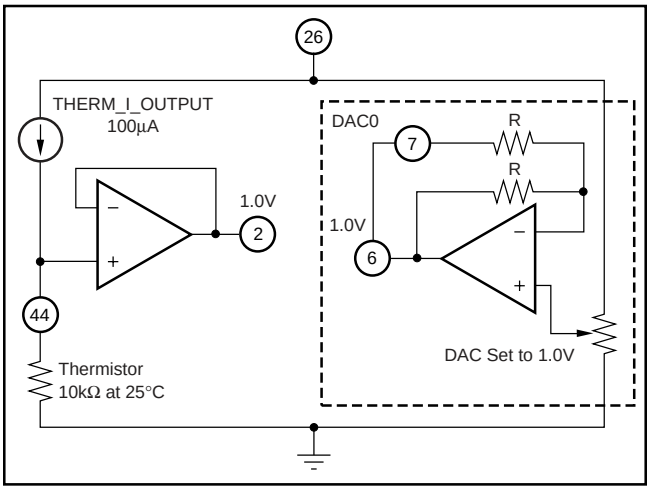


FIGURE 4. The Thermistor Feedback and Setpoint Viewed as a Bridge.

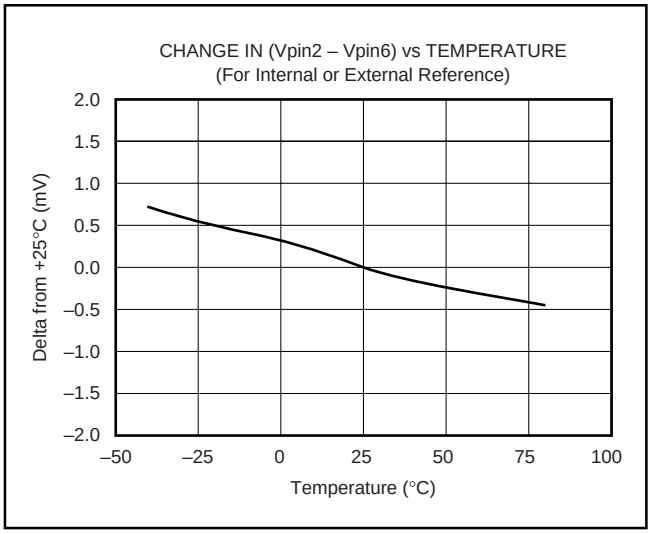


FIGURE 5. Change in (Vpin2 – Vpin6) vs Temperature.

SWITCHES

The AMC7820 has four internal switches (SW1, SW2, SW3, and SW4) to shut down the TEC and laser diode (see the application in Figure 7 for more detail).

SW1 and SW2 are controlled by the internal signals SW1_DISABLE and SW2_DISABLE, respectively. The status of these signals is determined by the four LSBs of the SHUTDOWN register (bits 0 through 3) designated SW1-1/SW1-0 and SW2-1/SW2-0. After power-on or reset, SW1 connects to ground, and SW2 connects to SW3.

SW3 is controlled by bits 2 and 3 (POL1/POL0) of the CONFIGURATION/STATUS register. After power-on or reset, SW3 connects to 2.5V (the internal reference voltage on pin 26).

Closing switch SW4 activates the TEC soft-start function implemented by the TEC SOFT_START CONTROLLER. SW4 is controlled by the internal signals SW2_DISABLE and SOFT_START_CTR. The LSBs (TS1/TS0) of the CONFIGURATION/STATUS register determines the status of SOFT_START_CTR. After power-on or reset, SW4 is closed and soft-start is activated. The host can write "00" to TS1/TS0 to turn off SW4.

The host can change the status of any switch by writing a proper pattern into the appropriate registers (refer to the AMC7820 Registers section).

TEC SOFT_START_CONTROLLER

This controller provides a soft start for a bidirectional TEC Driver when OPA7 is configured as an integrator (see Figure 6) and the TEC driver is referenced to 2.5V (see the Application section). Pin 1 (SW2_OUT) drives the external TEC driver. A value of 2.5V from this pin sets the TEC driver output current to zero, implementing a safe (zero current) starting condition.

After power-on or reset, switch SW2 is disabled interrupting control of the external TEC driver by the integrator OPA7. The actions of switches SW2 and SW3 apply 2.5V to pin 1, setting the external TEC driver output current to zero. Switch SW4 is also closed and the TEC SOFT_START_CONTROLLER is enabled. This controller drives the output of OPA7 to 2.5V which corresponds to zero TEC current. When the loop control of the external TEC driver is resumed, the TEC current is safely ramped up from zero. If the soft start controller is disabled and the control loop is also diabled with SW2, OPA7 will continue to integrate until its output reaches a supply rail. This will result in max current drive to the TEC, when the loop is enabled (a hard start).

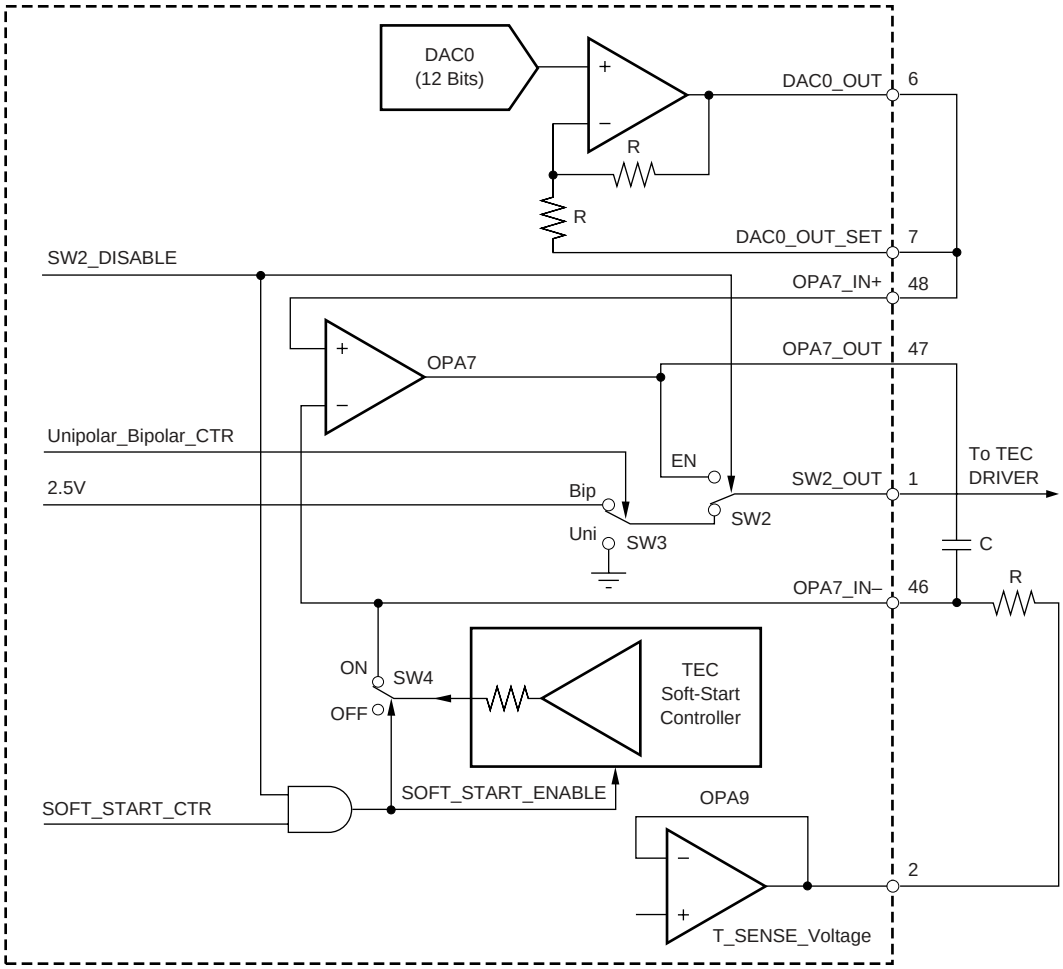


FIGURE 6. Soft Start Function.

APPLICATION

The AMC7820 can be used to control one CW type laser diode (or pump laser diode) current and one TEC cooler, two TEC coolers, or two laser diodes. See Figure 7 for a typical application to control one pump laser diode and one TEC. A similar approach can be used to control other CW type laser diodes.

TEC CONTROL

The TEC control loop is made up of the thermistor current source, a unity-gain buffer, a thermostat DAC (DAC0), the TEC integrator (OPA7), the internal TEC SOFT_START_ CONTROLLER, an external thermistor, and an external TEC Power Current Driver.

The external thermistor is driven by the current from the thermistor current source. The voltage across the thermistor represents the actual TEC temperature, and is fed into the

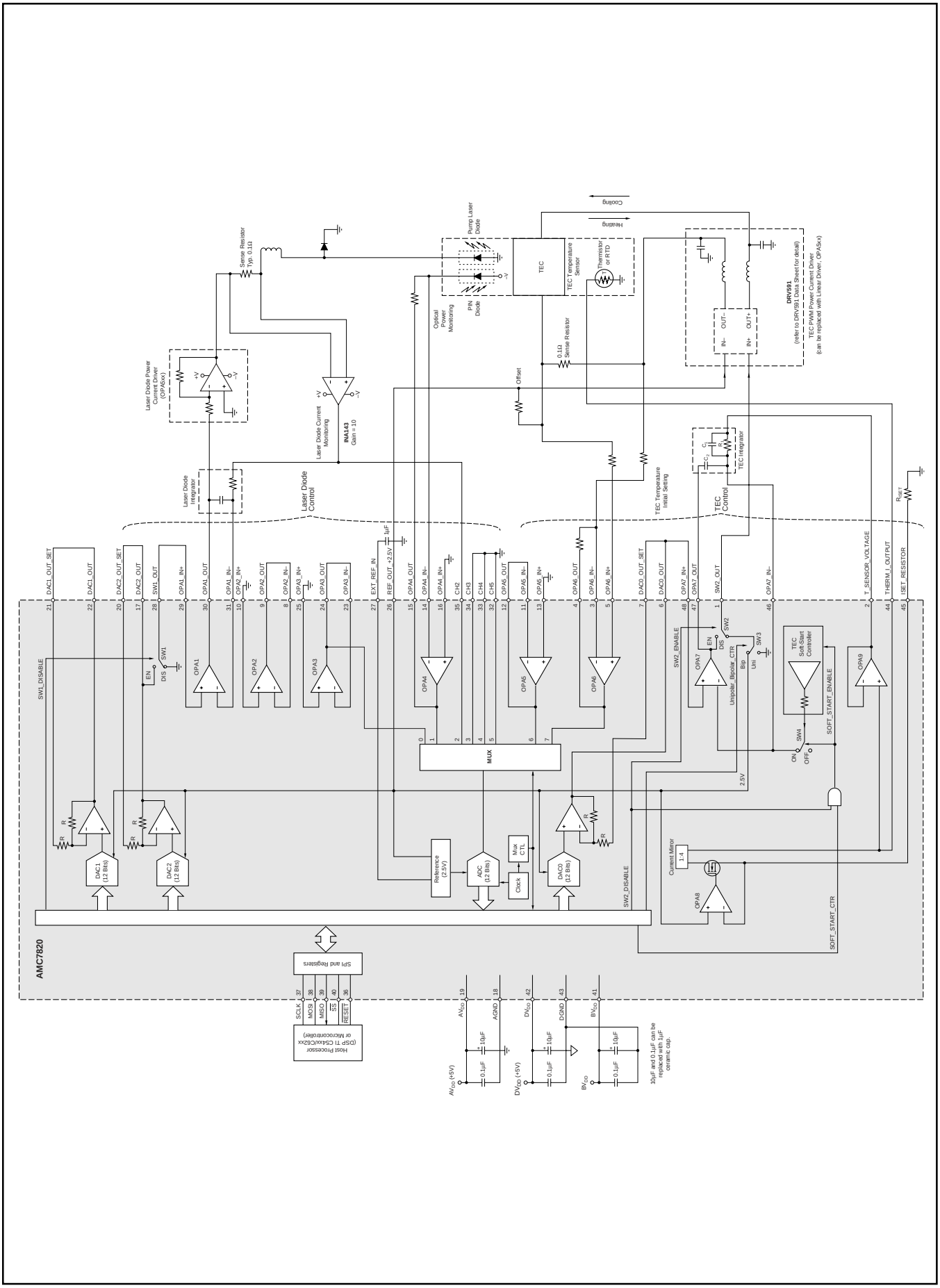


FIGURE 7. Typical AMC7820 Application: TEC and Laser Diode Current Control.

inverting input of TEC integrator, OPA7. The noninverting input of OPA7 connects to the thermostat DAC(DAC0), which sets the desired temperature of the pump laser diode module. The temperature that a certain voltage represents depends upon the value of the thermistor used and the drive current provided to that thermistor.

Pin 1 (SW2_OUT) controls the external TEC Power Current Driver (DRV591, a PWM power driver) which can be replaced with a linear driver (OPA5xx) if configured properly. In the application of Figure 7, 2.5V on pin 1 sets the TEC current to zero.

In normal operation, SW2 is enabled and OPA7 connects to the DRV591. The voltage across the thermistor controls the TEC current. When SW2 is disabled, the DRV591 is connected to SW3, which connects to 2.5V in the bipolar mode (which is the default mode). This results in zero TEC current, and shuts down the TEC. Meanwhile, TEC SOFT_START CONTROLLER drives the output of OPA7 to become equal to the reference voltage of 2.5V. This action provides a soft start when SW2 is enabled.

The TEC current is sensed across an external sense resistor (0.1Ω) by the amplifier OPA6, and is fed to analog channel 7 of the ADC. OPA6 is connected as a difference amplifier and is offset (by 2.5V) to provide the measurement of the bidirectional TEC current. The host processor monitors the current and takes proper action when necessary.

TEC CONTROL LOOP COMPENSATION

The AMC7820 has a dedicated amplifier (OPA7) to control the temperature of a Laser Diode Module. The amplifier can be configured in several ways to implement the control loop function, but it is commonly configured as a PID (Proportional-Integral-Derivative) controller. In this mode, the control loop consists of a low-frequency pole, a zero that cancels this pole below the dominant pole frequency of the TEC and, at higher frequencies, linear gain that promotes fast settling of the TEC.

Usually, the component values of the control loop are selected based upon the characteristics of the TEC (thermal gain and time constant), the gain of the TEC power driver, and the desired loop response. Frequently, the characteristics of the TEC are not known, which can lead to difficulty in designing the compensator analytically. An empirical design procedure using the actual loop components (TEC, power driver, and AMC7820) can be used to determine the compensator component values.

With this method, the loop response is monitored while making step changes to the control loop. A step change can be provided by writing data values to DAC0. An oscilloscope is used to monitor the temperature of the thermistor at the T_Sensor _Voltage pin.

The suggested manual tuning procedure is based upon the components shown in Figure 8.

1) Establish the setpoint of the control loop at the lowest anticipated temperature setting of the laser module. At this operating point, the gain of the temperature control loop is at it's highest. The loop is best compensated at this point.

2) Initially select R_1 = 2M, C_1 = 1uF, C_2 = 2uF. To improve the response, decrease the value of C_2. This increases the gain of the compensator near the dominant pole frequency of the TEC, resulting in faster settling times of the loop. However, at some value of C_2 the loop will start to oscillate. At this point, fix C_2 at 3x to 4x this value.

3) Verify the settling behavior of the control loop at the highest anticipated laser module setpoint temperature. The loop response may be somewhat different at this operating point. A compromise value of C_2 may be needed to balance the loop response at these operating point extremes.

Typical values of the loop compensation components are: R_1 = 2M, C_1 = 1uF, C_2 = 0.1uF. See Figures 9 through 12 for typical loop responses.

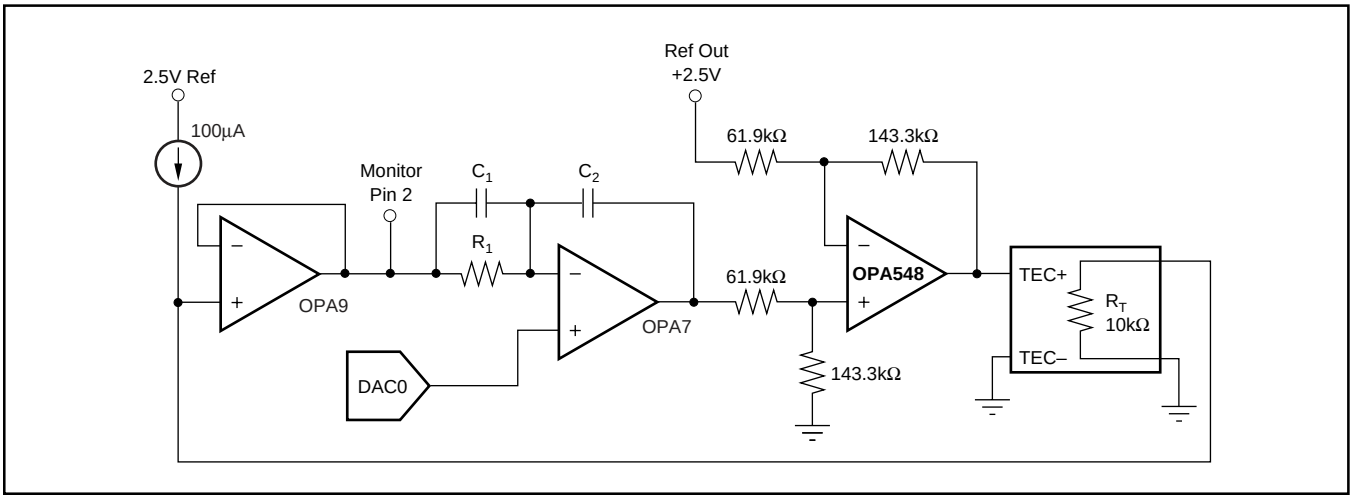


FIGURE 8. Compensation Loop.

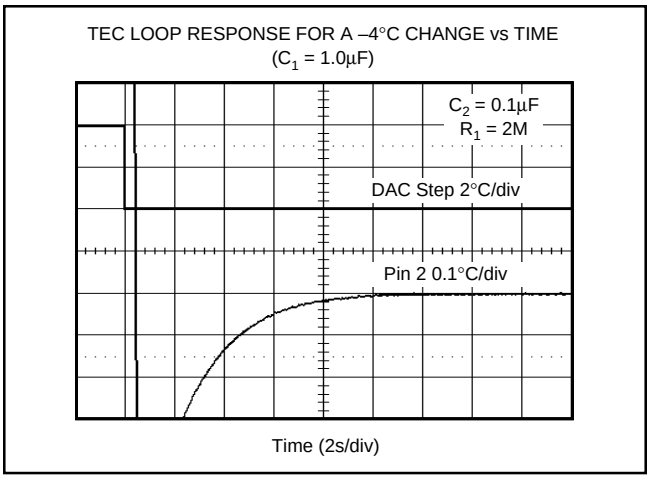


FIGURE 9. TEC Loop Response for a –4°C Change vs Time (C_1 = 1.0µF).

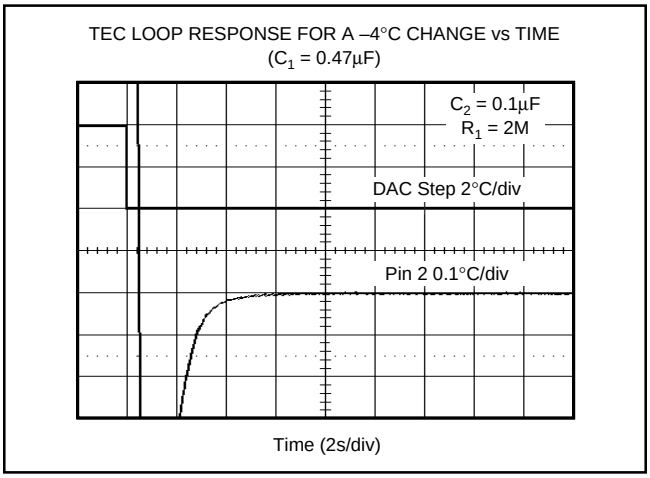


FIGURE 10. TEC Loop Response for a –4°C Change vs Time (C_1 = 0.47µF).

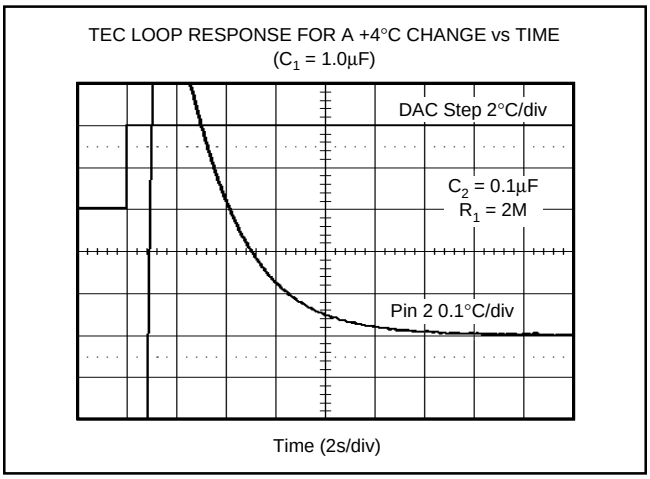


FIGURE 11. TEC Loop Response for a +4°C Change vs Time (C_1 = 1.0µF).

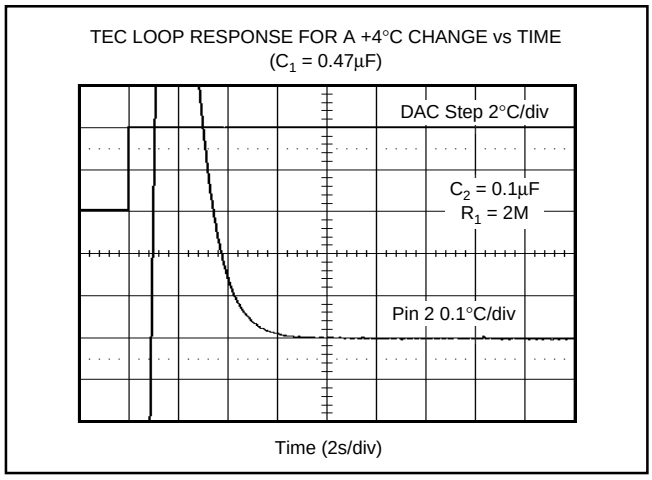


FIGURE 12. TEC Loop Response for a +4°C Change vs Time (C_1 = 0.47µF).

LASER DIODE CONTROL

The laser diode control loop, see Figure 7, maintains a constant diode current. The loop consists of an integrator (OPA1), a DAC (DAC2) to set the desired laser diode current, a transimpedance amplifier (OPA4) to monitor the optical power, an external current sense resistor, an external instrumentation amplifier (or difference amplifier) to sense the laser diode current, and an external laser diode current driver.

The current through the laser diode is sensed by the external sense resistor. The voltage across this resistor is fed to the instrumentation amplifier (gain of 10) which can have its inputs driven below ground. The output from this amplifier represents the laser diode current, and is fed back into the inverting input of the integrator (OPA1), closing the loop. The output of OPA1 drives the external power current driver. In normal operation, SW1 is enabled connecting the output of DAC2 (which represents the set point of the desired laser diode current) to the noninverting input of OPA1. After power-on or reset, SW1 is disabled and the noninverting input of OPA1 connects to ground. This forces laser current to zero, thereby shutting it down.

For applications where the laser diode cathode is grounded, all biasing voltages will be positive relative to ground. In this case, the external INA143 instrumentation amplifier can be eliminated, and an internal op amp can be substituted and configured as a 4-resistor difference amplifier.

The output optical power of the laser diode is monitored by the ADC (analog channel 1) through the back facet PIN diode and the transimpedance amplifier OPA4. The host processor monitors this power and takes proper action when necessary. Pin 15 is the output of OPA4 and represents the output optical power of the laser diode. The AMC7820 can put the laser diode in “constant power mode” as well. When the inverting input of the integrator OPA1 is connected to pin 15, instead of the output of INA143 that was shown in Figure 7, the laser control loop forces the output optical power of the laser diode to a constant level determined by the output of DAC2.

DIGITAL INTERFACE

The AMC7820 communicates through a standard SPI bus, which consists of four wires: SCLK (the serial clock pin), MISO (Master-Out Slave-In data pin), MOSI (Master-In Slave-Out data pin), and $\overline{SS}$ (Slave Select pin). The SPI master device activates the slave select signal ($\overline{SS}$ = LOW) to access the selected SPI slave device and generates SCLK to synchronize the movement of the data both in and out of the slave devices through the MOSI and MISO pins. The SPI slave devices depend on a master to start and synchronize transmissions.

A transmission begins when initiated by an SPI master. The word from the master is shifted into the AMC7820 through the MOSI pin under the control of the master serial clock, SCLK. The word from the AMC7820 registers (the slave) is shifted out from the MISO pin under control of SCLK as well.

The idle state of the serial clock for the AMC7820 is LOW, which corresponds to a clock polarity setting of 0 (typical microprocessor SPI control bit CPOL = 0). The AMC7820 interface is designed with a clock phase setting of 1 (typical microprocessor SPI control bit CPHA = 1). In both the master and slave, the data is shifted out on the rising edge of SCLK and sampled on the falling edge of SCLK, where the data is stable. The master begins driving its MOSI pin on the first rising edge of SCLK after $\overline{SS}$ is activated ($\overline{SS}$ = LOW).

To write data into the AMC7820, the host activates the slave select signal ($\overline{SS}$ = LOW) and issues a WRITE command to start the data transmission. The AMC7820 always interprets the first word (from the host) immediately following the falling edge of the $\overline{SS}$ signal as a command. The data to be written into the AMC7820 follows the command. $\overline{SS}$ must remain LOW until all data is transmitted (see Figure 13), otherwise the WRITE operation is terminated. Likewise, to read the data from the AMC7820, the host activates the slave select signal and sends a READ command. Then the AMC7820 sends data out through the MISO pin under control of SCLK. $\overline{SS}$ must remain LOW until all data is shifted out (see Figure 13), otherwise the transmission is terminated.

When the operation is terminated, the master must issue a new command to start a new operation. In the AMC7820, all data is 16-bit. It takes 16 clock cycles of SCLK to transfer one word of data.

AMC7820 COMMUNICATION PROTOCOL

The AMC7820 is entirely controlled by registers. Reading and writing these registers is accomplished by a 16-bit command that is sent prior to the data for that register. The command is constructed, as shown in Table I.

The command word begins with a R/$\overline{W}$ bit that specifies the direction of data flow. The following 4 bits specify the page of memory this command is directed to, as shown in Table II. The next five bits specify the register address on that page of memory to which the data is directed. The last six bits are reserved for future use.

PG3	PG2	PG1	PG0	PAGE ADDRESSED
0	0	0	0	0
0	0	0	1	1
0	0	1	0	Reserved
0	0	1	1	Reserved
0	1	0	0	Reserved
0	1	0	1	Reserved
0	1	1	0	Reserved
0	1	1	1	Reserved
1	0	0	0	Reserved
1	0	0	1	Reserved
1	0	1	0	Reserved
1	0	1	1	Reserved
1	1	0	0	Reserved
1	1	0	1	Reserved
1	1	1	0	Reserved
1	1	1	1	Reserved

TABLE II. Page Addressing.

To read all the first page of memory, for example, the host processor must send the command 0x8000—this specifies a read operation beginning at Page 0, Address 0. The processor can then start clocking data out of the AMC7820. The AMC7820 will automatically increment its address pointer to the end of the page; if the host processor continues clocking data out past the end of a page, the address will wrap around to the beginning of the page. This is true of either reading or writing, so it is important that the host makes sure of the address to which it is writing. Likewise, writing to Page 1 of memory would consist of the processor writing the command 0x0800 (which would specify a write operation) with PG0 set to 1, and all the ADDR bits set to 0. This would result in the address pointer pointing at the first location in memory on Page 1 of memory. See the AMC7820 Memory Map section for details of register locations. To make correct R/$\overline{W}$ operations, the host must issue $\overline{SS}$ and SCLK properly.

Bit 15 MSB	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 LSB
R/$\overline{W}$	PG3	PG2	PG1	PG0	ADDR4	ADDR3	ADDR2	ADDR1	ADDR0	X	X	X	X	X	X
NOTE: R/$\overline{W}$ = 1 when reading; 0 when writing. X = Don't care.															

TABLE I. AMC7820 Command Word.

Figure 13 shows an example of a complete data transaction between the host processor and the AMC7820.

AMC7820 MEMORY MAP

The AMC7820 has several 16-bit registers that allow control of the device as well as providing a location for results from the AMC7820 to be stored until read by the host microprocessor. These registers are separated into two pages of memory in the AMC7820: a Data page (Page 0) and a Control page (Page 1). The memory map is shown in Tables III and IV. Locations that are marked reserved will read back 0x0000 if they are read by the host.

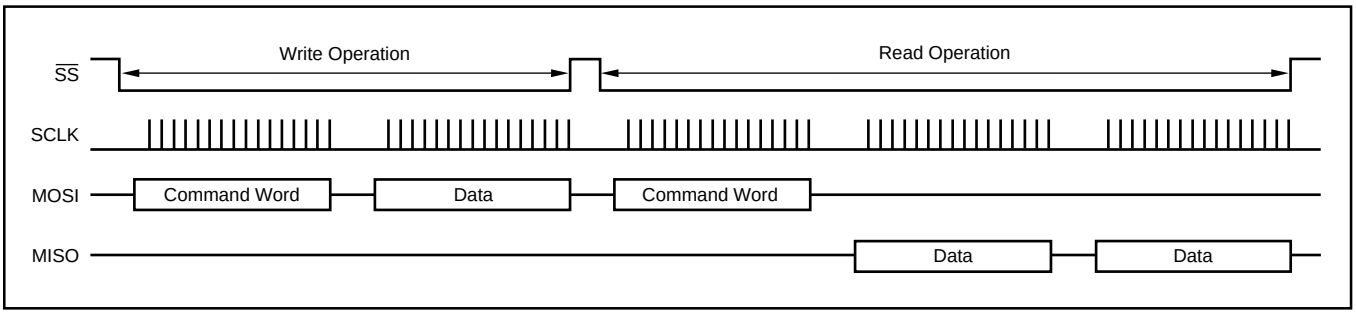


FIGURE 13. Write and Read Operation of the AMC7820 Interface.

PAGE 0: DATA REGISTERS

ADDRESS	REGISTER
00	CH0
01	CH1
02	CH2
03	CH3
04	CH4
05	CH5
06	CH6
07	CH7
08	Reserved
09	DAC0
0A	DAC1
0B	DAC2
0C	Reserved
0D	Reserved
0E	Reserved
0F	Reserved
10	Reserved
11	Reserved
12	Reserved
13	Reserved
14	Reserved
15	Reserved
16	Reserved
17	Reserved
18	Reserved
19	Reserved
1A	Reserved
1B	Reserved
1C	Reserved
1D	Reserved
1E	Reserved
1F	Reserved

TABLE III. AMC7820 Memory Map: Page 0.

PAGE 1: CONTROL REGISTERS

ADDRESS	REGISTER
00	Shut Down
01	Reset
02	Configuration/Status
03	Reserved
04	Reserved
05	Reserved
06	Reserved
07	Reserved
08	Reserved
09	Reserved
0A	Reserved
0B	Reserved
0C	Reserved
0D	Reserved
0E	Reserved
0F	Reserved
10	Reserved
11	Reserved
12	Reserved
13	Reserved
14	Reserved
15	Reserved
16	Reserved
17	Reserved
18	Reserved
19	Reserved
1A	Reserved
1B	Reserved
1C	Reserved
1D	Reserved
1E	Reserved
1F	Reserved

TABLE IV. AMC7820 Memory Map: Page 1.

AMC7820 REGISTERS

This section will describe each of the registers that were shown in the memory map of Tables III and IV. The registers are grouped according to the function they control.

AMC7820 ADC REGISTERS

The results of all ADC conversions are placed in the appropriate data register, as described in Table III. The data format of these read-only registers is as follows:

Bit 15 MSB	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 LSB
A2	A1	A0	DV	D11 MSB	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0 LSB

where,

A2 - A0—Channel Address Bits. These three bits will correspond to the address of the channel whose result is in the lower 12 bits.

DV—Data Valid. This bit is set (“1”) when a new conversion result is placed in the register. The DV bit is cleared (“0”) after the register is read. This allows software to determine if the result it has read from the register is the result of a new conversion or a previously read result. This bit is also cleared upon power-up or reset of the AMC7820.

D11 - D0—Data bits from the ADC conversion.

Upon power-up, the data registers are cleared to all zeros. This also occurs with a hardware or software RESET. Since the ADC operates at 100K samples/second (10µs per conversion), the host should allow at least 80µs before reading any ADC channels to allow the multiplexer time to scan through all eight channels and write valid data to the data registers.

AMC7820 DAC REGISTERS

The data to be written to the DAC is written into one of the three DAC data registers that are formatted as follows:

Bit 15 MSB	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 LSB
X	X	X	X	DB11 MSB	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0 LSB

where,

DB11 - DB0—Data bits to be written to the DAC. The analog output of the DAC is updated when the value is written into the register.

x = Don’t Care.

The DAC registers are cleared to all zeros (0x0000) upon power-up or reset. The DAC registers are read and write-enabled, so that the registers can be read back to confirm the data.

AMC7820 SHUTDOWN REGISTER

The enable and disable functions of SW1 and SW2 are accomplished by writing a proper word into the SHUTDOWN register. When enabled, SW1 connects to the output of DAC2, and SW2 connects to the output of OPA7. When disabled, SW1 connects to analog ground, and SW2 connects to the output of SW3. The format of the SHUTDOWN register is as follows:

Bit 15 MSB	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 LSB
X	X	X	X	X	X	X	X	X	X	X	X	SW1-1	SW1-0	SW2-1	SW2-0

where,

SW1-0 - SW1-1—SW1 Disable Control Bits. For the operation of these two bits, see Table V.

SW2-0 - SW2-1—SW2 Disable Control Bits. For the operation of these two bits, see Table V.

x = Don’t Care.

SW1/SW2 1	SW1/SW2 0	OPERATION
0	0	Invalid—a write of this value will not result in any change to the bit values stored in the register.
0	1	Enable (the normal operating mode). SW1 connects to DAC2, and SW2 connects to the output of OPA7.
1	0	Disable (condition after power-up or reset). SW1 connects to ground, and SW2 connects to SW3.
1	1	Invalid—a write of this value will not result in any change to the bit values stored in the register.

TABLE V. Shutdown Bit Patterns.

The default state of this register upon power-up or reset is such that both SW1 and SW2 are disabled (0x000A). The logic level of signal SW1_DISABLE is HIGH when switch SW1 is disabled, and LOW when SW1 is enabled. The logic level of signal SW2_DISABLE is HIGH when switch SW2 is disabled, and LOW when SW2 is enabled.

AMC7820 RESET REGISTER

The AMC7820 has a special register, the RESET register, which acts like the $\overline{\text{RESET}}$ pin of the device. Writing the code 0xXBB3, as shown below, to this register will cause the AMC7820 to perform a software reset. Note that only the lower 12 bits have significance for this reset function.

Bit 15 MSB	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 LSB
X	X	X	X	1	0	1	1	1	0	1	1	0	0	1	1

where,

x = Don't Care.

Writing any other values to this register will do nothing. Upon reset, this register is set to all zeros. Therefore, reading this register should always result in reading back 0x0000.

AMC7820 CONFIGURATION/STATUS REGISTER

AMC7820 can be configured to control bidirectional TEC and single direction TEC by properly setting SW3 and TEC_SOFT_START_CONTROLLER. This is accomplished by writing a proper word into this register.

A reset status bit indicates if a reset has occurred. The register is formatted as follows:

Bit 15 MSB	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 LSB
X	X	X	X	X	X	X	X	X	X	X	RSTC	POL1	POL0	TS1	TS0

where,

RSTC—Reset Complete. This bit is set to "1" on power-up or reset. This bit can be cleared by writing a "0" to this location, but it cannot be set to "1" by the host, only a reset being performed will set it to 1. This allows the host to determine if the part has been configured after power-up, and if a reset has occurred to the AMC7820 without the host's knowledge.

POL0 – POL1—Polarity bits that control SW3. The operation is shown in Table VI. After power-up or reset, these bits are set to bipolar mode, and SW3 is positioned to 2.5V.

TS1 – TS0—TEC Soft Start Enable Bits, which determine the status of the signal SOFT_START_CTR. The operation is shown in Table VII. After power-up or reset, TS1 = "0", TS0 = "1", SOFT_START_CTR = HIGH ("1").

POL1	POL0	OPERATION
0	0	Invalid—a write of this value will not result in any change to the bit values stored in the register.
0	1	Bipolar Mode. SW3 is positioned to 2.5V. (Condition after power-up or reset.)
1	0	Unipolar Mode. SW3 is positioned to AGND.
1	1	Invalid—a write of this value will not result in any change to the bit values stored in the register.

TABLE VI. Polarity Bit Operation.

TS1	TS0	OPERATION
0	0	SOFT_START_CTR is LOW ("0"). TEC SOFT_START_CONTROLLER is disabled regardless of the status of SW2.
0	1	SOFT_START_CTR is HIGH ("1"). TEC SOFT_START_CONTROLLER is enabled if SW2 is disabled (SW2_DISABLE = HIGH ("1")) (Condition after power-up or reset.)
1	0	SOFT_START_CTR is LOW ("0"). TEC SOFT_START_CONTROLLER is disabled regardless of the status of SW2.
1	1	Invalid—a write of this value will not result in any change to the status of SOFT_START_CTR.

TABLE VII. TEC Soft Start Enable Bit Operation.

LAYOUT

For optimum performance, care should be taken with the physical layout of the AMC7820 circuitry. The basic SAR architecture is sensitive to glitches or sudden changes on the power supply, reference, ground connections, and digital inputs that occur just prior to latching the output of the analog comparator of the ADC. Therefore, during any single conversion for an 'n-bit' SAR converter, there are n 'windows' in which large external transient voltages can easily affect the conversion result. Such glitches might originate from switching power supplies, nearby digital logic, and high-power devices. The degree of error in the digital output depends on the reference voltage, layout, and the exact timing of the external event.

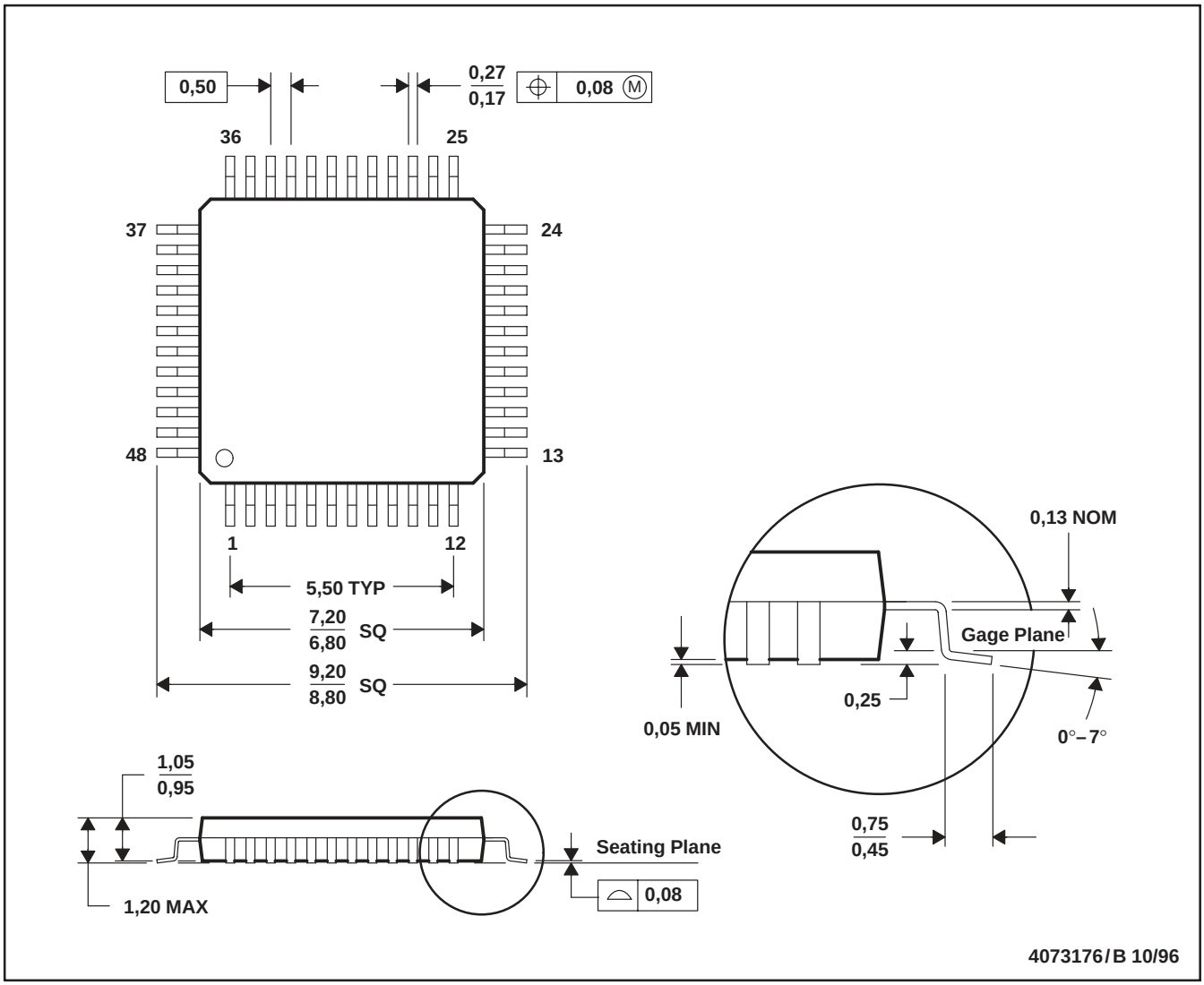
With this in mind, power to the AMC7820 should be clean and well bypassed. A 0.1μF ceramic bypass capacitor should be placed as close to the device as possible. A 1μF to 10μF capacitor may also be needed if the impedance of the connection between AV_{DD} and the power supply is high.

It is recommended to install a reference bypass capacitor (1μF) between the EXT_REF_IN pin and analog ground when internal reference is used. If an external reference voltage originates from an op amp, make sure that it can drive any bypass capacitor that is used without oscillation.

The AMC7820 architecture offers no inherent rejection of noise or voltage variation coming from an external reference input. Any noise and ripple from the reference will appear directly in the analog and digital results.

The AGND and DGND pins should be connected to a clean ground point. In many cases, this will be the "analog" ground. Avoid connections that are too near the grounding point of a microcontroller or digital signal processor. If needed, run a ground trace directly from the converter to the power-supply entry or battery-connection point. The ideal layout will include an analog ground plane dedicated to the AMC7820 and associated external analog circuitry.

PFB (S-PQFP-G48) **PLASTIC QUAD FLATPACK**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-026

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
AMC7820Y/250	ACTIVE	TQFP	PFB	48	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	AMC7820Y	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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