

STRUCTURE Silicon Monolithic Integrated Circuit

NAME OF PRODUCT DC-AC Inverter Control IC

TYPE **BD9270F**

FUNCTION

- 1ch control with Full-Bridge (For USE FET Body-Di)
- Lamp current and voltage sense feed back control
- Sequencing easily achieved with Soft Start Control
- Striking time can Control independently (STRK pin)
- Circuit protection with Timer Latch (COMP)
- Circuit protection with quick Shutdown (COMPSD)
- Mode-selectable the operating or stand-by mode by stand-by pin
- Synchronous operating the other BD9270F ICs
- BURST mode controlled by PWM input
- Output liner Control by external DC voltage
- Built-in Error mode output pin (FAIL pin)

○ Absolute Maximum Ratings (Ta = 25°C)

Parameter	Symbol	Limits	Unit
Supply Voltage	Vcc	20	V
OUTPUT DRIVER	LNx, HFNx,	20	V
Operating Temperature Range	Topr	-40~+85	°C
Storage Temperature Range	Tstg	-55~+150	°C
Maximum Junction Temperature	Tjmax	+150	°C
Power Dissipation	Pd	688	mW

*Pd derate at 5.5mW/°C for temperature above Ta = 25°C (When mounted on a PCB 70.0mm×70.0mm×1.6mm)

○ Operating condition

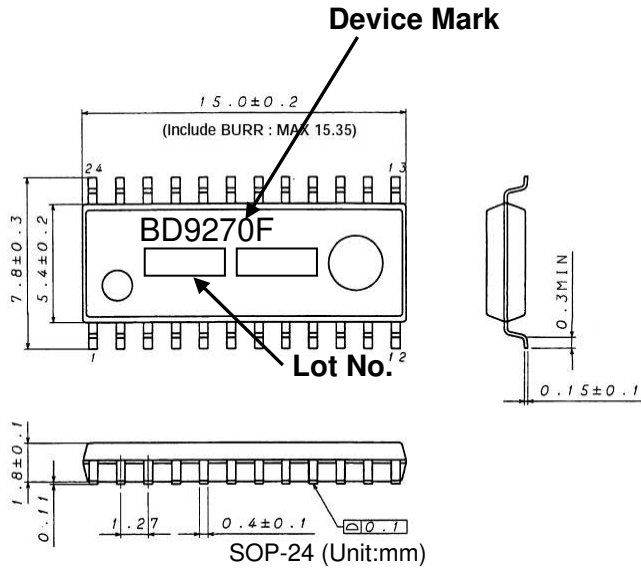
Parameter	Symbol	Limits	Unit
Supply voltage	Vcc	8.5~19.0	V
DRIVER frequency	FOUT	30~110	kHz

○ Electric Characteristics (Ta=25°C, VCC=12V, STB=3.0V)

Parameter	Symbol	Limits			Unit	Conditions
		MIN.	TYP.	MAX.		
((WHOEL DEVICE))						
Operating current	Icc1	—	4.5	8.1	mA	FOUT=60kHz, FB=GND, DUTY=0V
Stand-by current	Icc2	—	30	70	uA	
((STAND BY CONTROL))						
Stand-by voltage H	VstH	2	—	VCC	V	System ON
Stand-by voltage L	VstL	-0.3	—	0.8	V	System OFF
((REF4V BLOCK))						
REF4V output voltage	VREG	3.92	4.00	4.08	V	
REF4V source current	IREG	5	—	—	mA	
((VCC UVLO BLOCK))						
Operating voltage (VCC)	Vvccuvlo	7.0	7.5	8.0	V	
Hysteresis width (VCC)	Δ Vvccuvlo	0.50	0.60	0.70	V	
((OSC BLOCK))						
Drive output frequency	FOUT	63.0	65.0	67.0	kHz	RT=18.9k Ω
RT pin voltage	VRT	1.05	1.50	1.95	V	
SRT ON resistance	RSRT	—	100	200	Ω	
((SS STRK BLOCK))						
Soft start current	ISS	0.9	1.1	1.3	uA	
SS operation start voltage	VSS_ST	0.18	0.20	0.22	V	
SS term END voltage	VSS_ED	1.35	1.50	1.65	V	
STRK current	ISTRK	0.8	1.0	1.2	uA	
STRK term END voltage	VSTRK_ED	1.94	2.00	2.06	V	
((FEED BACK BLOCK))						
IS threshold voltage 1	VIS1	1.225	1.25	1.275	V	
IS threshold voltage 2	VIS2	—	VREFIN	VIS1	V	VREF applying voltage
VS threshold voltage	VVS	1.22	1.25	1.28	V	
IS source current 1	IIS1	—	—	0.9	uA	DUTY=1.5V
IS source current 2	IIS2	40	50	60	uA	DUTY=0V, IS=1.0V
VS source current	IVS	—	—	0.9	uA	
IS COMP detect voltage 1	VISCOMP1	0.593	0.625	0.657	V	VREFIN \geq 1.25V
IS COMP detect voltage 2	VISCOMP2	—	0.50	—	V	VREFIN= 1V
VREF input voltage range	VREFIN	0.6	—	1.6	V	No effect at VREF > 1.25V
((DUTY BLOCK))						
DUTY threshold voltage	DUTY-th	0.90	1.00	1.10	V	Low = IS high (burst off)
((OUTPUT BLOCK))						
LN output sink resistance	RsinkLN	1.8	3.5	7.0	Ω	VCC=12V
LN output source resistance	RsourceLN	4.5	9.0	18.0	Ω	VCC=12V
HFN output sink resistance	RsinkHFN	1.8	3.5	7.0	Ω	VCC=12V
HFN output source resistance	RsourceHFN	4.5	9.0	18.0	Ω	VCC=12V
MAX DUTY	MAX DUTY	44.0	45.5	47.0	%	FOUT=65kHz
((TIMER LATCH BLOCK))						
Timer Latch setting voltage	VCP	1.94	2.00	2.06	V	
Timer Latch setting current	ICP	0.9	1.0	1.1	uA	
((COMP BLOCK))						
COMP over voltage detect	VCOMPH	1.94	2.00	2.06	V	VSS > 1.65V, SRT operate, CP timer latch
Hysteresis width (COMP)	Δ VCOMPH	0.05	0.10	0.15	V	
COMPSD over voltage detect	VCOMPSDH	1.94	2.00	2.06	V	VSS > 1.65V, OSC 2 count
Hysteresis width (COMPSD)	Δ VCOMPSDH	0.05	0.10	0.15	V	
FAIL ON resistance	RFAIL	—	100	200	Ω	
((SYNCHRONOUS BLOCK))						
CT_SYNC_OUT High voltage	VCT_SYNC	3.8	4.0	4.2	V	
CT_SYNC_OUT Low voltage	VCT_SYNC_L	—	—	0.5	V	
CT_SYNC_OUT sink resistance	RSYNC_OUT_sink	—	150	300	Ω	
CT_SYNC_OUT source resistance	RSYNC_OUT_source	—	300	400	Ω	
CT_SYNC_IN High voltage input range	VCT_SYNC_IN_H	2.5	—	VCT_SYNC	V	
CT_SYNC_IN Low voltage input range	VCT_SYNC_IN_L	-0.3	—	1	V	

(This product is not designed to be radiation-resistant.)

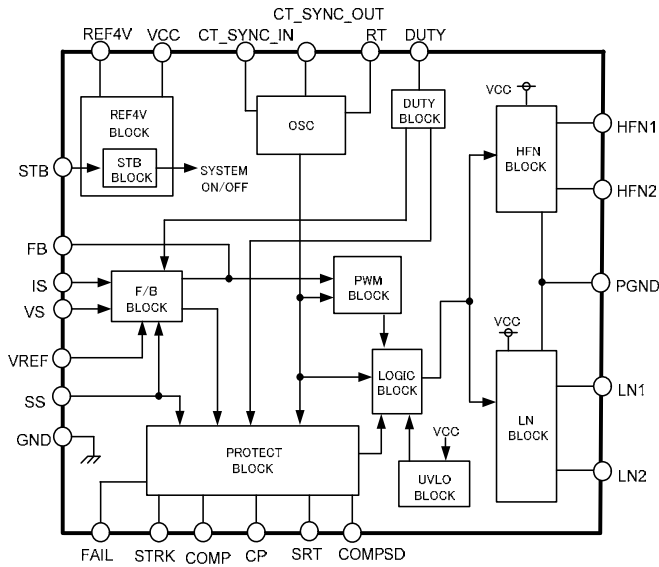
OPackage Dimensions



OPin Description

PIN No.	PIN NAME	FUNCTION
1	PGND	Ground for FET drivers
2	LN2	NMOS FET driver
3	HFN2	NMOS FET driver (New Function)
4	CT_SYNC_IN	CT synchronous signal input pin
5	CT_SYNC_OUT	CT synchronous signal output pin
6	REF4V	Internal regulator output
7	SRT	External resistor from SRT to RT for adjusting the start-up triangle oscillator
8	RT	External resistor from RT to GND for adjusting the triangle oscillator
9	GND	GROUND
10	DUTY	Control PWM mode and BURST mode
11	FAIL	Error mode OUTPUT Pin (open drain)
12	STB	Stand-by switch
13	CP	External capacitor from CP to GND for Timer Latch
14	VREF	Reference voltage input pin for Error amplifier
15	VS	Error amplifier input
16	IS	Error amplifier input
17	FB	Error amplifier output
18	SS	External capacitor from SS to GND for Soft Start Control
19	STRK	Striking time setting pin
20	COMPSD	Over voltage detect pin with Shutdown
21	COMP	Over voltage detect pin with timer latch
22	VCC	Supply voltage input
23	HFN1	NMOS FET driver (New Function)
24	LN1	NMOS FET driver

OBlock Diagram



○NOTE FOR USE

1. This product is produced with strict quality control, but might be destroyed if used beyond its absolute maximum ratings. Once IC is destroyed, failure mode will be difficult to determine, like short mode or open mode. Therefore, physical protection countermeasure, like fuse is recommended in case operating conditions go beyond the expected absolute maximum ratings.
2. The circuit functionality is guaranteed within of ambient temperature operation range as long as it is within recommended operating range. The standard electrical characteristic values cannot be guaranteed at other voltages in the operating ranges, however the variation will be small.
3. Mounting failures, such as misdirection or miscounts, may harm the device.
4. A strong electromagnetic field may cause the IC to malfunction.
5. The GND pin should be the location within $\pm 0.3V$ compared with the PGND pin. ALL Pin Voltage should be under VCC voltage +0.3V even if the voltage is under each terminal ratings.
6. BD9270F incorporate a built-in thermal shutdown circuit (TSD circuit). The thermal shutdown circuit (TSD circuit) is designed only to shut the IC off to prevent runaway thermal operation. It is not designed to protect the IC or guarantee its operation of the thermal shutdown circuit is assumed.
7. When modifying the external circuit components, make sure to leave an adequate margin for external components actual value and tolerance as well as dispersion of the IC.
8. About the external FET, the parasitic Capacitor may cause the gate voltage to change, when the drain voltage is switching. Make sure to leave adequate margin for this IC variation.
9. Under operating CP charge (under error mode) analog dimming and burst dimming are not operate.
10. Under operating Slow Start Control (SS is less than 1.5V), It does not operate Timer Latch.
11. By STB voltage, BD9270F are changed to 2 states. Therefore, do not input STB pin voltage between one state and the other state (0.8~2.0V).
12. The pin connected a connector need to connect to the resistor for electrical surge destruction.
13. This IC is a monolithic IC which (as shown is Fig-1) has P⁺ substrate and between the various pins. A P-N junction is formed from this P layer of each pin. For example, the relation between each potential is as follows,

○ (When GND > PinB and GND > PinA, the P-N junction operates as a parasitic diode.)

○ (When PinB > GND > PinA, the P-N junction operates as a parasitic transistor.)

Parasitic diodes can occur inevitably in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits as well as operation faults and physical damage. Accordingly you must not use methods by which parasitic diodes operate, such as applying a voltage that is lower than the GND (P substrate) voltage to an input pin.

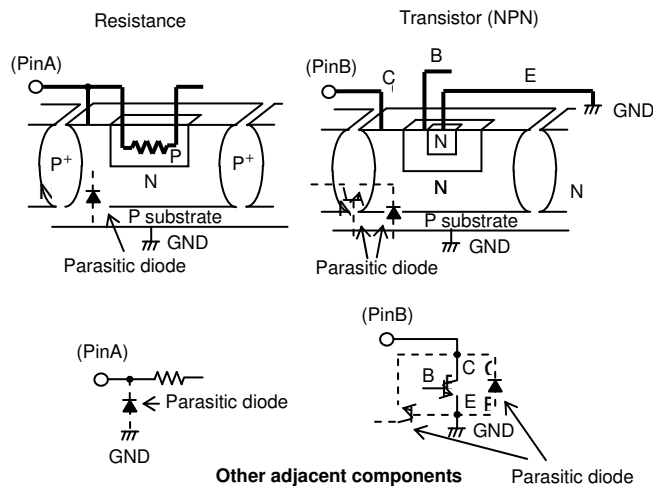


Fig-1 Simplified structure of a Bipolar IC

Notes

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