i.MX 6 and i.MX 7 Series Comparison Table

i.MX applications processors are multicore ARM®-based solutions for multimedia and display applications with scalability, high performance, and low power capabilities.

Features	i.MX 6QuadPlus / i.MX 6DualPlus	i.MX 6Quad/ i.MX 6Dual	i.MX 6DualLite	i.MX 6Solo	i.MX 6SoloX	i.MX 6SoloLite	i.MX 6UltraLite	i.MX 6ULL	i.MX 7Solo	i.MX 7Dual
CPU	(i.MX 6QuadPlus) 4 x Cortex®-A9 (i.MX 6DualPlus) 2 x Cortex-A9	(i.MX 6Quad) 4 x Cortex-A9 (i.MX 6Dual) 2 x Cortex-A9	2 x Cortex-A9	Cortex-A9	Cortex-A9, Cortex-M4	Cortex-A9	Cortex-A7	Cortex-A7	Cortex-A7, Cortex-M4	2 x Cortex-A7, Cortex-M4
Maximum CPU Frequency	1.2 GHz	1.2 GHz	1 GHz	1 GHz	(A9) 1 GHz (M4) 227 MHz	1 GHz	696 MHz	528 MHz	(A7) 800 MHz (M4) 200 MHz	(A7) 1.2 GHz (M4) 200 MHz
I-Cache/D-Cache	32 KB/32 KB L1, 1 MB L2	32 KB/32 KB L1, 1 MB L2	32 KB/32 KB L1, 512 KB L2	32 KB/32 KB L1, 512 KB L2	(A9) 32 KB/32 KB L1, 256 KB L2 (M4) 16 KB/16 KB L1	32 KB/32 KB L1, 256 KB L2	32 KB/32 KB L1, 128 KB L2*	32 KB/32 KB L1, 128 KB L2*	(A7) 32 KB/32 KB L1, 512 KB L2 (M4) 16 KB/16 KB L1	(A7) 32 KB/32 KB L1, 512 KB L2 (M4) 16 KB/16 KB L1
Embedded SRAM	512 KB	256 KB	128 KB	128 KB	128 KB	128 KB	128 KB	128 KB	256 KB	256 KB
External Memory Interface and DDR Bus Speed	2 x 32 LP-DDR2, 1-ch. x 64 DDR3/DDR3L, page and channel interleaving at up to 528 MHz, rawNAND	2 x 32 LP-DDR2, 1-ch. x 64 DDR3/DDR3L, page and channel interleaving at up to 528 MHz, rawNAND	2 x 32 LP-DDR2, 1-ch. x 64 DDR3/DDR3L page and channel interleaving at 400 MHz, rawNAND	1 x 32 LP-DDR2, DDR3/DDR3L page and channel interleaving at 400 MHz, rawNAND	1 x 32 LP-DDR2, DDR3/DDR3L page and channel interleaving at 400 MHz, rawNAND, QuadSPI NOR	1 x 32 LP-DDR2, DDR3/DDR3L at 400 MHz	1 x 16 LP-DDR2, DDR3/DDR3L at 400 MHz, rawNAND, QuadSPI NOR	1 x 16 LP-DDR2, DDR3/DDR3L at 400 MHz, rawNAND, QuadSPI NOR	32/16-bit LP-DDR2, DDR3, DDR3L, and LPDDR3 up to 533 MHz, rawNAND, QuadSPI NOR	32/16-bit LP-DDR2, DDR3, DDR3L, and LPDDR3 up to 533 MHz, rawNAND, QuadSPI NOR
Display Interface	HDMI + PHY, 2 x parallel, 2 x LVDS, MIPI DSI	HDMI + PHY, 2x parallel, 2 x LVDS, MIPI DSI	HDMI + PHY, 1 x parallel, 2 x LVDS, MIPI DSI, EPDC	HDMI + PHY, 1 x parallel, 2 x LVDS, MIPI DSI, EPDC	1 x parallel, 1 x LVDS	1 x parallel, EPDC	1 x parallel*, touchscreen controller	1 x parallel*, touchscreen controller	24-bit parallel RGB, MIPI DSI	24-bit parallel RGB, MIPI DSI, EPDC
LCD Resolution	2 x QXGA (2048 x 1536) or 2 x WXGA (1280 x 720)	2 x QXGA (2048 x 1536) or 2 x WXGA (1280 x 720)	2 x WXGA (1280 x 720)	2 x WXGA (1280 x 720)	2 x WXGA (1280 x 720)*	SXGA+ (1400 x 1050)	WXGA (1366 x 768)*	WXGA (1366 x 768)*	1080p (1920 x 1080), SXGA+ (1400 x 1050)	1080p (1920 x 1080), SXGA+ (1400 x 1050)
Hardware Video Acceleration^	HD (1080 + 720)p30 video decode, HD 1080p30 video encode	HD (1080 + 720)p30 video decode, HD 1080p30 video encode	HD (1080 + 720)p30 video decode, HD 1080p30 video encode	HD1080p30 video decode, HD 1080p30 encode	SW Only	SW Only	SW Only	SW Only	SW Only	SW Only
Hardware 2D/3D Graphics Acceleration	OpenGL® ES 1.1/2.0/3.0 OpenCL™ 1.1 EP, OpenVG™ 1.1, 2DBLT, 8 layer composition, 4 shaders—720 MHz, embedded prefetch & resolve engine	OpenGL® ES 1.1/2.0/3.0 OpenCL™ 1.1 EP, OpenVG™ 1.1, 2DBLT, 2 layer composition, 4 shaders—594 MHz	OpenGL ES 1.1/2.0/3.0, OpenVG 1.1, 2DBLT, 2 layer composition, 1 shader—528 MHz	OpenGL ES 1.1/2.0/3.0 OpenVG 1.1, 2DBLT, 1 shader—528 Mhz	OpenGL ES 1.1/2.0, OpenVG 1.1, 2DBLT, 1 shader—720 MHz	OpenVG 1.1, 2DBLT 2 layer composition	No, but has a PxP*	No, but has a PxP*	No, but has a PxP*	No, but has a PxP*
Camera Sensor Interface (CSI)	Parallel CSI, MIPI CSI	Parallel CSI, MIPI CSI	Parallel CSI, MIPI CSI	Parallel CSI, MIPI CSI	Parallel CSI, Analog	Parallel CSI	Parallel CSI*	Parallel CSI*	Parallel CSI, MIPI CSI	Parallel CSI, MIPI CSI
Universal Asynchronous Receiver/ Transmitter (UART)	5	5	5	5	6	5	8*	8*	7	7
Serial Peripheral Interface (SPI)/I^2C	5/3	5/3	4/4	4/4	4/4	4/4	4/4*	4/4*	4/4	4/4
USB Controller	1 x HS USB 2.0 OTG + PHY 1 x HS USB 2.0 Host + PHY 2 x HS USB 2.0 Host (HSIC)	1 x HS USB 2.0 OTG + PHY 1 x HS USB 2.0 Host + PHY 2 x HS USB 2.0 Host (HSIC)	1 x HS USB 2.0 OTG + PHY 1 x HS USB 2.0 Host + PHY 2 x HS USB 2.0 Host (HSIC)	1 x HS USB 2.0 OTG + PHY 1 x HS USB 2.0 Host + PHY 2 x HS USB 2.0 Host (HSIC)	2 x HS USB 2.0 OTG + PHY 1 x HS USB 2.0 Host (HSIC)	2 x HS USB 2.0 OTG + PHY 1 x HS USB 2.0 Host (HSIC)	2 x HS USB 2.0 OTG + PHY*	2 x HS USB 2.0 OTG + PHY*	1 x HS USB 2.0 OTG + PHY 1 x HS USB 2.0 Host (HSIC)	2 x HS USB 2.0 OTG + PHY 1 x HS USB 2.0 Host (HSIC)
Power Management	NXP MMPF0100	NXP MMPF0100	NXP MMPF0100	NXP MMPF0100/MMPF0200	NXP MMPF0100/MMPF0200	NXP MMPF0100/MMPF0200	Discrete	Discrete	NXP MC32PF3000/MC34PF3000	NXP MC32PF3000/MC34PF3000
Digital Audio Interface	SSI/I^2S x 3, ESAI, S/PDIF, ASRC	SSI/I^2S x 3, ESAI, S/PDIF, ASRC	SSI/I^2S x 3, ESAI, S/PDIF, ASRC	SSI/I^2S x 3, ESAI, S/PDIF, ASRC	SSI/I^2S x 5, ESAI, SAI, S/PDIF, ASRC	SSI/I^2S x 3, S/PDIF	SAI/I^2S x 3, S/PDIF, ASRC*	SAI/I^2S x 3, S/PDIF, ASRC*, ESAI x 1	3 x SAI	3 x SAI
Ethernet	1 Gbit/s + IEEE® 1588	1 Gbit/s + IEEE 1588	1 Gbit/s + IEEE 1588	1 Gbit/s + IEEE 1588	2 x 1 Gbit/s + IEEE 1588 + AVB	10/100 Mbit/s	2 x 10/100 Mbit/s + IEEE 1588*	2 x 10/100 Mbit/s + IEEE 1588*	1 x Gbit w/AVB + IEEE 1588	2 x Gbit w/AVB + IEEE 1588
PCI Express®	PCIe® v2.0	PCIe v2.0	PCIe v2.0	PCIe v2.0	PCIe v2.0*	No	No	No	No	PCIe v2.1
CAN	2	2	2	2	2	No	2*	2*	2	2
Multimedia Card (eMMC)/Secure Digital Controller (SDIO)	4 x eMMC 4.5 / SD 3.0	4 x eMMC 4.5 / SD 3.0	4 x eMMC 4.5 / SD 3.0	4 x eMMC 4.5 / SD 3.0	4 x eMMC 4.5 / SD 3.0	4 x eMMC 4.5 / SD 3.0	2 x eMMC 4.5 / SD 3.0	2 x eMMC 4.5 / SD 3.0	2 x eMMC 5.0 / SD 3.0	3 x eMMC 5.0 / SD 3.0
Hard Disk Drive Interface	S-ATA II 3 Gbit/s	S-ATA II 3 Gbit/s	No	No	No	No	No	No	No	No
Smart Card Interface Module	No	No	No	No	No	No	Yes* (ISO7816-3)	No	2	2
Security	Secure Boot, RNG, Tamper Detection, secure storage, AES-128, DES 3DES, ARC4, MD5, SHA-1, SHA-224, SHA-256, 16 KB Secure RAM, tamper-resistant RTC, secure debug, OTP Space	Secure Boot, RNG, Tamper Detection, secure storage, AES-128, DES 3DES, ARC4, MD5, SHA-1, SHA-224, SHA-256, 16 KB Secure RAM, tamper-resistant RTC, secure debug, OTP Space	Secure Boot, RNG, Tamper Detection, secure storage, AES-128, DES 3DES, ARC4, MD5, SHA-1, SHA-224, SHA-256, 16 KB Secure RAM, tamper-resistant RTC, secure debug, OTP Space	Secure Boot, RNG, Tamper Detection, secure storage, AES-128, DES 3DES, ARC4, MD5, SHA-1, SHA-224, SHA-256, 16 KB Secure RAM, tamper-resistant RTC, secure debug, OTP Space	Secure Boot, RNG, Tamper Detection, secure storage, AES-128, DES 3DES, ARC4, MD5, SHA-1, SHA-224, SHA-256, 16 KB Secure RAM, tamper-resistant RTC, secure debug, OTP Space	Secure Boot, tamper reaction, RNG, key storage, AES, DES, 3DES, ARC4, MD5, SHA-1, SHA-256, 128 KB Secure RAM, secure debug	Secure Boot, RNG, Tamper Detection, Secure Storage (including 32 KB Secure RAM), Cryptographic Accelerators (AES-128, DES 3DES, ARC4, MD5, SHA-1, SHA-224, SHA-256, RSA/ECDSA), Secure Debug, OTP Space	Secure Boot, RNG, AES-128	ARM Trust Zone, Secure Boot, RNG, Tamper Detection, secure storage, AES-128, AES-256, DES, 3DES, ARC4, RSA (up to 4096), ECDSA, MD5, SHA-1, SHA-224, SHA-256, 32 KB Secure RAM, tamper-resistant RTC, secure debug, OTP Space	ARM Trust Zone, Secure Boot, RNG, Tamper Detection, secure storage, AES-128, AES-256, DES, 3DES, ARC4, RSA (up to 4096), ECDSA, MD5, SHA-1, SHA-224, SHA-256, 32 KB Secure RAM, tamper-resistant RTC, secure debug, OTP Space
Timer	3	3	3	3	3	3	4*	4*	2 x FlexTimer, 4 x GPT	2 x FlexTimer, 4 x GPT
Real-Time Clock	Secure RTC	Secure RTC	Secure RTC	Secure RTC	Secure RTC	Secure RTC	Secure RTC	Secure RTC	Secure RTC	Secure RTC
Pulse Width Modulation	4	4	4	4	8	4	8*	8*	4	4
Package	21 x 21 BGA 0.8 mm pitch	21 x 21 BGA 0.8 mm pitch, POP#	21 x 21 BGA 0.8 mm pitch	21 x 21 BGA 0.8 mm pitch	14 x 14 BGA 0.65 mm pitch 17 x 17 BGA 0.8 mm pitch 19 x 19 BGA 0.8 mm pitch	13 x 13 BGA 0.5 mm pitch	14 x 14 289 BGA 0.8 mm pitch 9 x 9 289 BGA 0.5 mm pitch	14 x 14 289 BGA 0.8 mm pitch 9 x 9 289 BGA 0.5 mm pitch	12 x 12 BGA 0.4 mm pitch 19 x 19 BGA 0.75 mm pitch	12 x 12 BGA 0.4 mm pitch 19 x 19 BGA 0.75 mm pitch
ADC Channels	No	No	No	No	Yes*	No	Yes, Two 12-bit ADC, 1 with touch controller, up to 10 channel*	Yes, Two 12-bit ADC, 1 with touch controller, up to 10 channel*	2 x 12-bit ADC	2 x 12-bit ADC
Qualifications	Automotive, commercial and industrial	Automotive, commercial and industrial	Automotive, commercial and industrial	Automotive, commercial and industrial	Automotive, commercial and industrial	Commercial	Automotive, commercial and industrial	Commercial and industrial	Commercial and industrial	Commercial and industrial

General Note1: Refer to IC documentation for specifications per processor.
General Note 2: The number of interfaces is dependent on the pin muxing.
* Some features vary across packages.
^ Performance dependent on application use case.
\# Refer to IC documentation for POP Package ARM and DDR frequencies and further details.

www.nxp.com/iMX6Series and **www.nxp.com/iMX7Series**

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Please note: The product data sheet and reference manual are your best source for the most current and detailed technical data on the i.MX applications processor you prefer. For documentation on i.MX applications processors, visit **www.nxp.com/iMX**. Share ideas, design tips and meet other i.MX fans at **iMXcommunity.org**.