REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Add one vendor, CAGE 18324. Inactivate Military drawing part numbers 5962-8778801FX, 5962-8778801EX, for new design. Add paragraph 4.5 and make editorial changes throughout.	88-09-16	M. A. Frye
B	Changed generic number and vendor similar part number. Changes to table I. Remove programming procedures for method A. Deleted programming waveforms and table III. Editorial changes throughout.	90-01-17	M. A. Frye
C	Updated drawing to current requirements. Editorial changes throughout. – gap	01-04-03	Raymond Monnin

THE ORIGINAL FIRST PAGE OF THIS DRAWING HAS BEEN REPLACED.

REV																				
SHEET																				
REV																				
SHEET																				
REV STATUS				REV			C	C	C	C	C	C	C	C	C	C	C			
OF SHEETS				SHEET			1	2	3	4	5	6	7	8	9	10	11			

PMIC N/A	PREPARED BY Monica L. Grosel	**DEFENSE SUPPLY CENTER COLUMBUS** **COLUMBUS, OHIO 43216** **http://www.dscc.dla.mil**
STANDARD MICROCIRCUIT DRAWING THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE AMSC N/A	CHECKED BY Ray Monnin	
	APPROVED BY Michael A. Frye	MICROCIRCUIT, MEMORY, DIGITAL, 256 X 4-BIT BIPOLAR PROM, MONOLITHIC SILICON
	DRAWING APPROVAL DATE 88-03-01	
	REVISION LEVEL C	SIZE A / CAGE CODE **67268** / **5962-87788**
		SHEET 1 OF 11

DSCC FORM 2233
APR 97

5962-E287-01

DISTRIBUTION STATEMENT A. Approved for public release; distribution is unlimited.

1. SCOPE

1.1 Scope. This drawing describes device requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A.

1.2 Part or Identifying Number (PIN). The complete PIN is as shown in the following example:

5962-87788	01	E	X
Drawing number	Device type (see 1.2.1)	Case outline (see 1.2.2)	Lead finish (see 1.2.3)

1.2.1 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function	Access time
01	27S21, 82S129	256 x 4-bit bipolar PROM (three-state)	60 ns
02	27S21A, 82S129A	256 x 4-bit bipolar PROM (three-state)	40 ns

1.2.2 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
E	GDIP1-T16 or CDIP2-T16	16	Dual-in-line
F	GDFP2-F16 or CDFP3-F16	16	Flat package
2	CQCC1-N20	20	Square leadless chip carrier

1.2.3 Lead finish. The lead finish is as specified in MIL-PRF-38535, appendix A.

1.3 Absolute maximum ratings.

Supply voltage range	-0.5 V dc to +7.0 V dc
Input voltage range	-0.5 V dc to +5.5 V dc
Storage temperature range	-65°C to +150°C
Maximum power dissipation (P_D) per device 1/	715 mW
Lead temperature (soldering, 10 seconds)	+300°C
Thermal resistance, junction-to-case (θ_{JC}) 2/	See MIL-STD-1835
Junction temperature (T_J)	+175°C
DC voltage applied to outputs range (except during programming)	-0.5 V dc to +5.5 V dc maximum
DC voltage applied to outputs during programming	21 V dc
Output current into outputs during programming (maximum duration of 1 second)	250 mA
DC input current range	-30 mA to +5.0 mA

1/ Must withstand the added P_D due to short circuit test, e.g., I_{OS}.
2/ Heat sinking is recommended to reduce the junction temperature.

1.4 Recommended operating conditions.

Supply voltage range (V_{CC})	4.5 V dc minimum to 5.5 V dc maximum
Minimum high level input voltage (V_{IH})	2.0 V dc
Maximum low level input voltage (V_{IL})	0.8 V dc
Case operating temperature range (T_C)	-55°C to +125°C

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those listed in the issue of the Department of Defense Index of Specifications and Standards (DoDISS) and supplement thereto, cited in the solicitation.

SPECIFICATION

DEPARTMENT OF DEFENSE

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

STANDARDS

DEPARTMENT OF DEFENSE

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

HANDBOOKS

DEPARTMENT OF DEFENSE

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Unless otherwise indicated, copies of the specification, standards, and handbooks are available from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein. Product built to this drawing that is produced by a Qualified Manufacturer Listing (QML) certified and qualified manufacturer or a manufacturer who has been granted transitional certification to MIL-PRF-38535 may be processed as QML product in accordance with the manufacturers approved program plan and qualifying activity approval in accordance with MIL-PRF-38535. This QML flow as documented in the Quality Management (QM) plan may make modifications to the requirements herein. These modifications shall not affect form, fit, or function of the device. These modifications shall not affect the PIN as described herein. A "Q" or "QML" certification mark in accordance with MIL-PRF-38535 is required to identify when the QML flow option is used

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535, appendix A and herein.

3.2.1 Case outlines. The case outlines shall be in accordance with 1.2.2 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.2 Truth table. The truth table shall be as specified on figure 2.

3.2.2.1 Unprogrammed devices. The truth table for unprogrammed devices shall be as specified on figure 2.

3.2.2.2 Programmed devices. The requirements for supplying programmed devices are not part of this drawing.

3.2.3 Logic diagram(s). The logic diagram(s) shall be as specified on figure 3.

3.2.4 Switching test circuit. The switching test circuit shall be as specified on figure 4.

3.2.5 Switching waveforms. The switching waveforms shall be as specified on figure 5.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

3.5 Marking. Marking shall be in accordance with MIL-PRF-38535, appendix A. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked as listed in MIL-HDBK-103 (see 6.6 herein). For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device.

3.5.1 Certification/compliance mark. A compliance indicator “C” shall be marked on all non-JAN devices built in compliance to MIL-PRF-38535, appendix A. The compliance indicator “C” shall be replaced with a "Q" or "QML" certification mark in accordance with MIL-PRF-38535 to identify when the QML flow option is used.

3.6 Processing options. Since the PROM is an unprogrammed memory capable of being programmed by either the manufacturer or the user to result in a wide variety of PROM configurations, two processing options are provided for selection in the contract, using an altered item drawing.

3.6.1 Unprogrammed PROM delivered to the user. All testing shall be verified through group A testing as defined in 4.3.1. It is recommended that users perform subgroups 7 and 9 after programming to verify the specific program configuration.

3.6.2 Manufacturer-programmed PROM delivered to the user. All testing requirements and quality assurance provisions herein, including the requirements of the altered item drawing shall be satisfied by the manufacturer prior to delivery.

3.7 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply shall affirm that the manufacturer's product meets the requirements of MIL-PRF-38535, appendix A and the requirements herein.

3.8 Certificate of conformance. A certificate of conformance as required in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.9 Notification of change. Notification of change to DSCC-VA shall be required in accordance with MIL-PRF-38535, appendix A.

3.10 Verification and review. DSCC, DSCC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Output high voltage	V_{OH}	V_{CC} = 4.5 V, I_{OH} = -2.0 mA V_{IH} = 2.0 V, V_{IL} = 0.8 V	1, 2, 3	All	2.4		V
Output low voltage	V_{OL}	V_{CC} = 4.5 V, I_{OL} = 16 mA V_{IH} = 2.0 V, V_{IL} = 0.8 V	1, 2, 3			.5	V
Input high level current	I_{IH}	V_{CC} = 5.5 V, V_{IN} = 5.5 V	1, 2, 3			40	µA
Input low level current	I_{IL}	V_{CC} = 5.5 V, V_{IN} = 0.45 V	1, 2, 3			-250	µA
Power supply current	I_{CC}	V_{CC} = 5.5 V, V_{IN} = 0.0 V	1, 2, 3			130	mA
Input clamp voltage	V_{IC}	V_{CC} = 4.5 V, I_{IN} = -18 mA	1, 2, 3			-1.2	V
High output leakage current	I_{OZH}	V_{CC} = 5.5 V, V_{IH} = 2.0 V, V_O = 4.5 V	1, 2, 3			40	µA
	I_{OZL}	V_{IL} = 0.8 V, V_{CS} = 2.4 V, V_O = 0.4 V				-40	
Output short circuit current	I_{OS}	V_{CC} = 5.5 V V_{OUT} = 0.0 V 1/	1, 2, 3		-15	90	mA
Functional tests		See 4.3.1d	7, 8				
Address access time	t_{AVQV}	C_L = 50 pF S1 is closed See figures 4 and 5	9, 10, 11	01		60	ns
				02		40	
Enable access time	t_{GVQV}	See figures 4 and 5 2/	9, 10, 11	01		30	ns
				02		25	
Enable recovery time	t_{GVQZ}	See figures 4 and 5 2/	9, 10, 11	01		30	ns
				02		25	

1/ Not more than one output should be shorted at a time and the duration of the short circuit condition should not exceed one second.

2/ t_{GVQV} is tested with C_L = 50 pF to the 1.5 V level; S1 is open for high impedance to high tests and closed for high impedance to low tests. t_{GVQZ} is tested with C_L = 5 pF. High to high impedance tests are made with S1 open to an output voltage of V_{OH} - 0.5 V. Low to high impedance tests are made with S1 closed to the V_{OL} + 0.5 V level.

Device Types	All	
Case Outlines	E and F	2
Terminal number	Terminal symbol	
1	A_6	NC
2	A_5	A_6
3	A_4	A_5
4	A_3	A_4
5	A_0	A_3
6	A_1	A_0
7	A_2	A_1
8	GND	A_2
9	O_3	NC
10	O_2	GND
11	O_1	NC
12	O_0	O_3
13	$\overline{CS}$ 1	O_2
14	$\overline{CS}$ 2	O_1
15	A_7	NC
16	V_{CC}	O_0
17	---	$\overline{CS}$ 1
18	---	$\overline{CS}$ 2
19	---	A_7
20	---	V_{CC}

FIGURE 1. Terminal connections.

Word No.	Enable		Address								Data			
	$\overline{CS}$ 1	$\overline{CS}$ 2	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	O_3	O_2	O_1	O_0
NA	L	L	X	X	X	X	X	X	X	X	L	L	L	L
	H	H	X	X	X	X	X	X	X	X	OC	OC	OC	OC
	H	L	X	X	X	X	X	X	X	X	OC	OC	OC	OC
	L	H	X	X	X	X	X	X	X	X	OC	OC	OC	OC

NOTES:
1. NA = Not applicable.
2. X = Input may be high level, low level, or open circuit.
3. OC = Open circuit (high resistance output).
4. Program readout can only be accomplished with enable input at low level.

FIGURE 2. Truth table (unprogrammed).

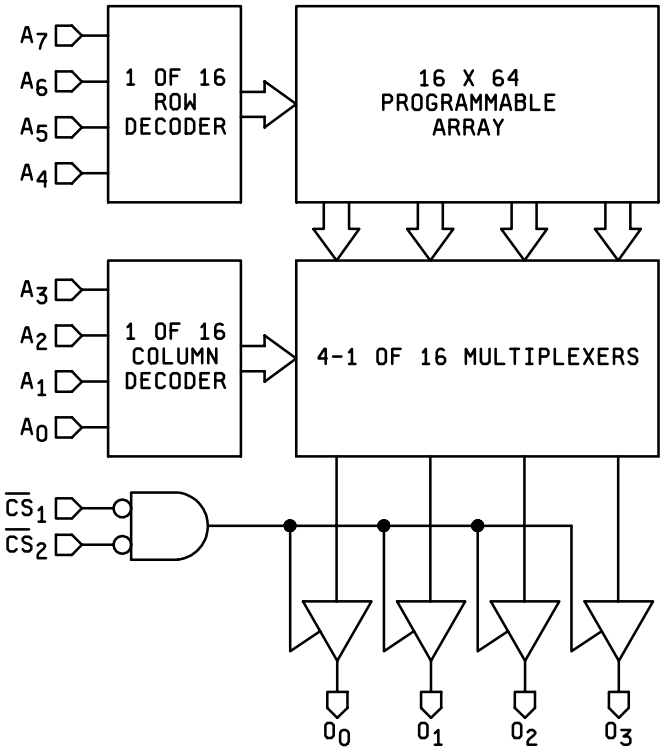
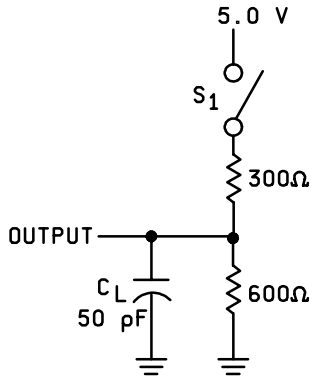


FIGURE 3. Logic diagram.

Output load for all tests except t_{GVQZ}

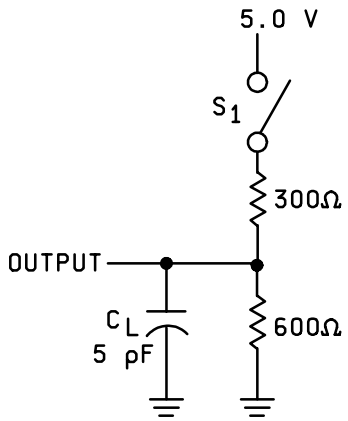


CIRCUIT A

NOTES:
1. All device test loads should be located within 2 inches of the device output pin.
2. S1 is open for output data high to hi-Z and hi-Z to output data high test.
   S1 is closed for all other AC test.
3. Load capacitance includes all stray and fixture capacitance.

FIGURE 4. Switching test circuit or equivalent.

Output load for t_{GVQZ}



CIRCUIT B

NOTES:
1. All device test loads should be located within 2 inches of the device output pin.
2. S1 is open for output data high to hi-Z and hi-Z to output data high test.
   S1 is closed for all other AC test.
3. Load capacitance includes all stray and fixture capacitance.

FIGURE 4. Switching test circuit or equivalent - Continued.

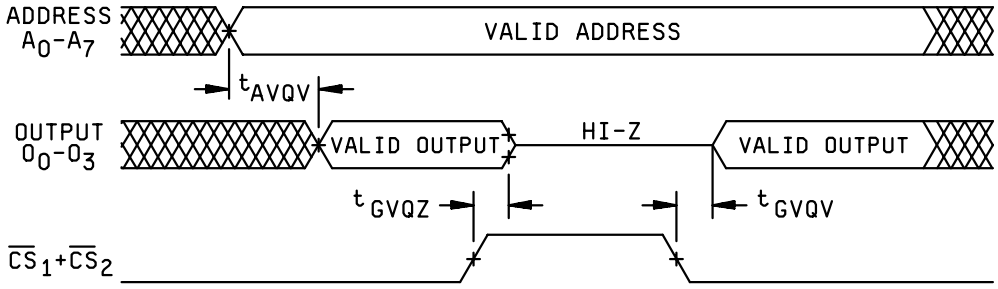


FIGURE 5. Switching waveforms.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition C or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015 of MIL-STD-883.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)
Interim electrical parameters (method 5004)	
Final electrical test parameters (method 5004)	1*, 2, 3, 7*, 8, 9, 10**, 11**
Group A test requirements (method 5005)	1, 2, 3, 7, 8, 9, 10**, 11**
Groups C and D end-point electrical parameters (method 5005)	1, 2, 3

* PDA applies to subgroup 1 and 7.
** Subgroups 10 and 11, if not tested shall be guaranteed to the limits specified in table I.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 4, 5, and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Unprogrammed devices shall be tested for programmability and ac performance compliance to the requirements of group A, subgroups 9, 10, and 11. Either of two techniques is acceptable.

(1) Testing the entire lot using additional built-in test circuitry which allows the manufacturer to verify programmability and ac performance without programming the user array. If this is done, the resulting test pattern shall be verified on all devices during subgroups 9, 10, and 11, group A testing in accordance with the sampling plan specified in method 5005 of MIL-STD-883.

(2) If such compliance cannot be tested on an unprogrammed device, a sample shall be selected to satisfy programmability requirements prior to performing subgroups 9, 10, and 11. Twelve devices shall be submitted to programming. If more than two devices fail to program, the lot shall be rejected. At the manufacturer's option, the sample may be increased to 24 total devices with no more than four total device failures allowed. Ten devices from the programmability sample shall be submitted to the requirements of group A, subgroups 9, 10, and 11. If more than two total devices fail, the lot shall be rejected. At the manufacturer's option, the sample may be increased to 20 total devices with no more than four total device failures allowable.

d. Subgroups 7 and 8 shall include verification of the truth table.

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test conditions, method 1005 of MIL-STD-883.

(1) Test condition C or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

(2) T_A = +125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.4 Programming procedures. Programming procedures shall be as specified by the device manufacturers.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535, appendix A.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.4 Record of users. Military and industrial users shall inform Defense Supply Center Columbus when a system application requires configuration control and the applicable SMD. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronics devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0544.

6.5 Comments. Comments on this drawing should be directed to DSCC-VA, Columbus, Ohio 43216-5000, or telephone (614) 692-0674.

6.6 Approved sources of supply. Approved sources of supply are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DSCC-VA.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 01-04-03

Approved sources of supply for SMD 5962-87788 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/	Reference military specification part numbers
5962-8778801FA	58625	SL82S129/BFA	MIL-M-38510/20304BFA
	0C7V7	82S129/BFA	
	3/	AM27S21/BFA	
5962-87788012A	3/	AM27S21/B2A	
5962-8778802EA	58625	SL82S129A/BEA	MIL-M-38510/20304BEA
	0C7V7	82S129A/BEA	
	3/	AM27S21A/BEA	
5962-8778802FA	58625	SL82S129A/BFA	MIL-M-38510/20304BFA
	0C7V7	82S129A/BFA	
	3/	AM27S21A/BFA	
5962-87788022A	3/	AM27S21A/B2A	

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.
2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.
3/ Not available from an approved source of supply.

Vendor CAGE number	Vendor name and address
58625	Lansdale Semiconductor, Inc. 2502 W Huntington Drive Tempe, AZ 85282-3134
0C7V7	Qualified Parts Laboratory, Inc. 3605 Kifer Road Santa Clara, CA 95051