

74VHC245; 74VHCT245

Octal bus transceiver; 3-state

Rev. 01 — 25 August 2009

Product data sheet

1. General description

The 74VHC245; 74VHCT245 are high-speed Si-gate CMOS devices.

The 74VHC245; 74VHCT245 are octal transceivers featuring non-inverting 3-state bus compatible outputs in both send and receive directions.

The 74VHC245; 74VHCT245 feature an output enable input (\overline{OE}), for easy cascading, and a send and receive direction control input (DIR).

\overline{OE} controls the outputs so that the buses are effectively isolated.

2. Features

- Balanced propagation delays
- All inputs have Schmitt-trigger action
- Inputs accept voltages higher than V_{CC}
- Input levels:
 - ◆ The 74VHC245 operates with CMOS input level
 - ◆ The 74VHCT245 operates with TTL input level
- ESD protection:
 - ◆ HBM JESD22-A114E exceeds 2000 V
 - ◆ MM JESD22-A115-A exceeds 200 V
 - ◆ CDM JESD22-C101C exceeds 1000 V
- Multiple package options
- Specified from $-40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$ and from $-40\text{ }^{\circ}\text{C}$ to $+125\text{ }^{\circ}\text{C}$

3. Ordering information

Table 1. Ordering information

| Type number | Package | | | Version |
|---------------------------|---|----------|---|----------|
| | Temperature range | Name | Description | |
| 74VHC245D 74VHCT245D | $-40\text{ }^{\circ}\text{C}$ to $+125\text{ }^{\circ}\text{C}$ | SO20 | plastic small outline package; 20 leads; body width 7.5 mm | SOT163-1 |
| 74VHC245PW 74VHCT245PW | $-40\text{ }^{\circ}\text{C}$ to $+125\text{ }^{\circ}\text{C}$ | TSSOP20 | plastic thin shrink small outline package; 20 leads; body width 4.4 mm | SOT360-1 |
| 74VHC245BQ 74VHCT245BQ | $-40\text{ }^{\circ}\text{C}$ to $+125\text{ }^{\circ}\text{C}$ | DHVQFN20 | plastic dual-in-line compatible thermal enhanced very thin quad flat package; no leads; 20 terminals; body $2.5 \times 4.5 \times 0.85\text{ mm}$ | SOT764-1 |

4. Functional diagram

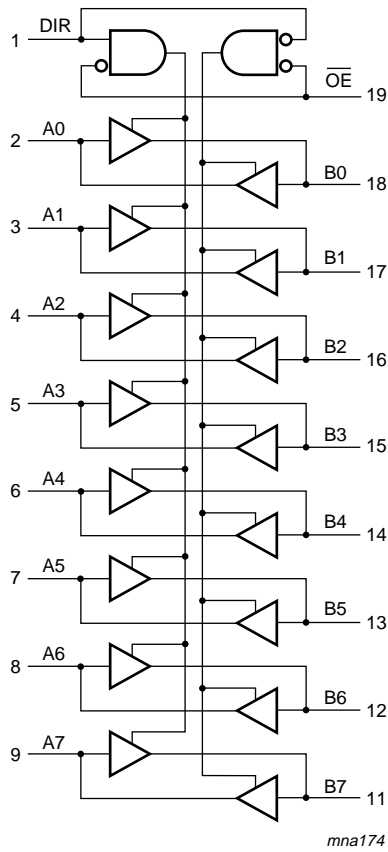


Fig 1. Logic symbol

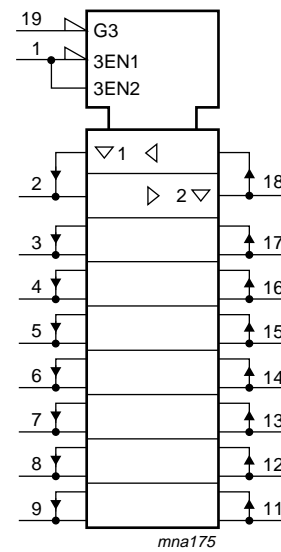
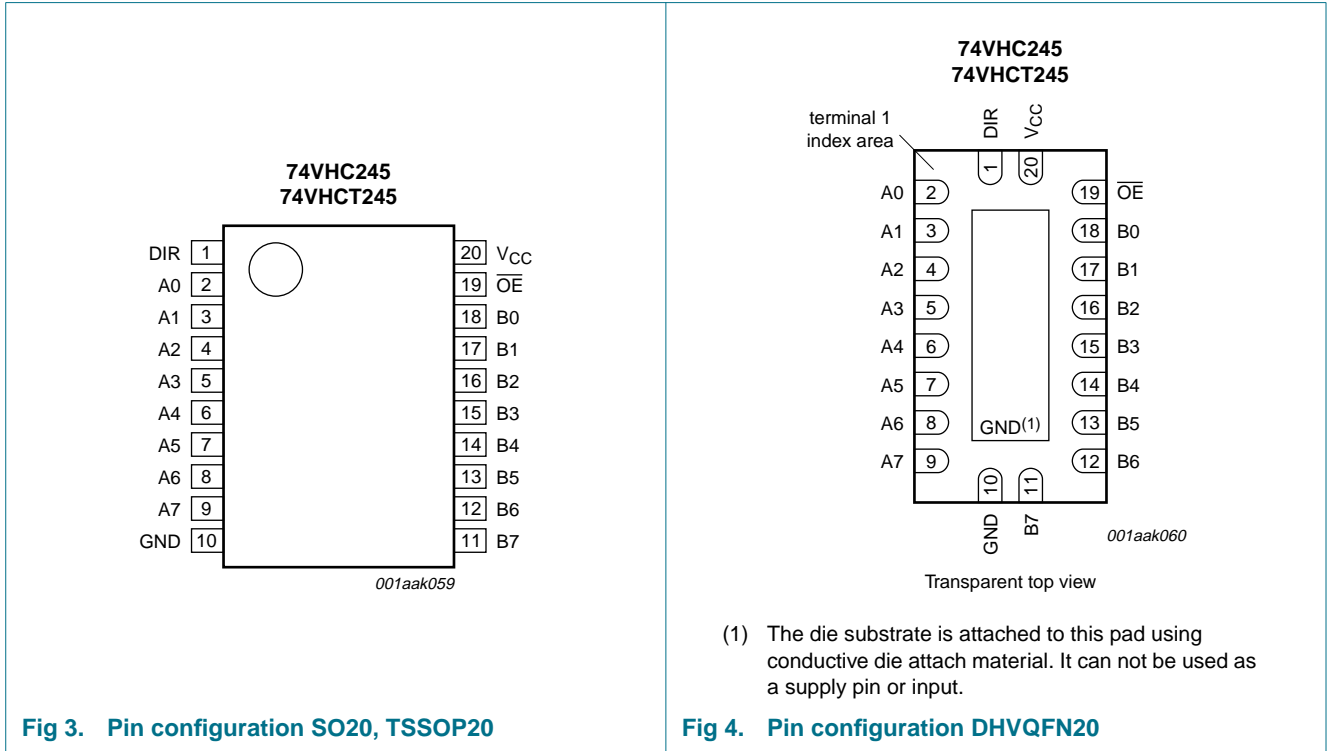


Fig 2. IEC logic symbol

5. Pinning information

5.1 Pinning



5.2 Pin description

Table 2. Pin description

| Symbol | Pin | Description |
|--------|-----|-------------------------|
| DIR | 1 | direction control input |
| A0 | 2 | data input/output |
| A1 | 3 | data input/output |
| A2 | 4 | data input/output |
| A3 | 5 | data input/output |
| A4 | 6 | data input/output |
| A5 | 7 | data input/output |
| A6 | 8 | data input/output |
| A7 | 9 | data input/output |
| GND | 10 | ground (0 V) |
| B7 | 11 | data input/output |
| B6 | 12 | data input/output |
| B5 | 13 | data input/output |
| B4 | 14 | data input/output |
| B3 | 15 | data input/output |
| B2 | 16 | data input/output |

Table 2. Pin description ...continued

| Symbol | Pin | Description |
|-----------------|-----|----------------------------------|
| B1 | 17 | data input/output |
| B0 | 18 | data input/output |
| \overline{OE} | 19 | output enable input (active LOW) |
| V_{CC} | 20 | supply voltage |

6. Functional description

Table 3. Function table^[1]

| Control | | Input/output | |
|-----------------|-----|--------------|--------|
| \overline{OE} | DIR | An | Bn |
| L | L | A = B | inputs |
| L | H | inputs | B = A |
| H | X | Z | Z |

- [1] H = HIGH voltage level;
 L = LOW voltage level;
 X = don't care;
 Z = high-impedance OFF-state.

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

| Symbol | Parameter | Conditions | Min | Max | Unit |
|-----------|-------------------------|--|---------|------|------|
| V_{CC} | supply voltage | | -0.5 | +7.0 | V |
| V_I | input voltage | | -0.5 | +7.0 | V |
| I_{IK} | input clamping current | $V_I < -0.5$ V | [1] -20 | - | mA |
| I_{OK} | output clamping current | $V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V | [1] -20 | +20 | mA |
| I_O | output current | $V_O = -0.5$ V to $(V_{CC} + 0.5$ V) | -25 | +25 | mA |
| I_{CC} | supply current | | - | +75 | mA |
| I_{GND} | ground current | | -75 | - | mA |
| T_{stg} | storage temperature | | -65 | +150 | °C |
| P_{tot} | total power dissipation | $T_{amb} = -40$ °C to +125 °C | [2] - | 500 | mW |

- [1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
 [2] For SO20 packages: above 70 °C the value of P_{tot} derates linearly at 8 mW/K.
 For TSSOP20 packages: above 60 °C the value of P_{tot} derates linearly at 5.5 mW/K.
 For DHVQFN20 packages: above 60 °C the value of P_{tot} derates linearly at 4.5 mW/K.

8. Recommended operating conditions

Table 5. Operating conditions

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---------------------|-------------------------------------|---|-----|-----|----------|------|
| 74VHC245 | | | | | | |
| V_{CC} | supply voltage | | 2.0 | 5.0 | 5.5 | V |
| V_I | input voltage | | 0 | - | 5.5 | V |
| V_O | output voltage | | 0 | - | V_{CC} | V |
| T_{amb} | ambient temperature | | -40 | +25 | +125 | °C |
| $\Delta t/\Delta V$ | input transition rise and fall rate | $V_{CC} = 3.0\text{ V to }3.6\text{ V}$ | - | - | 100 | ns/V |
| | | $V_{CC} = 4.5\text{ V to }5.5\text{ V}$ | - | - | 20 | ns/V |
| 74VHCT245 | | | | | | |
| V_{CC} | supply voltage | | 4.5 | 5.0 | 5.5 | V |
| V_I | input voltage | | 0 | - | 5.5 | V |
| V_O | output voltage | | 0 | - | V_{CC} | V |
| T_{amb} | ambient temperature | | -40 | +25 | +125 | °C |
| $\Delta t/\Delta V$ | input transition rise and fall rate | $V_{CC} = 4.5\text{ V to }5.5\text{ V}$ | - | - | 20 | ns/V |

9. Static characteristics

Table 6. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

| Symbol | Parameter | Conditions | 25 °C | | | -40 °C to +85 °C | | -40 °C to +125 °C | | Unit |
|-----------------|--|--|-------|------|------|------------------|------|-------------------|------|------|
| | | | Min | Typ | Max | Min | Max | Min | Max | |
| 74VHC245 | | | | | | | | | | |
| V_{IH} | HIGH-level input voltage | $V_{CC} = 2.0\text{ V}$ | 1.5 | - | - | 1.5 | - | 1.5 | - | V |
| | | $V_{CC} = 3.0\text{ V}$ | 2.1 | - | - | 2.1 | - | 2.1 | - | V |
| | | $V_{CC} = 5.5\text{ V}$ | 3.85 | - | - | 3.85 | - | 3.85 | - | V |
| V_{IL} | LOW-level input voltage | $V_{CC} = 2.0\text{ V}$ | - | - | 0.5 | - | 0.5 | - | 0.5 | V |
| | | $V_{CC} = 3.0\text{ V}$ | - | - | 0.9 | - | 0.9 | - | 0.9 | V |
| | | $V_{CC} = 5.5\text{ V}$ | - | - | 1.65 | - | 1.65 | - | 1.65 | V |
| V_{OH} | HIGH-level output voltage | $V_I = V_{IH}$ or V_{IL} | | | | | | | | |
| | | $I_O = -50\ \mu\text{A}$; $V_{CC} = 2.0\text{ V}$ | 1.9 | 2.0 | - | 1.9 | - | 1.9 | - | V |
| | | $I_O = -50\ \mu\text{A}$; $V_{CC} = 3.0\text{ V}$ | 2.9 | 3.0 | - | 2.9 | - | 2.9 | - | V |
| | | $I_O = -50\ \mu\text{A}$; $V_{CC} = 4.5\text{ V}$ | 4.4 | 4.5 | - | 4.4 | - | 4.4 | - | V |
| | | $I_O = -4.0\text{ mA}$; $V_{CC} = 3.0\text{ V}$ | 2.58 | - | - | 2.48 | - | 2.40 | - | V |
| | $I_O = -8.0\text{ mA}$; $V_{CC} = 4.5\text{ V}$ | 3.94 | - | - | 3.80 | - | 3.70 | - | V | |
| V_{OL} | LOW-level output voltage | $V_I = V_{IH}$ or V_{IL} | | | | | | | | |
| | | $I_O = 50\ \mu\text{A}$; $V_{CC} = 2.0\text{ V}$ | - | 0 | 0.1 | - | 0.1 | - | 0.1 | V |
| | | $I_O = 50\ \mu\text{A}$; $V_{CC} = 3.0\text{ V}$ | - | 0 | 0.1 | - | 0.1 | - | 0.1 | V |
| | | $I_O = 50\ \mu\text{A}$; $V_{CC} = 4.5\text{ V}$ | - | 0 | 0.1 | - | 0.1 | - | 0.1 | V |
| | | $I_O = 4.0\text{ mA}$; $V_{CC} = 3.0\text{ V}$ | - | - | 0.36 | - | 0.44 | - | 0.55 | V |
| | $I_O = 8.0\text{ mA}$; $V_{CC} = 4.5\text{ V}$ | - | - | 0.36 | - | 0.44 | - | 0.55 | V | |

Table 6. Static characteristics ...continued

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

| Symbol | Parameter | Conditions | 25 °C | | | -40 °C to +85 °C | | -40 °C to +125 °C | | Unit |
|------------------|---------------------------|---|-------|-----|------------|------------------|-----------|-------------------|------------|---------------|
| | | | Min | Typ | Max | Min | Max | Min | Max | |
| I_I | input leakage current | $V_I = 5.5 \text{ V}$ or GND; $V_{CC} = 0 \text{ V}$ to 5.5 V | - | - | 0.1 | - | 1.0 | - | 2.0 | μA |
| I_{OZ} | OFF-state output current | $V_I = V_{IH}$ or V_{IL} ; $V_O = V_{CC}$ or GND; $V_{CC} = 5.5 \text{ V}$ | - | - | ± 0.25 | - | ± 2.5 | - | ± 10.0 | μA |
| I_{CC} | supply current | $V_I = V_{CC}$ or GND; $I_O = 0 \text{ A}$; $V_{CC} = 5.5 \text{ V}$ | - | - | 4.0 | - | 40 | - | 80 | μA |
| C_I | input capacitance | $V_I = V_{CC}$ or GND | - | 3 | 10 | - | 10 | - | 10 | pF |
| C_O | output capacitance | | - | 4 | - | - | - | - | - | pF |
| 74VHCT245 | | | | | | | | | | |
| V_{IH} | HIGH-level input voltage | $V_{CC} = 4.5 \text{ V}$ to 5.5 V | 2.0 | - | - | 2.0 | - | 2.0 | - | V |
| V_{IL} | LOW-level input voltage | $V_{CC} = 4.5 \text{ V}$ to 5.5 V | - | - | 0.8 | - | 0.8 | - | 0.8 | V |
| V_{OH} | HIGH-level output voltage | $V_I = V_{IH}$ or V_{IL} ; $V_{CC} = 4.5 \text{ V}$ $I_O = -50 \mu\text{A}$ | 4.4 | 4.5 | - | 4.4 | - | 4.4 | - | V |
| | | $I_O = -8.0 \text{ mA}$ | 3.94 | - | - | 3.80 | - | 3.70 | - | V |
| | | | | | | | | | | |
| V_{OL} | LOW-level output voltage | $V_I = V_{IH}$ or V_{IL} ; $V_{CC} = 4.5 \text{ V}$ $I_O = 50 \mu\text{A}$ | - | 0 | 0.1 | - | 0.1 | - | 0.1 | V |
| | | $I_O = 8.0 \text{ mA}$ | - | - | 0.36 | - | 0.44 | - | 0.55 | V |
| | | | | | | | | | | |
| I_I | input leakage current | $V_I = 5.5 \text{ V}$ or GND; $V_{CC} = 0 \text{ V}$ to 5.5 V | - | - | 0.1 | - | 1.0 | - | 2.0 | μA |
| I_{OZ} | OFF-state output current | $V_I = V_{IH}$ or V_{IL} ; $V_O = V_{CC}$ or GND per input pin; other inputs at V_{CC} or GND; $I_O = 0 \text{ A}$; $V_{CC} = 5.5 \text{ V}$ | - | - | ± 0.25 | - | ± 2.5 | - | ± 10.0 | μA |
| I_{CC} | supply current | $V_I = V_{CC}$ or GND; $I_O = 0 \text{ A}$; $V_{CC} = 5.5 \text{ V}$ | - | - | 4.0 | - | 40 | - | 80 | μA |
| ΔI_{CC} | additional supply current | per input pin; $V_I = V_{CC} - 2.1 \text{ V}$; other pins at V_{CC} or GND; $I_O = 0 \text{ A}$; $V_{CC} = 4.5 \text{ V}$ to 5.5 V | - | - | 1.35 | - | 1.5 | - | 1.5 | mA |
| C_I | input capacitance | $V_I = V_{CC}$ or GND | - | 3 | 10 | - | 10 | - | 10 | pF |
| C_O | output capacitance | | - | 4 | - | - | - | - | - | pF |

10. Dynamic characteristics

Table 7. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V); for test circuit see [Figure 7](#).

| Symbol | Parameter | Conditions | 25 °C | | | –40 °C to +85 °C | | –40 °C to +125 °C | | Unit |
|--|-------------------------------|---|---------------------|--------------------|------|------------------|------|-------------------|------|------|
| | | | Min | Typ ^[1] | Max | Min | Max | Min | Max | |
| 74VHC245 | | | | | | | | | | |
| t_{pd} | propagation delay | An to Bn; Bn to An; see Figure 5 | [2] | | | | | | | |
| | | $V_{CC} = 3.0\text{ V to }3.6\text{ V}$ | | | | | | | | |
| | | $C_L = 15\text{ pF}$ | - | 5.0 | 8.4 | 1.0 | 10.0 | 1.0 | 10.5 | ns |
| | | $C_L = 50\text{ pF}$ | - | 6.5 | 11.9 | 1.0 | 13.5 | 1.0 | 15.0 | ns |
| | | $V_{CC} = 4.5\text{ V to }5.5\text{ V}$ | | | | | | | | |
| | | $C_L = 15\text{ pF}$ | - | 3.5 | 5.5 | 1.0 | 6.5 | 1.0 | 7.0 | ns |
| t_{en} | enable time | \overline{OE} to An; \overline{OE} to Bn; signal name DIR; see Figure 6 | [3] | | | | | | | |
| | | $V_{CC} = 3.0\text{ V to }3.6\text{ V}$ | | | | | | | | |
| | | $C_L = 15\text{ pF}$ | - | 6.5 | 13.2 | 1.0 | 15.5 | 1.0 | 16.5 | ns |
| | | $C_L = 50\text{ pF}$ | - | 9.0 | 16.7 | 1.0 | 19.0 | 1.0 | 21.0 | ns |
| | | $V_{CC} = 4.5\text{ V to }5.5\text{ V}$ | | | | | | | | |
| | | $C_L = 15\text{ pF}$ | - | 4.0 | 8.5 | 1.0 | 10.0 | 1.0 | 11.0 | ns |
| t_{dis} | disable time | \overline{OE} to An; \overline{OE} to Bn; signal name DIR; see Figure 6 | [4] | | | | | | | |
| | | $V_{CC} = 3.0\text{ V to }3.6\text{ V}$ | | | | | | | | |
| | | $C_L = 15\text{ pF}$ | - | 7.5 | 12.5 | 1.0 | 15.5 | 1.0 | 16.0 | ns |
| | | $C_L = 50\text{ pF}$ | - | 10.0 | 15.8 | 1.0 | 18.0 | 1.0 | 20.0 | ns |
| | | $V_{CC} = 4.5\text{ V to }5.5\text{ V}$ | | | | | | | | |
| | | $C_L = 15\text{ pF}$ | - | 4.5 | 7.8 | 1.0 | 9.2 | 1.0 | 10.0 | ns |
| C_{PD} | power dissipation capacitance | $f_i = 1\text{ MHz}; V_i = \text{GND to }V_{CC}$ | [5] | - | 12 | - | - | - | - | pF |
| | | $C_L = 50\text{ pF}$ | - | 6.0 | 9.7 | 1.0 | 11.0 | 1.0 | 12.5 | ns |
| 74VHCT245; $V_{CC} = 4.5\text{ V to }5.5\text{ V}$ | | | | | | | | | | |
| t_{pd} | propagation delay | An to Bn; Bn to An; see Figure 5 | [2] | | | | | | | |
| | | $C_L = 15\text{ pF}$ | - | 3.5 | 7.7 | 1.0 | 8.5 | 1.0 | 10.0 | ns |
| | | $C_L = 50\text{ pF}$ | - | 4.5 | 8.7 | 1.0 | 9.5 | 1.0 | 11.0 | ns |
| t_{en} | enable time | \overline{OE} to An; \overline{OE} to Bn; signal name DIR; see Figure 6 | [3] | | | | | | | |
| | | $C_L = 15\text{ pF}$ | - | 5.0 | 13.8 | 1.0 | 15.0 | 1.0 | 17.5 | ns |
| | | $C_L = 50\text{ pF}$ | - | 6.0 | 14.8 | 1.0 | 16.0 | 1.0 | 18.5 | ns |

Table 7. Dynamic characteristics ...continued

Voltages are referenced to GND (ground = 0 V); for test circuit see [Figure 7](#).

| Symbol | Parameter | Conditions | 25 °C | | | -40 °C to +85 °C | | -40 °C to +125 °C | | Unit |
|------------------|-------------------------------------|---|-------|--------------------|------|------------------|------|-------------------|------|------|
| | | | Min | Typ ^[1] | Max | Min | Max | Min | Max | |
| t _{dis} | disable time | OE to An; OE to Bn; signal name DIR; see Figure 6 | | | | | | | | |
| | | C _L = 15 pF | - | 5.0 | 14.4 | 1.0 | 15.5 | 1.0 | 18.0 | ns |
| | | C _L = 50 pF | - | 6.0 | 15.4 | 1.0 | 16.5 | 1.0 | 19.5 | ns |
| C _{PD} | power dissipation capacitance | f _i = 1 MHz; V _i = GND to V _{CC} | [5] | - | 15 | - | - | - | - | pF |

[1] Typical values are measured at nominal supply voltage (V_{CC} = 3.3 V and V_{CC} = 5.0 V).

[2] t_{pd} is the same as t_{PLH} and t_{PHL}.

[3] t_{en} is the same as t_{PZL} and t_{PZH}.

[4] t_{dis} is the same as t_{PLZ} and t_{PHZ}.

[5] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).

$$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

f_i = input frequency in MHz;

f_o = output frequency in MHz;

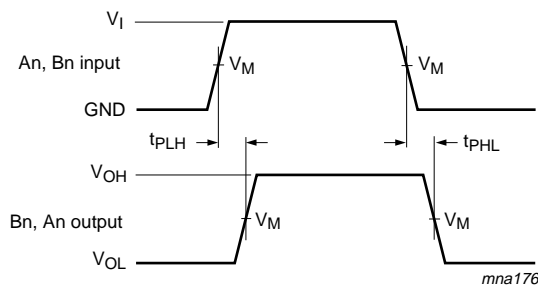
C_L = output load capacitance in pF;

V_{CC} = supply voltage in V;

N = number of inputs switching;

Σ(C_L × V_{CC}² × f_o) = sum of the outputs.

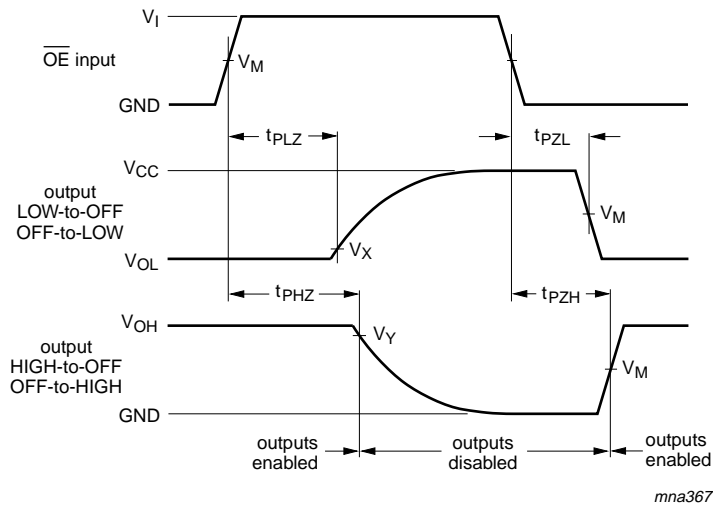
10.1 Waveforms



Measurement points are given in [Table 8](#).

V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Fig 5. Input to output propagation delays

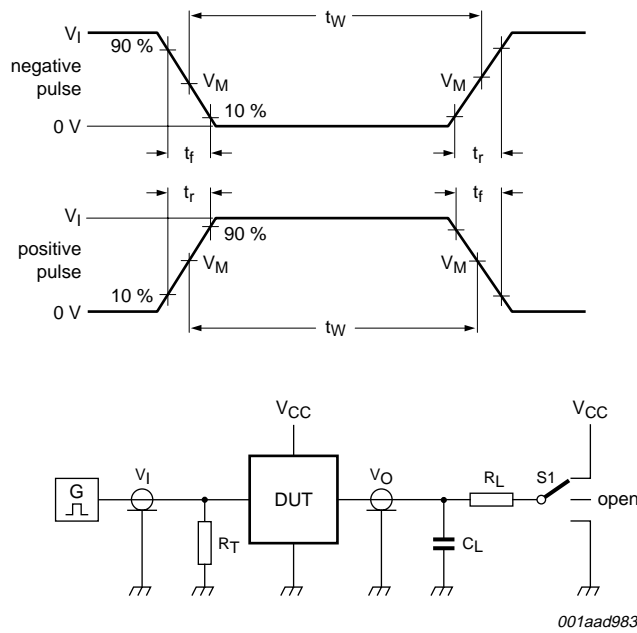


Measurement points are given in [Table 8](#).
 V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Fig 6. Enable and disable times

Table 8. Measurement points

| Type | Input | Output | | |
|-----------|-------------|-------------|------------------|------------------|
| | V_M | V_M | V_X | V_Y |
| 74VHC245 | $0.5V_{CC}$ | $0.5V_{CC}$ | $V_{OL} + 0.3 V$ | $V_{OH} - 0.3 V$ |
| 74VHCT245 | 1.5 V | $0.5V_{CC}$ | $V_{OL} + 0.3 V$ | $V_{OH} - 0.3 V$ |



Test data is given in [Table 9](#).

Definitions test circuit:

R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator.

C_L = Load capacitance including jig and probe capacitance.

R_L = Load resistance.

$S1$ = Test selection switch.

Fig 7. Load circuitry for measuring switching times

Table 9. Test data

| Type | Input | | Load | | S1 position | | |
|-----------|----------|---------------|--------------|--------------|--------------------|--------------------|--------------------|
| | V_I | t_r, t_f | C_L | R_L | t_{PHL}, t_{PLH} | t_{PZH}, t_{PHZ} | t_{PZL}, t_{PLZ} |
| 74VHC245 | V_{CC} | ≤ 3.0 ns | 15 pF, 50 pF | 1 k Ω | open | GND | V_{CC} |
| 74VHCT245 | 3.0 V | ≤ 3.0 ns | 15 pF, 50 pF | 1 k Ω | open | GND | V_{CC} |

11. Package outline

SO20: plastic small outline package; 20 leads; body width 7.5 mm

SOT163-1

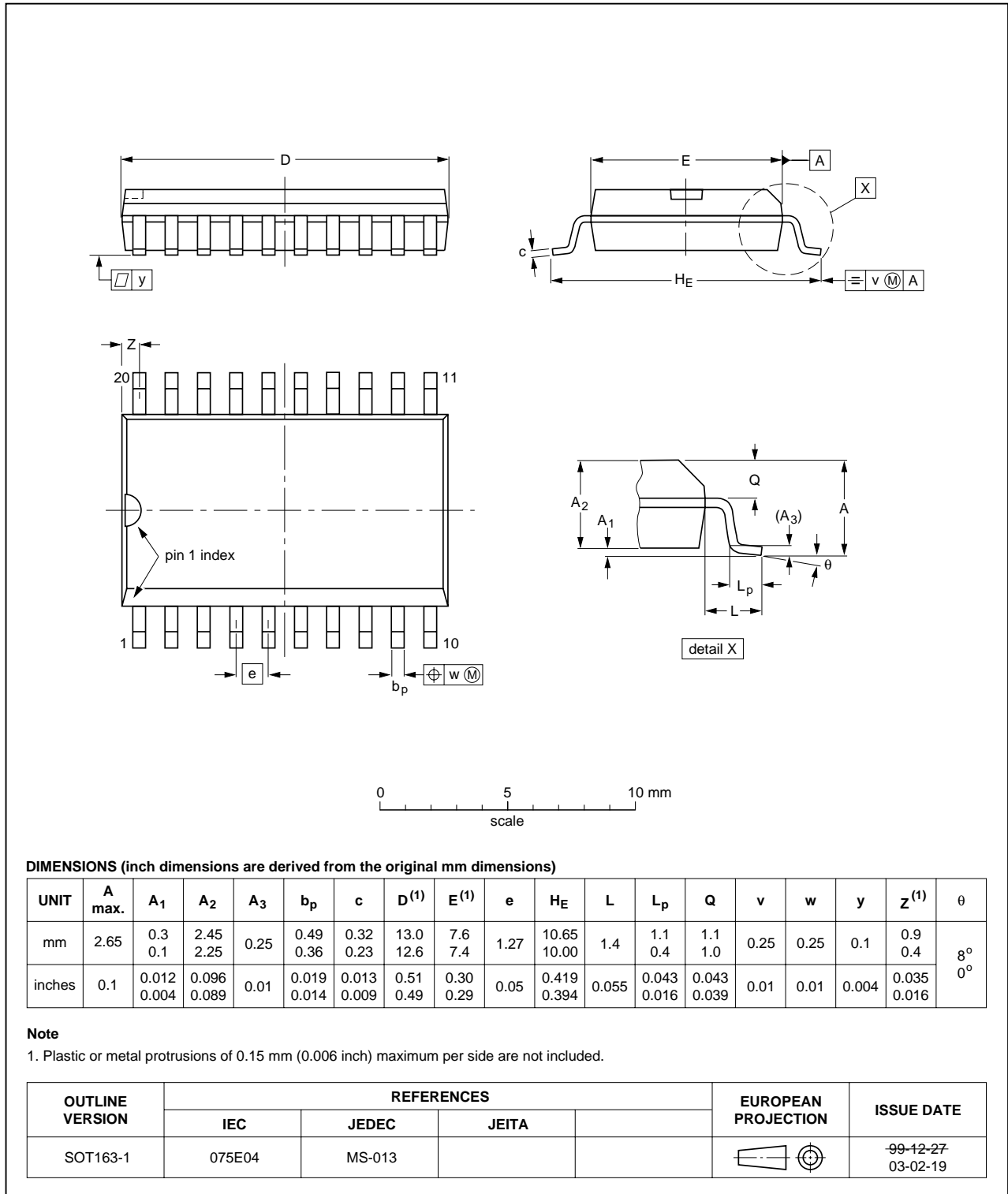


Fig 8. Package outline SOT163-1 (SO20)

TSSOP20: plastic thin shrink small outline package; 20 leads; body width 4.4 mm

SOT360-1

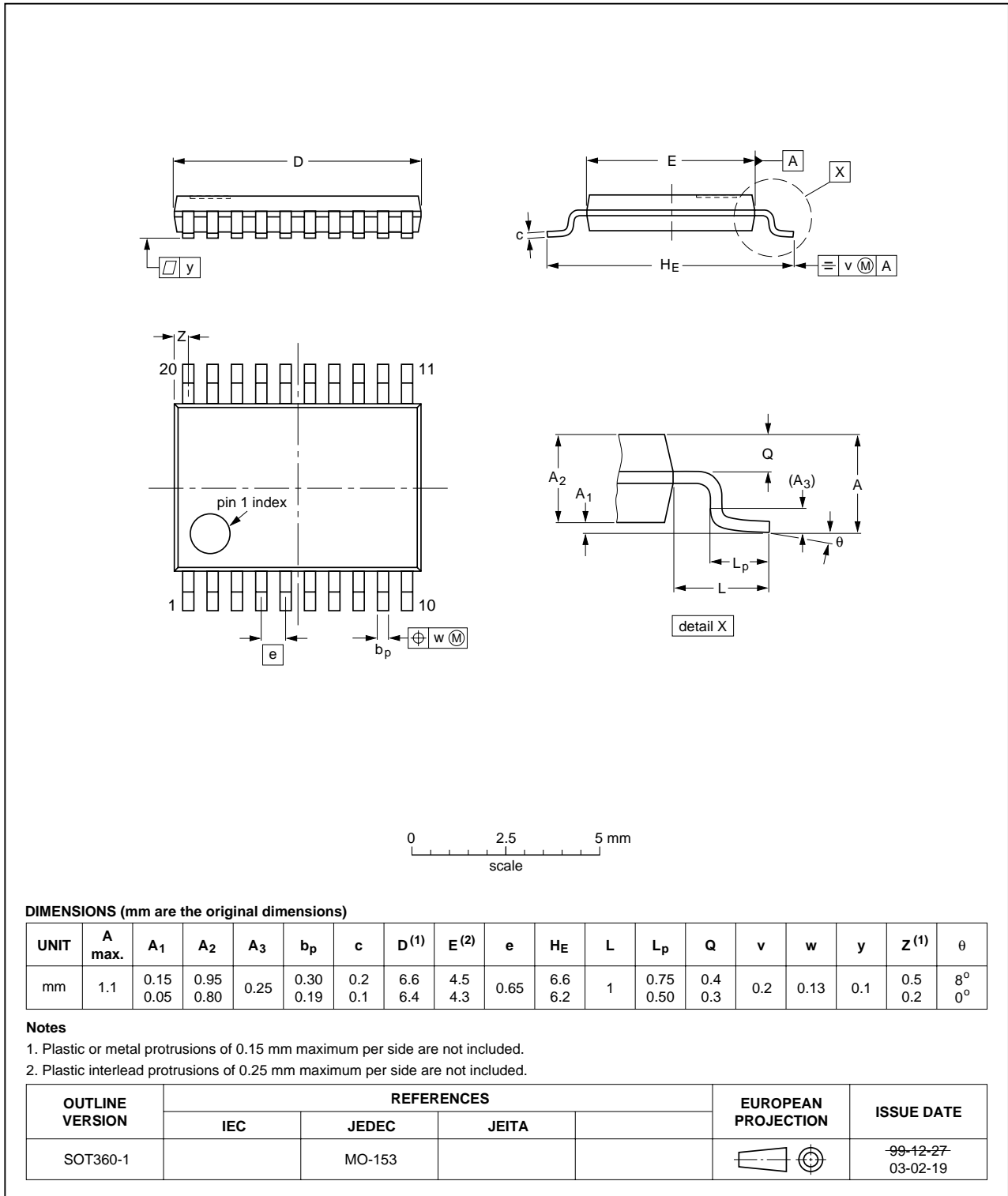


Fig 9. Package outline SOT360-1 (TSSOP20)

DHVQFN20: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 20 terminals; body 2.5 x 4.5 x 0.85 mm

SOT764-1

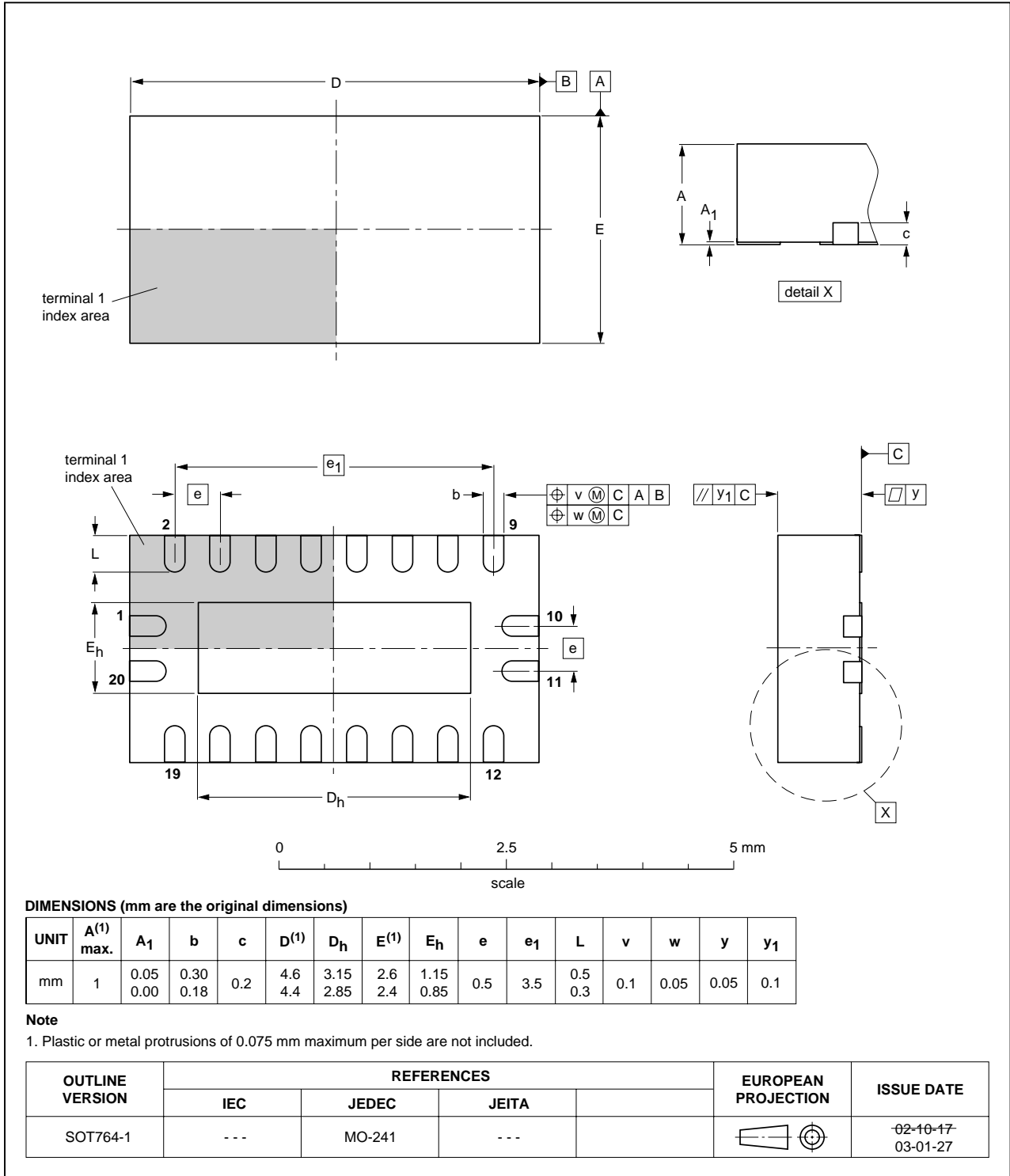


Fig 10. Package outline SOT764-1 (DHVQFN20)

12. Abbreviations

Table 10. Abbreviations

| Acronym | Description |
|---------|---|
| CDM | Charged Device Model |
| CMOS | Complementary Metal-Oxide Semiconductor |
| DUT | Device Under Test |
| ESD | ElectroStatic Discharge |
| HBM | Human Body Model |
| MM | Machine Model |
| TTL | Transistor-Transistor Logic |

13. Revision history

Table 11. Revision history

| Document ID | Release date | Data sheet status | Change notice | Supersedes |
|-----------------|--------------|--------------------|---------------|------------|
| 74VHC_VHCT245_1 | 20090825 | Product data sheet | - | - |

14. Legal information

14.1 Data sheet status

| Document status ^{[1][2]} | Product status ^[3] | Definition |
|-----------------------------------|-------------------------------|---|
| Objective [short] data sheet | Development | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet | Qualification | This document contains data from the preliminary specification. |
| Product [short] data sheet | Production | This document contains the product specification. |

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nexperia.com>.

14.2 Definitions

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