**ALPHA & OMEGA SEMICONDUCTOR**

# AON6718L
## 30V N-Channel MOSFET
## SRFET™

### General Description

SRFET™ AON6718L uses advanced trench technology with a monolithically integrated Schottky diode to provide excellent $R_{DS(ON)}$,and low gate charge. This device is ideally suited for use as a low side switch in CPU core power conversion.

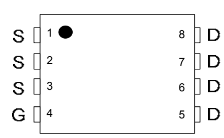
### Features

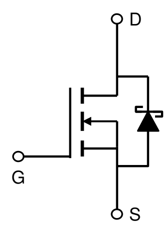
$V_{DS}$ (V) = 30V
$I_D$ = 80A (VGS = 10V)
$R_{DS(ON)}$ < 3.7mΩ ($V_{GS}$ = 10V)
$R_{DS(ON)}$ < 5mΩ ($V_{GS}$ = 4.5V)

100% UIS Tested
100% Rg Tested


DFN5X6

Top View




**SRFET™**
**S**oft **R**ecovery MOS**FET**:
Integrated Schottky Diode

| Absolute Maximum Ratings $T_A$=25°C unless otherwise noted | | | | |
|---|---|---|---|---|
| **Parameter** | | **Symbol** | **Maximum** | **Units** |
| Drain-Source Voltage | | $V_{DS}$ | 30 | V |
| Gate-Source Voltage | | $V_{GS}$ | ±20 | V |
| Continuous Drain Current [G] | $T_C$=25°C | $I_D$ | 80 | A |
| | $T_C$=100°C | | 63 | |
| Pulsed Drain Current [C] | | $I_{DM}$ | 210 | |
| Continuous Drain Current | $T_A$=25°C | $I_{DSM}$ | 18 | A |
| | $T_A$=70°C | | 15 | |
| Avalanche Current [C] | | $I_{AR}$ | 40 | A |
| Repetitive avalanche energy L=0.1mH [C] | | $E_{AR}$ | 80 | mJ |
| Power Dissipation [B] | $T_C$=25°C | $P_D$ | 83 | W |
| | $T_C$=100°C | | 33 | |
| Power Dissipation [A] | $T_A$=25°C | $P_{DSM}$ | 2.1 | W |
| | $T_A$=70°C | | 1.3 | |
| Junction and Storage Temperature Range | | $T_J$, $T_{STG}$ | -55 to 150 | °C |

| Thermal Characteristics | | | | | |
|---|---|---|---|---|---|
| **Parameter** | | **Symbol** | **Typ** | **Max** | **Units** |
| Maximum Junction-to-Ambient [A] | t ≤ 10s | $R_{\theta JA}$ | 14.2 | 17 | °C/W |
| Maximum Junction-to-Ambient [A D] | Steady-State | | 42 | 60 | °C/W |
| Maximum Junction-to-Case | Steady-State | $R_{\theta JC}$ | 1.2 | 1.5 | °C/W |

## Electrical Characteristics ($T_J$=25°C unless otherwise noted)

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **STATIC PARAMETERS** | | | | | | |
| $BV_{DSS}$ | Drain-Source Breakdown Voltage | $I_D$=250µA, $V_{GS}$=0V | 30 | | | V |
| $I_{DSS}$ | Zero Gate Voltage Drain Current | $V_{DS}$=30V, $V_{GS}$=0V | | 0.025 | 0.1 | mA |
| | | $T_J$=125°C | | | 20 | |
| $I_{GSS}$ | Gate-Body leakage current | $V_{DS}$=0V, $V_{GS}$= ±20V | | | 0.1 | µA |
| $V_{GS(th)}$ | Gate Threshold Voltage | $V_{DS}$=$V_{GS}$ $I_D$=250µA | 1.3 | 1.8 | 2.2 | V |
| $I_{D(ON)}$ | On state drain current | $V_{GS}$=10V, $V_{DS}$=5V | 160 | | | A |
| $R_{DS(ON)}$ | Static Drain-Source On-Resistance | $V_{GS}$=10V, $I_D$=20A | | 3.1 | 3.7 | mΩ |
| | | $T_J$=125°C | | 4.3 | 5.2 | |
| | | $V_{GS}$=4.5V, $I_D$=20A | | 4.1 | 5 | mΩ |
| $g_{FS}$ | Forward Transconductance | $V_{DS}$=5V, $I_D$=20A | | 87 | | S |
| $V_{SD}$ | Diode Forward Voltage | $I_S$=1A,$V_{GS}$=0V | | 0.4 | 0.7 | V |
| $I_S$ | Maximum Body-Diode Continuous Current[G] | | | | 40 | A |
| **DYNAMIC PARAMETERS** | | | | | | |
| $C_{iss}$ | Input Capacitance | $V_{GS}$=0V, $V_{DS}$=15V, f=1MHz | 2975 | 3719 | 4463 | pF |
| $C_{oss}$ | Output Capacitance | | 485 | 693 | 900 | pF |
| $C_{rss}$ | Reverse Transfer Capacitance | | 204 | 340 | 476 | pF |
| $R_g$ | Gate resistance | $V_{GS}$=0V, $V_{DS}$=0V, f=1MHz | 0.28 | 0.56 | 0.84 | Ω |
| **SWITCHING PARAMETERS** | | | | | | |
| $Q_g$(10V) | Total Gate Charge | $V_{GS}$=10V, $V_{DS}$=15V, $I_D$=20A | 48 | 60 | 72 | nC |
| $Q_g$(4.5V) | Total Gate Charge | | 20 | 25 | 30 | nC |
| $Q_{gs}$ | Gate Source Charge | | 12 | 15 | 18 | nC |
| $Q_{gd}$ | Gate Drain Charge | | 6 | 10 | 14 | nC |
| $t_{D(on)}$ | Turn-On DelayTime | $V_{GS}$=10V, $V_{DS}$=15V, $R_L$=0.75Ω, $R_{GEN}$=3Ω | | 9.2 | | ns |
| $t_r$ | Turn-On Rise Time | | | 10.7 | | ns |
| $t_{D(off)}$ | Turn-Off DelayTime | | | 40 | | ns |
| $t_f$ | Turn-Off Fall Time | | | 12.5 | | ns |
| $t_{rr}$ | Body Diode Reverse Recovery Time | $I_F$=20A, dI/dt=500A/µs | 10 | 13 | 16 | ns |
| $Q_{rr}$ | Body Diode Reverse Recovery Charge | $I_F$=20A, dI/dt=500A/µs | 21 | 26.5 | 32 | nC |

A. The value of $R_{\theta JA}$ is measured with the device mounted on 1in$^2$ FR-4 board with 2oz. Copper, in a still air environment with $T_A$ =25°C. The Power dissipation $P_{DSM}$ is based on $R_{\theta JA}$ and the maximum allowed junction temperature of 150°C. The value in any given application depends on the user's specific board design.

B. The power dissipation $P_D$ is based on $T_{J(MAX)}$=150°C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.

C. Repetitive rating, pulse width limited by junction temperature $T_{J(MAX)}$=150°C. Ratings are based on low frequency and duty cycles to keep initial $T_J$ =25°C.

D. The $R_{\theta JA}$ is the sum of the thermal impedence from junction to case $R_{\theta JC}$ and case to ambient.

E. The static characteristics in Figures 1 to 6 are obtained using <300µs pulses, duty cycle 0.5% max.

F. These curves are based on the junction-to-case thermal impedence which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of $T_{J(MAX)}$=150°C. The SOA curve provides a single pulse rating.

G. The maximum current rating is limited by bond-wires.

H. These tests are performed with the device mounted on 1 in$^2$ FR-4 board with 2oz. Copper, in a still air environment with $T_A$=25°C.

Rev2: Oct-09

## TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

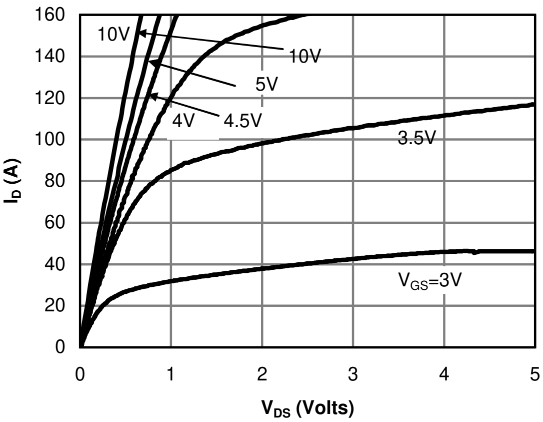



Fig 1: On-Region Characteristics (Note E)

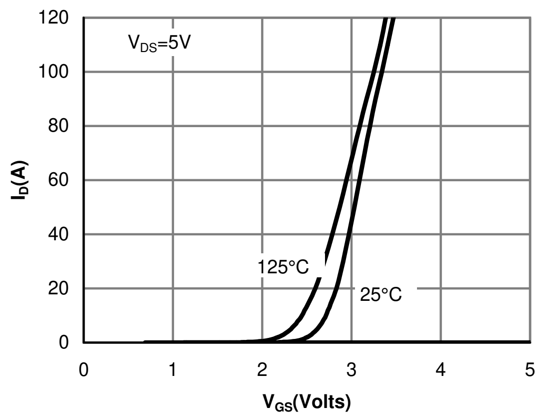



Figure 2: Transfer Characteristics (Note E)

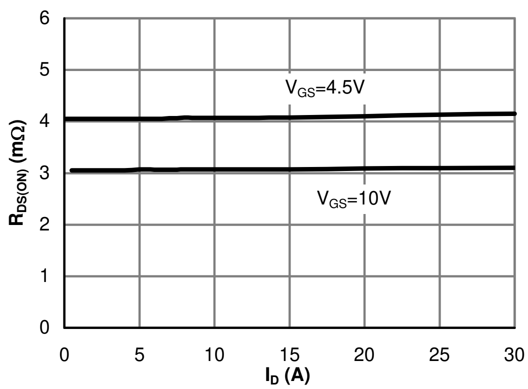



Figure 3: On-Resistance vs. Drain Current and Gate Voltage (Note E)

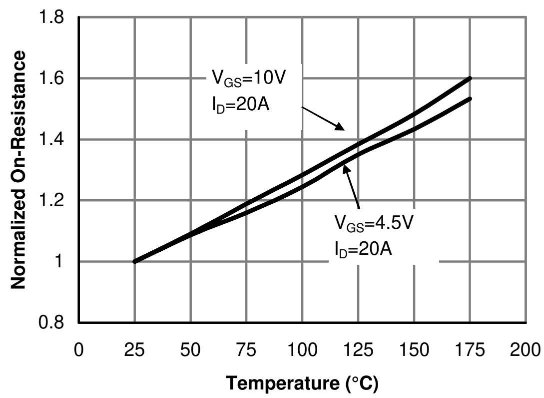



Figure 4: On-Resistance vs. Junction Temperature (Note E)

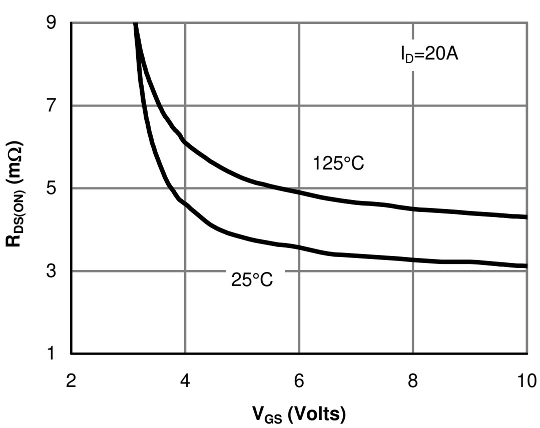



Figure 5: On-Resistance vs. Gate-Source Voltage (Note E)

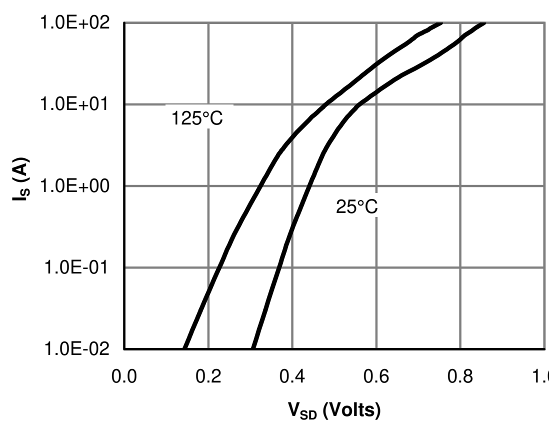



Figure 6: Body-Diode Characteristics (Note E)

## TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

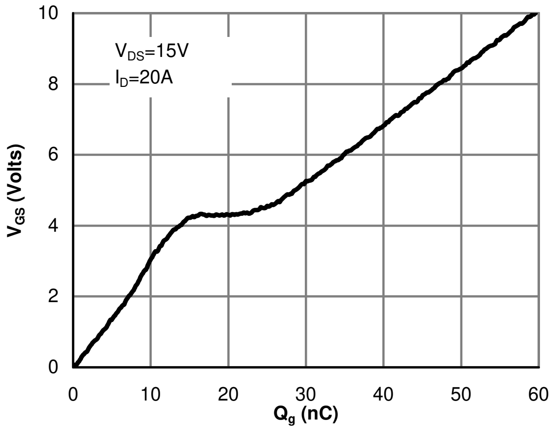



Figure 7: Gate-Charge Characteristics

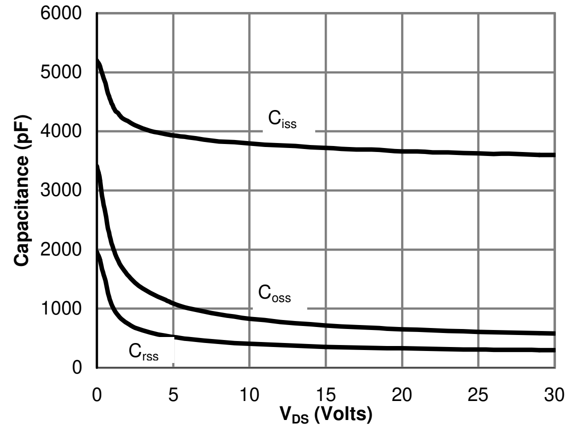



Figure 8: Capacitance Characteristics

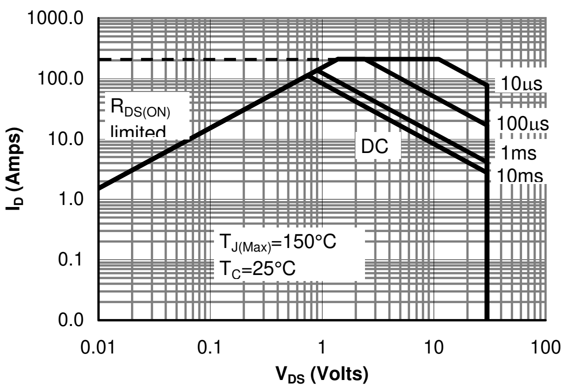



Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

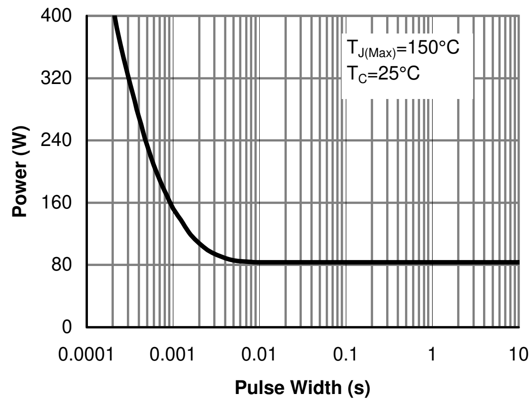



Figure 10: Single Pulse Power Rating Junction-to-Case (Note F)

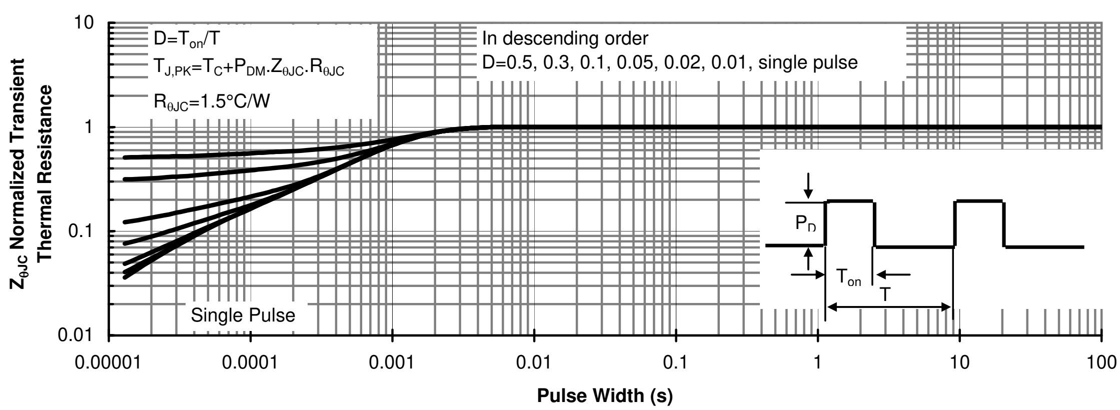



Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)

## TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

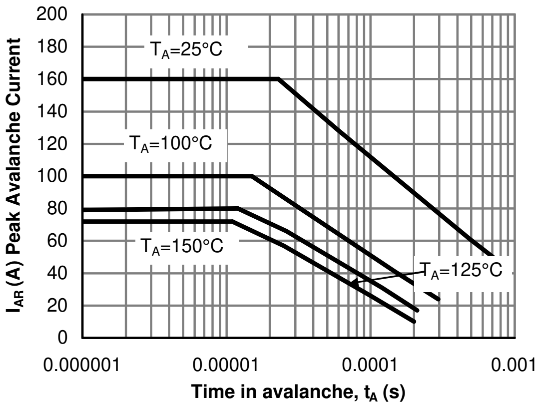



Figure 12: Single Pulse Avalanche capability (Note C)

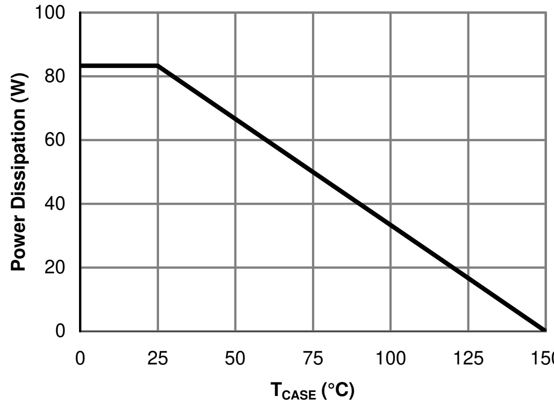



Figure 13: Power De-rating (Note F)

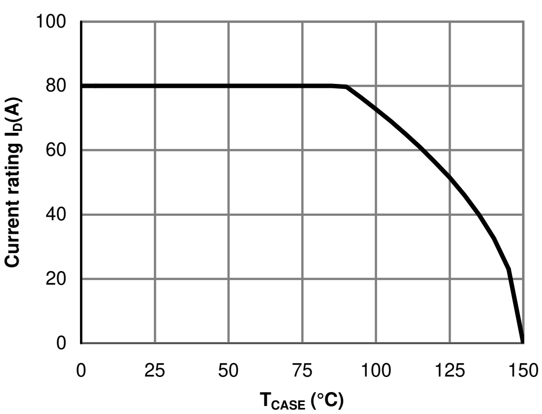



Figure 14: Current De-rating (Note F)

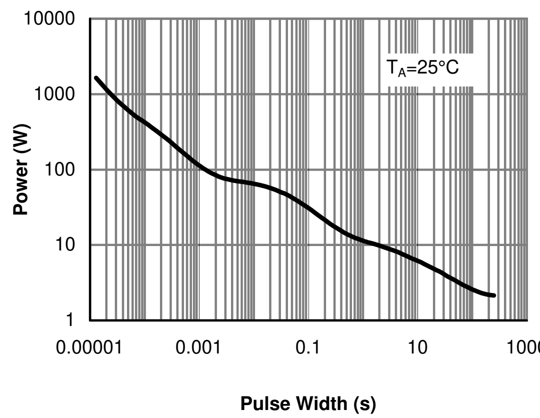



Figure 15: Single Pulse Power Rating Junction-to-Ambient (Note H)

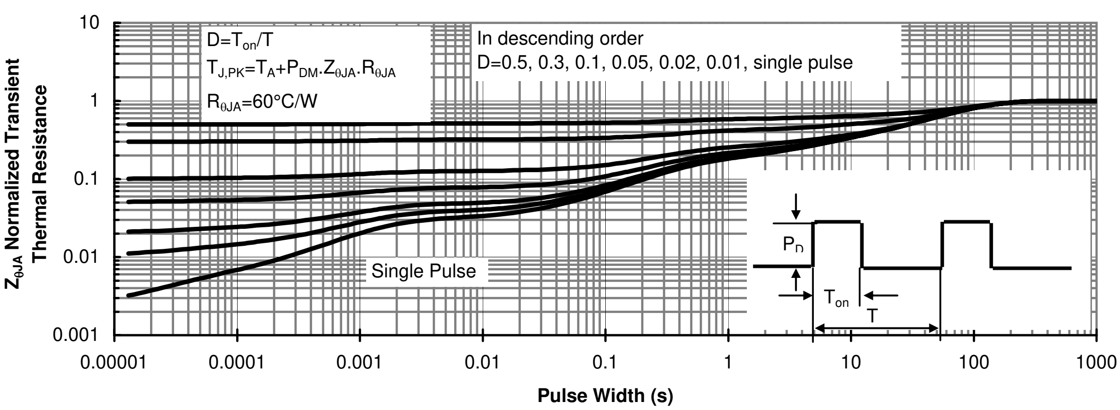



Figure 16: Normalized Maximum Transient Thermal Impedance (Note H)

## TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

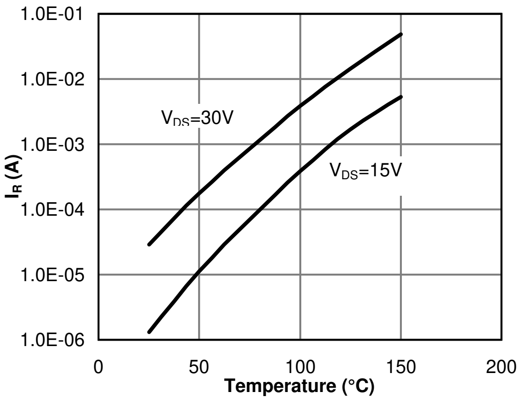



**Figure 17: Diode Reverse Leakage Current vs. Junction Temperature**

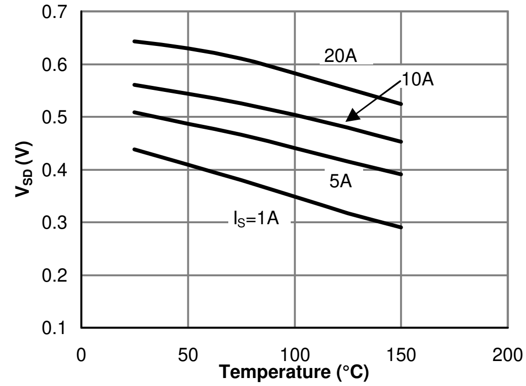



**Figure 18: Diode Forward voltage vs. Junction Temperature**

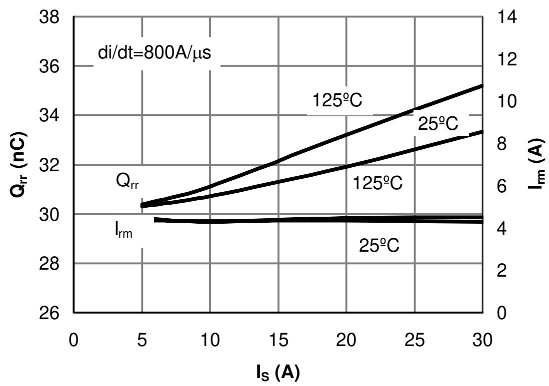



**Figure 19: Diode Reverse Recovery Charge and Peak Current vs. Conduction Current**

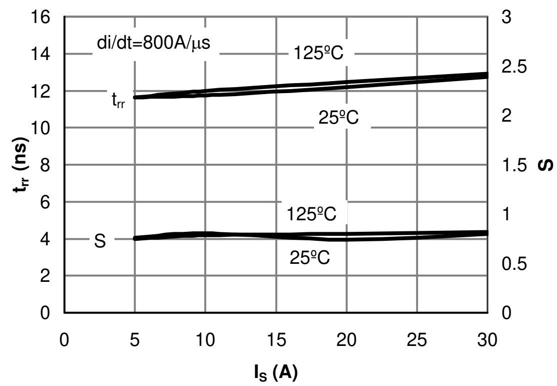



**Figure 20: Diode Reverse Recovery Time and Softness Factor vs. Conduction Current**

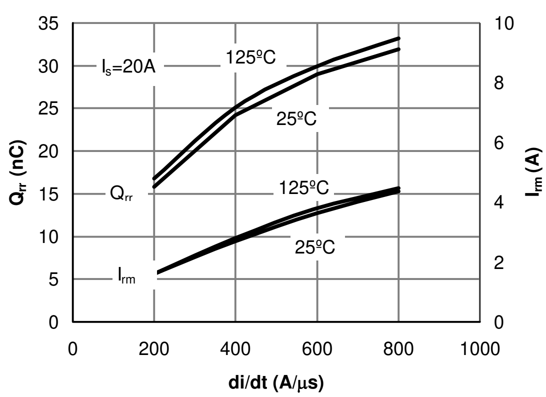



**Figure 21: Diode Reverse Recovery Charge and Peak Current vs. di/dt**

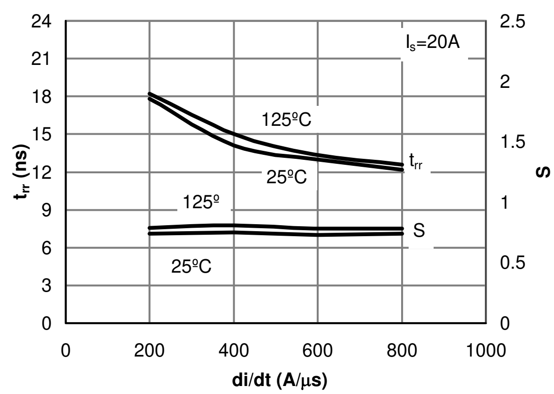
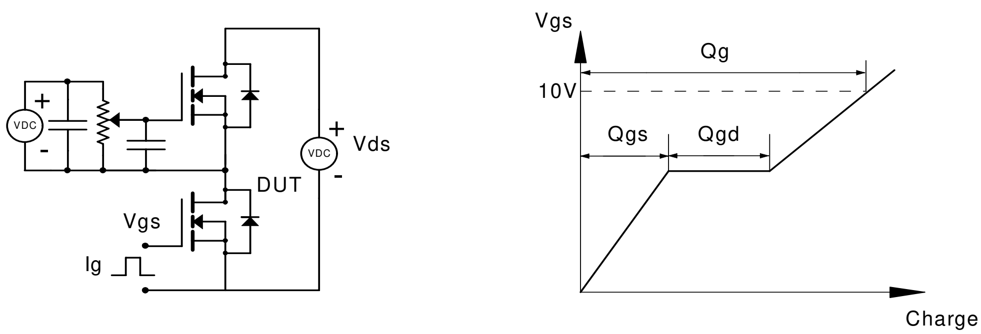
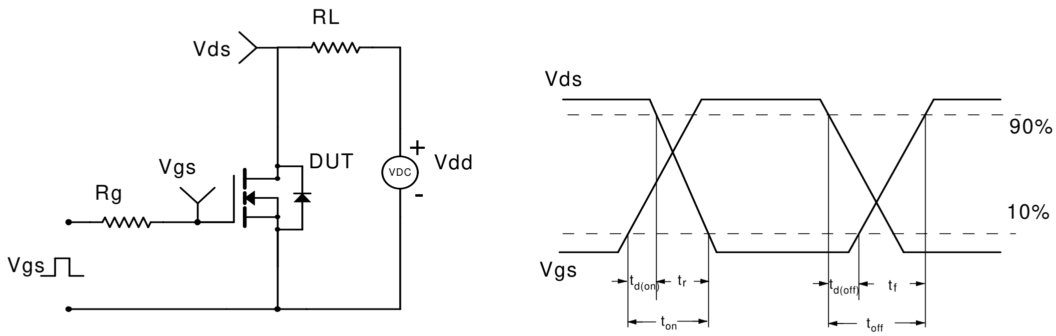



**Figure 22: Diode Reverse Recovery Time and Softness Factor vs. di/dt**

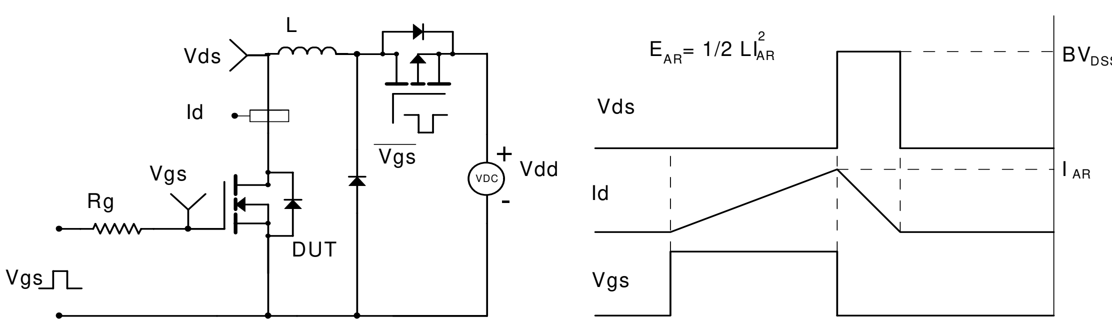
Gate Charge Test Circuit & Waveform




Resistive Switching Test Circuit & Waveforms




Unclamped Inductive Switching (UIS) Test Circuit & Waveforms




Diode Recovery Test Circuit & Waveforms