MOTOROLA

Military 54LS670

4 X 4 Register File With 3-State Outputs

ELECTRICALLY TESTED PER:
MIL-M-38510/31901

The 54LS670 is a high-speed, low-power 4 x 4 Register File organized as four words by four bits. Separate read and write inputs, both address and enable, allow simultaneous read and write operation.

The 3-state outputs make it possible to connect up to 128 outputs to increase the word capacity up to 512 words. Any number of these devices can be operated in parallel to generate an n-bit length.

- Simultaneous Read/Write Operation
- Expandable to 512 Words of n-Bits
- Typical Access Time of 20 ns
- 3-State Outputs for Expansion
- Typical Power Dissipation of 125 mW

AVAILABLE AS:

1) JAN: JM38510/31901BXA
2) SMD: 7704201
3) 883: 54LS670/BXAJC

X = CASE OUTLINE AS FOLLOWS:
PACKAGE: CERDIP: E
CERFLAT: F
LCC: 2

THE LETTER "M" APPEARS BEFORE THE / ON LCC.

WRITE FUNCTION TABLE (SEE NOTES A, B, AND C)

Write Inputs			Word			
W_B	W_A	$\overline{E}_W$	0	1	2	3
L	L	L	Q = D	Q_0	Q_0	Q_0
L	H	L	Q_0	Q = D	Q_0	Q_0
H	L	L	Q_0	Q_0	Q = D	Q_0
H	H	L	Q_0	Q_0	Q_0	Q = D
X	X	H	Q_0	Q_0	Q_0	Q_0

NOTES:
A. H = high level, L = low level, X = irrelevant.
B. (Q = D) = The four selected internal flip-flop outputs will assume the states applied to the four external data inputs.
C. Q_0 = the level of Q before the indicated input conditions were established.
D. W0B1 = The first bit of word 0, etc.

READ FUNCTION TABLE (SEE NOTES A AND D)

Read Inputs			Outputs			
R_B	R_A	$\overline{E}_R$	Q_1	Q_2	Q_3	Q_4
L	L	L	W0B1	W0B2	W0B3	W0B4
L	H	L	W1B1	W1B2	W1B3	W1B4
H	L	L	W2B1	W2B2	W2B3	W2B4
H	H	L	W3B1	W3B2	W3B3	W3B4
X	X	H	H	H	H	H

NOTES:
A. H = high level, L = low level, X = irrelevant.
B. (Q = D) = The four selected internal flip-flop outputs will assume the states applied to the four external data inputs.
C. Q_0 = the level of Q before the indicated input conditions were established.
D. W0B1 = The first bit of word 0, etc.

PIN ASSIGNMENTS

FUNCT.	DIL 620-09	FLATS 650-05	LCC 756A-02	BURN-IN (COND. A)
D_2	1	1	2	V_{CC}
D_3	2	2	3	V_{CC}
D_4	3	3	4	V_{CC}
R_B	4	4	5	V_{CC}
R_A	5	5	7	V_{CC}
Q_4	6	6	8	V_{CC}
Q_3	7	7	9	V_{CC}
GND	8	8	10	GND
Q_2	9	9	12	V_{CC}
Q_1	10	10	13	V_{CC}
$\overline{E}_R$	11	11	14	V_{CC}
$\overline{E}_W$	12	12	15	V_{CC}
W_B	13	13	17	V_{CC}
W_A	14	14	18	V_{CC}
D_1	15	15	19	V_{CC}
V_{CC}	16	16	20	V_{CC}

BURN-IN CONDITIONS:
V_{CC} = 5.0 V MIN/6.0 V MAX

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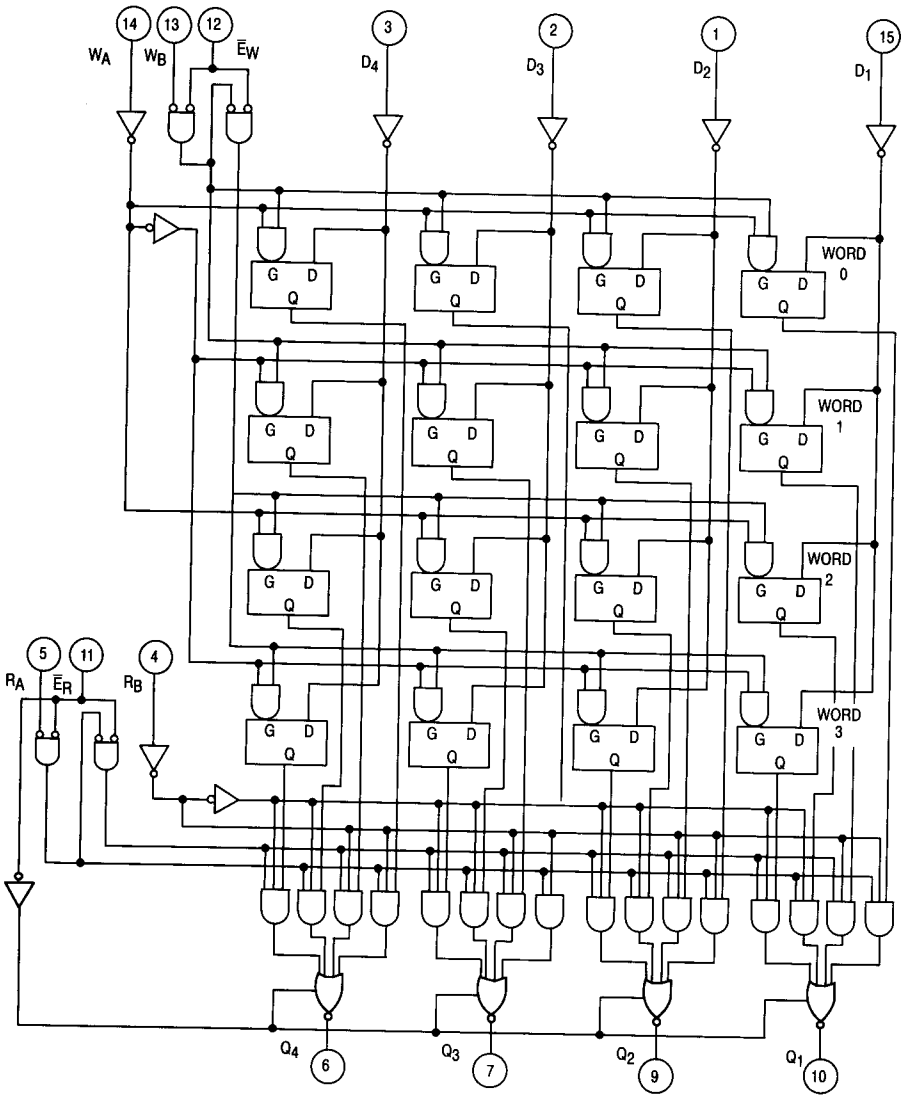
LOGIC DIAGRAM



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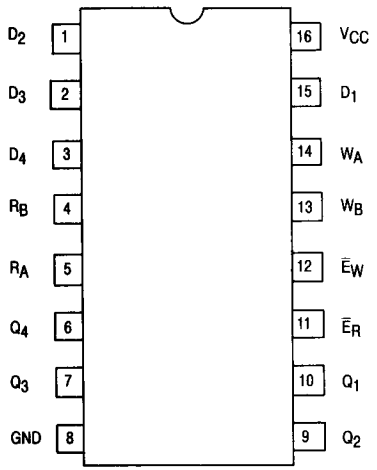
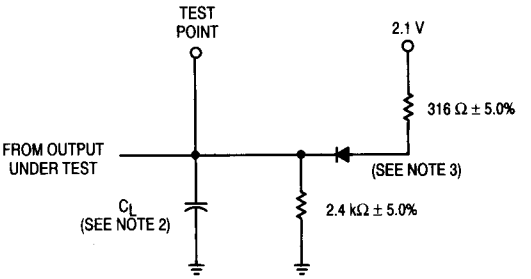
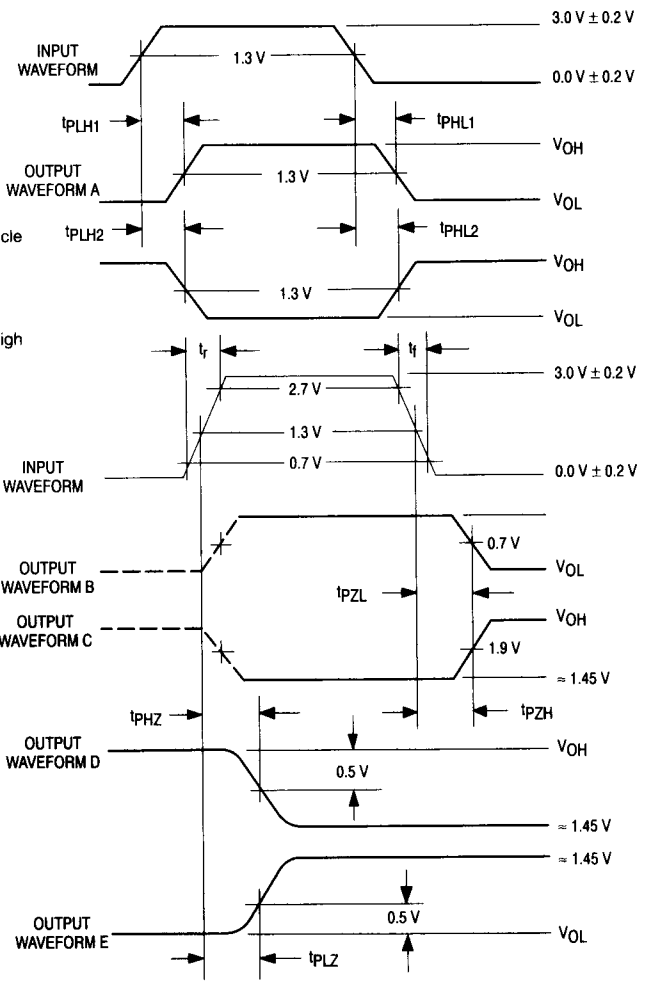
CONNECTION DIAGRAM



AC TEST CIRCUIT



WAVEFORMS



NOTES:

1. The input pulse has the following characteristics: PRR ≤ 1.0 MHz, t_r ≤ 15 ns, and t_f ≤ 6.0 ns; duty cycle = 50% ± 15%.
2. CL = 50 pF ± 10%, including scope probe and jig capacitance.
3. All diodes are 1N3064 and 1N916.
4. Terminal conditions (pins not designated may be high ≥ 2.0 V, low ≤ 0.7 V, or open)
5. Voltage measurements are made with respect to network ground terminal.

SWITCH POSITIONS

Symbol	SW1	SW2
t_{PZH}	Open	Closed
t_{PZL}	Closed	Open
t_{PLZ}	Closed	Closed
t_{PHZ}	Closed	Closed

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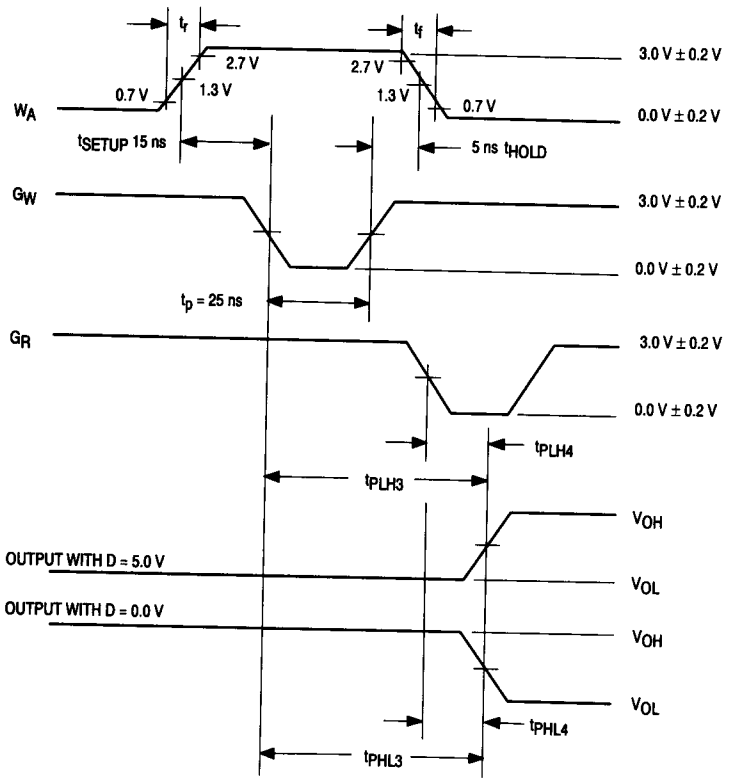
WAVEFORMS


t_r
t_f
2.7 V
2.7 V
0.7 V
1.3 V
1.3 V
0.7 V
W_A
3.0 V ± 0.2 V
0.0 V ± 0.2 V
t_{SETUP} 15 ns
5 ns t_{HOLD}
G_W
3.0 V ± 0.2 V
0.0 V ± 0.2 V
t_p = 25 ns
G_R
3.0 V ± 0.2 V
0.0 V ± 0.2 V
t_{PLH4}
t_{PLH3}
V_{OH}
OUTPUT WITH D = 5.0 V
V_{OL}
OUTPUT WITH D = 0.0 V
V_{OH}
V_{OL}
t_{PHL4}
t_{PHL3}

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Symbol	Parameter	Limits						Unit	Test Condition (Unless Otherwise Specified)
		+ 25°C		+ 125°C		− 55°C			
	Static Parameters:	Subgroup 1		Subgroup 2		Subgroup 3			
		Min	Max	Min	Max	Min	Max		
V_{OH}	Logical "1" Output Voltage	2.4		2.4		2.4		V	V_{CC} = 4.5 V, I_{OH} = − 1.0 mA, V_{IH} = 2.0 V, other inputs = 0.7 V.
V_{OL}	Logical "0" Output Voltage		0.4		0.4		0.4	V	V_{CC} = 4.5 V, I_{OL} = 4.0 mA, V_{IL} = 0.7 V.
V_{IC}	Input Clamping Voltage		− 1.5					V	V_{CC} = 4.5 V, I_{IN} = − 18 mA, other inputs are open.
I_{IL1}	Logical "0" Input Current	− 135	− 370	− 135	− 370	− 135	− 370	µA	V_{CC} = 5.5 V, V_{IN} = 0.4 V, other inputs are open.
I_{IL2}	Logical "0" Input Current	− 0.48	− 1.2	− 0.48	− 1.2	− 0.48	− 1.2	mA	V_{CC} = 5.5 V, $V_{IN(ER)}$ = 0.4 V, other inputs are open.
I_{IL3}	Logical "0" Input Current	− 0.32	− 0.8	− 0.32	− 0.8	− 0.32	− 0.8	mA	V_{CC} = 5.5 V, $V_{IN(RA)}$ = 0.4 V, other inputs are open.
I_{IL4}	Logical "0" Input Current	− 150	− 380	− 150	− 380	− 150	− 380	µA	V_{CC} = 5.5 V, $V_{IN(EW)}$ = 0.4 V, other inputs are open.
I_{IH1}	Logical "1" Input Current		20		20		20	µA	V_{CC} = 5.5 V, V_{IH} = 2.7 V, other inputs are open.
I_{IHH1}	Logical "1" Input Current		100		100		100	µA	V_{CC} = 5.5 V, V_{IHH} = 5.5 V, other inputs are open.
I_{IH2}	Logical "1" Input Current		40		40		40	µA	V_{CC} = 5.5 V, $V_{IH(EW)}$ = 2.7 V, other inputs are open.
I_{IHH2}	Logical "1" Input Current		300		300		300	µA	V_{CC} = 5.5 V, $V_{IHH(ER)}$ = 5.5 V, other inputs are open.
I_{IH3}	Logical "1" Input Current		60		60		60	µA	V_{CC} = 5.5 V, $V_{IH(ER)}$ = 2.7 V, other inputs are open.
I_{IHH3}	Logical "1" Input Current		200		200		200	µA	V_{CC} = 5.5 V, $V_{IHH(EW)}$ = 5.5 V, other inputs are open.
I_{OS}	Output Short Circuit Current	− 30	− 130	− 30	− 130	− 30	− 130	mA	V_{CC} = 5.5 V, V_{IN} = 5.5 V, other inputs are GND, V_{OUT} = GND.
I_{CC}	Power Supply Current Off		50		50		50	mA	V_{CC} = 5.5 V, V_{IN} = 4.5 V, other inputs are GND.
I_{OZH}	Output Off Current High		20		20		20	µA	V_{CC} = 5.5 V, V_{IN} = 2.0 V, other inputs = 0.7 V, V_{OUT} = 2.7 V.
I_{OZL}	Output Off Current Low		− 20		− 20		− 20	µA	V_{CC} = 5.5 V, V_{IN} = 2.0 V, other inputs = 0.7 V, V_{OUT} = 0.4 V.
V_{IH}	Logical "1" Input Voltage	2.0		2.0		2.0		V	V_{CC} = 4.5 V.
V_{IL}	Logical "0" Input Voltage		0.7		0.7		0.7	V	V_{CC} = 4.5 V.
	Functional Tests	Subgroup 7		Subgroup 8A		Subgroup 8B			per Truth Table with V_{CC} = 5.0 V, V_{INL} = 0.4 V, and V_{INH} = 2.4 V.

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Symbol	Parameter	Limits						Unit	Test Condition (Unless Otherwise Specified)
	Switching Parameters:	+ 25°C		+ 125°C		− 55°C			
		Subgroup 9		Subgroup 10		Subgroup 11			
		Min	Max	Min	Max	Min	Max		
t_{PHL1} t_{PHL1}	Propagation Delay D to Q_n	2.0 —	45 40	2.0 —	58 53	2.0 —	58 53	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 316 Ω V_{CC} = 5.0 V, C_L = 45 pF.
t_{PLH1} t_{PLH1}	Propagation Delay D to Q_n	2.0 —	50 45	2.0 —	65 60	2.0 —	65 60	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 316 Ω V_{CC} = 5.0 V, C_L = 45 pF.
t_{PHL2} t_{PHL2}	Propagation Delay R_A or R_B to Q_n	2.0 —	50 45	2.0 —	65 60	2.0 —	65 60	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 316 Ω V_{CC} = 5.0 V, C_L = 45 pF.
t_{PLH2} t_{PLH2}	Propagation Delay R_A or R_B to Q_n	2.0 —	45 40	2.0 —	58 53	2.0 —	58 53	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 316 Ω V_{CC} = 5.0 V, C_L = 45 pF.
t_{PHL3} t_{PHL3}	Propagation Delay E_W to Q_n	2.0 —	55 50	2.0 —	72 67	2.0 —	72 67	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 316 Ω V_{CC} = 5.0 V, C_L = 45 pF.
t_{PLH3} t_{PLH3}	Propagation Delay E_W to Q_n	2.0 —	50 45	2.0 —	65 60	2.0 —	65 60	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 316 Ω V_{CC} = 5.0 V, C_L = 45 pF.
t_{PHZ} t_{PHZ}	Propagation Delay Output Disable Time	2.0 —	55 50	2.0 —	72 67	2.0 —	72 67	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 316 Ω V_{CC} = 5.0 V, C_L = 5.0 pF.
t_{PLZ} t_{PLZ}	Propagation Delay Output Disable Time	2.0 —	40 35	2.0 —	52 48	2.0 —	52 48	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 316 Ω V_{CC} = 5.0 V, C_L = 5.0 pF.
t_{PZH} t_{PZH}	Propagation Delay Output Enable Time	2.0 —	40 35	2.0 —	52 48	2.0 —	52 48	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 316 Ω V_{CC} = 5.0 V, C_L = 45 pF.
t_{PZL} t_{PZL}	Propagation Delay Output Enable Time	2.0 —	45 40	2.0 —	58 53	2.0 —	58 53	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 316 Ω V_{CC} = 5.0 V, C_L = 45 pF.