FemtoClock® Crystal-to-LVDS Clock Generator

844008I-46

DATA SHEET

General Description

The 844008I-46 is a 10Gb Ethernet Clock Generator and a member of the HiPerClocks™ family of high performance devices from IDT. The 844008I-46 can synthesize 156.25MHz or 100MHz with a 25MHz crystal. It has a total of 8 LVDS outputs. The 844008I-46 has excellent phase jitter performance and is packaged in a 32 Lead VFQFN package, making it ideal for use in systems with limited board space.

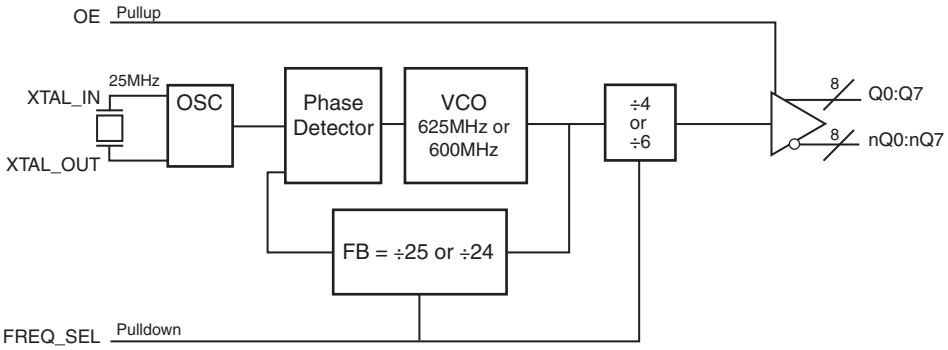
Features

- Eight differential LVDS outputs
- Crystal oscillator interface designed for 18pF parallel resonant crystals
- Supports the following output frequencies: 156.25MHz or 100MHz
- VCO frequency: 625MHz or 600MHz
- RMS phase jitter @ 156.25MHz, using a 25MHz crystal (1.875MHz - 20MHz): 0.45ps (typical)
- Full 2.5V supply mode
- -40°C to 85°C ambient operating temperature
- Available in lead-free (RoHS 6) packages
- For functional replacement part use 8T49N285

Frequency Select Function Table

Input					
XTAL Frequency (MHz)	FREQ_SEL	FB Divider	Output Divider	VCO (MHz)	Output Frequency (MHz)
25	0	÷25	÷4	625	156.25 (default)
25	1	÷24	÷6	600	100

Block Diagram



Pin Assignment

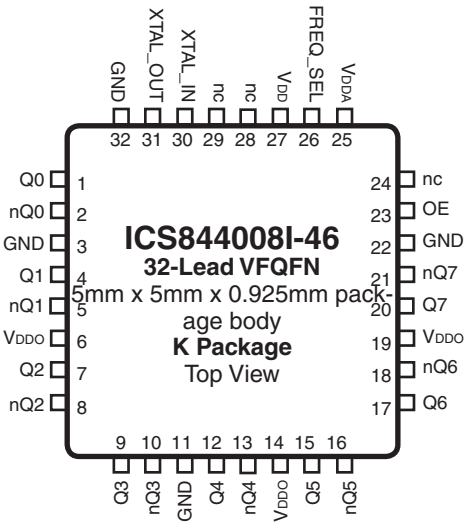


Table 1. Pin Descriptions

Number	Name	Type		Description
1, 2	Q0, nQ0	Output		Differential output pair. LVDS interface levels.
3, 11, 22, 32	GND	Power		Power supply ground.
4, 5	Q1, nQ1	Ouput		Differential output pair. LVDS interface levels.
6, 14, 19	V_{DDO}	Power		Output supply pins.
7, 8	Q2, nQ2	Output		Differential output pair. LVDS interface levels.
9, 10	Q3, nQ3	Output		Differential output pair. LVDS interface levels.
12, 13	Q4, nQ4	Output		Differential output pair. LVDS interface levels.
15, 16	Q5, nQ5	Output		Differential output pair. LVDS interface levels.
17, 18	Q6, nQ6	Output		Differential output pair. LVDS interface levels.
20, 21	Q7, nQ7	Output		Differential output pair. LVDS interface levels.
23	OE	Input	Pullup	Output enable pin. When LOW, outputs are disabled. When HIGH. outputs are enabled. LVCMOS/LVTTL interface levels. See Table 3.
24, 28, 29	nc	Unused		No connect.
25	V_{DDA}	Power		Analog supply pin.
26	FREQ_SEL	Input	Pulldown	Frequency select pin. LVCMOS/LVTTL interface levels.
27	V_{DD}	Power		Core supply pin.
30, 31	XTAL_IN, XTAL_OUT	Input		Parallel resonant crystal interface. XTAL_OUT is the output, XTAL_IN is the input.

NOTE: *Pullup and Pulldown* refer to internal input resistors. See Table 2, Pin Characteristics, for typical values.

Table 2. Pin Characteristics

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance			4		pF
$R_{PULLDOWN}$	Input Pulldown Resistor			51		kΩ
R_{PULLUP}	Input Pullup Resistor			51		kΩ

Table 3. OE Function Table

Inputs OE	Outputs Q[0:7]/nQ[0:7]
1	Enabled (default)
0	Hi-Z

Absolute Maximum Ratings

Supply Voltage, V_{DD}	4.6V
Inputs, V_I	-0.5V to V_{DD} + 0.5V
Outputs, I_O (LVDS)	
Continuous Current	10mA
Surge Current	15mA
Package Thermal Impedance, θ_{JA}	37°C/W (0 mps)
Storage Temperature, T_{STG}	-65°C to 150°C

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Table 4A. Power Supply DC Characteristics, $V_{DD} = V_{DDO}$ = 2.5V±5%, TA = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Core Supply Voltage		2.375	2.5	2.625	V
V_{DDA}	Analog Supply Voltage		V_{DD} – 0.25	2.5	V_{DD}	V
V_{DDO}	Output Supply Voltage		2.375	2.5	2.625	V
I_{DD}	Power Supply Current				60	mA
I_{DDA}	Analog Supply Current				25	mA
I_{DDO}	Output Supply Current				140	mA

Table 4B. LVCMOS / LVTTL DC Characteristics, $V_{DD} = V_{DDO}$ = 2.5V±5%, TA = -40°C to 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage			2		V_{DD} + 0.3	V
V_{IL}	Input Low Voltage			-0.3		0.8	V
I_{IH}	Input High Current	OE	$V_{DD} = V_{IN}$ = 2.625			5	µA
		FREQ_SEL	$V_{DD} = V_{IN}$ = 2.625			150	µA
I_{IL}	Input Low Current	OE	V_{DD} = 2.625V, V_{IN} = 0V	-150			µA
		FREQ_SEL	V_{DD} = 2.625V, V_{IN} = 0V	-5			µA

Table 4C. LVDS DC Characteristics, $V_{DD} = V_{DDO}$ = 2.5V±5%, TA = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OD}	Differential Output Voltage		247	340	454	mV
ΔV_{OD}	V_{OD} Magnitude Change				50	mV
V_{OS}	Offset Voltage		1.10	1.25	1.375	V
ΔV_{OS}	V_{OS} Magnitude Change				50	mV

TABLE 5. CRYSTAL CHARACTERISTICS

Parameter	Test Conditions	Minimum	Typical	Maximum	Units
Mode of Oscillation			Fundamental		
Frequency			25		MHz
Equivalent Series Resistance (ESR)				50	Ω
Shunt Capacitance				7	pF
Drive Level				300	µW

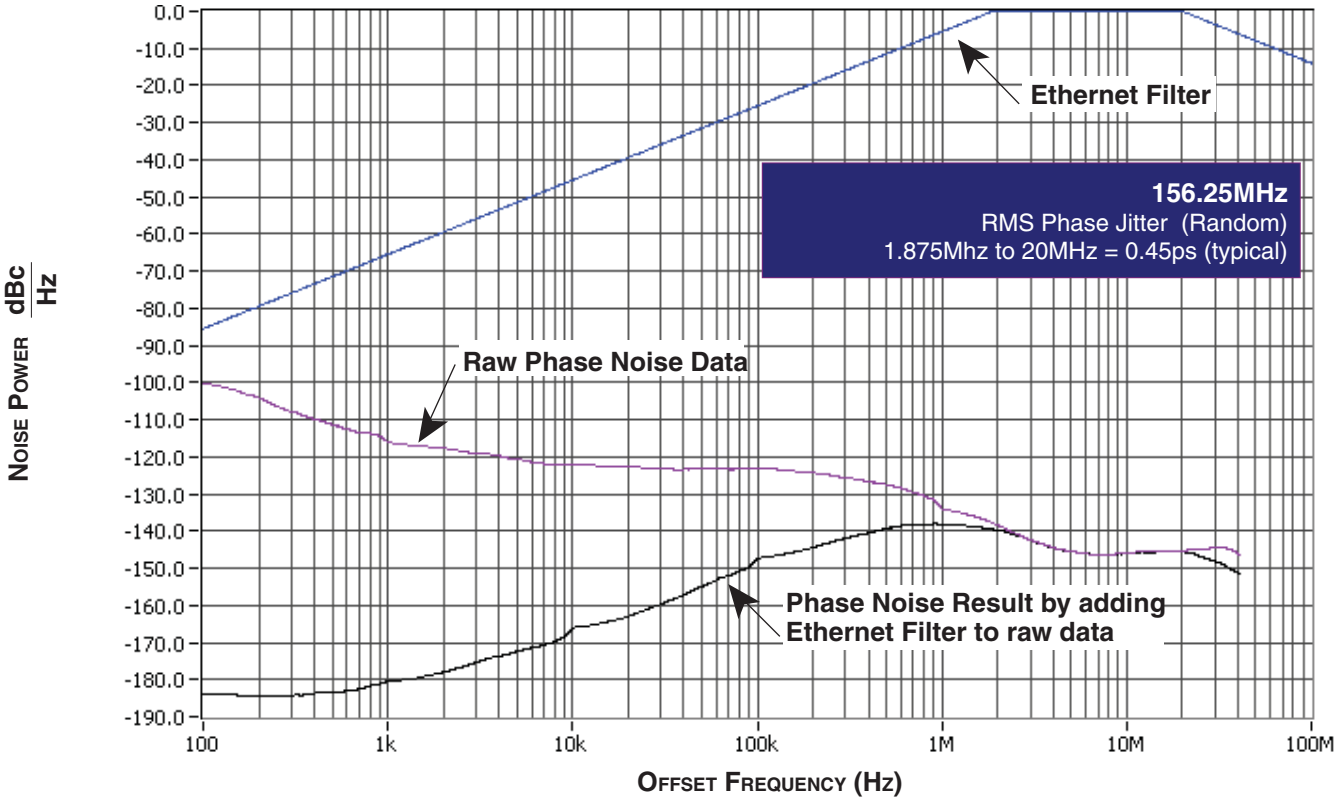
NOTE: Characterized using an 18pF parallel resonant crystal.

TABLE 6. AC CHARACTERISTICS, $V_{DD} = V_{DDO} = 2.5V \pm 5\%$, T_A = -40°C TO 85°C

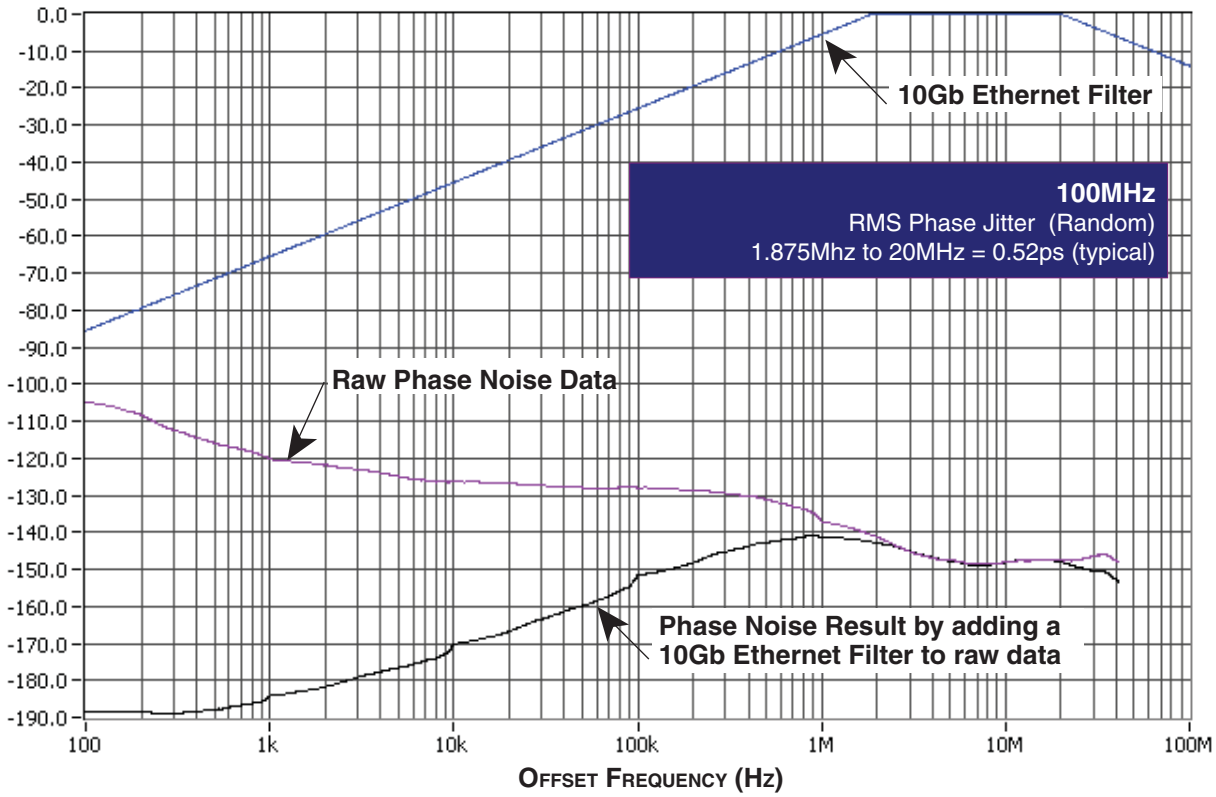
Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{OUT}	Output Frequency	FREQ_SEL = 0		156.25		MHz
		FREQ_SEL = 1		100		MHz
tsk(o)	Output Skew; NOTE 1, 2				75	ps
tjit(cc)	Cycle-to-Cycle Jitter				20	ps
tjit(Ø)	RMS Phase Jitter (Random); NOTE 3	156.25MHz (1.875MHz - 20MHz)		0.45		ps
		100MHz (1.875MHz - 20MHz)		0.52		ps
t_R / t_F	Output Rise/Fall Time	20% to 80%	300		700	ps
odc	Output Duty Cycle		48		52	%

NOTE 1: Defined as skew between outputs at the same supply voltages and with equal load conditions. Measured at the differential cross points.
NOTE 2: This parameter is defined in accordance with JEDEC Standard 65.
NOTE 3: Please refer to the Phase Noise Plot.

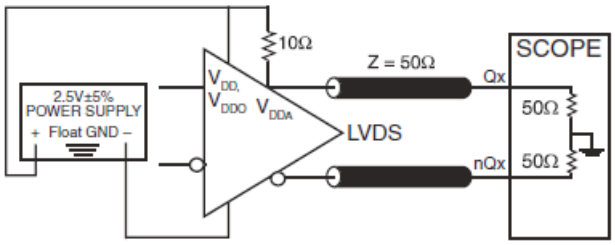
Typical Phase Noise at 156.25MHz



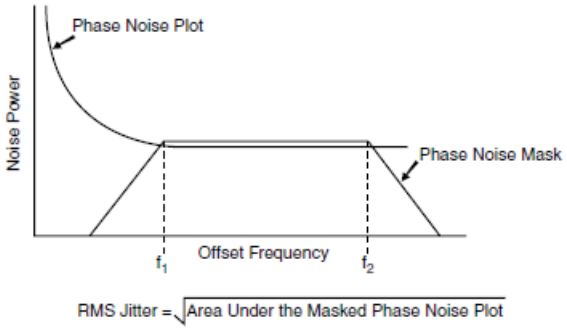
Typical Phase Noise at 100MHz



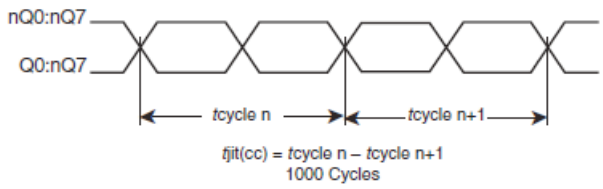
PARAMETER MEASUREMENT INFORMATION



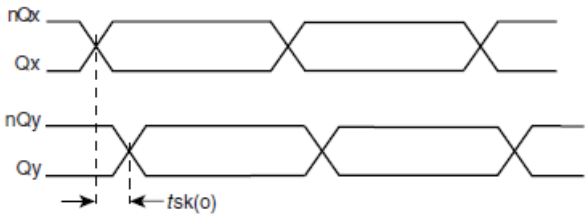
2.5V LVDS OUTPUT LOAD AC TEST CIRCUIT



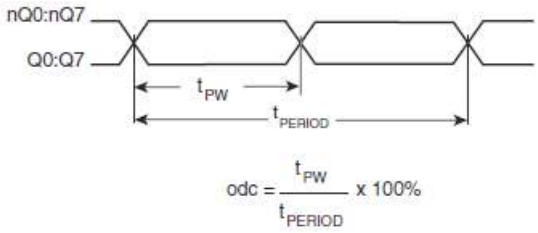
RMS PHASE JITTER



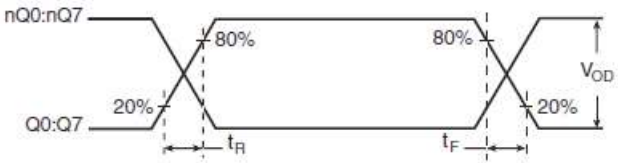
CYCLE-TO-CYCLE JITTER



OUTPUT SKEW

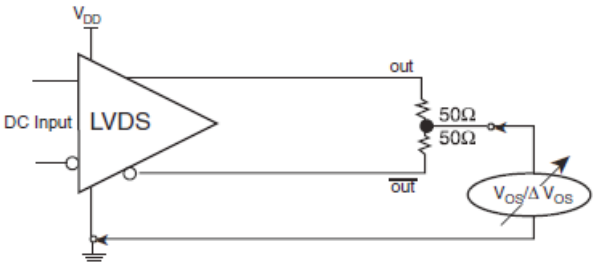


OUTPUT DUTY CYCLE/PULSE WIDTH/PERIOD

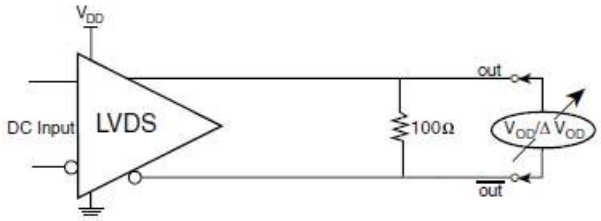


OUTPUT RISE/FALL TIME

PARAMETER MEASUREMENT INFORMATION, CONTINUED



OFFSET VOLTAGE SETUP



DIFFERENTIAL OUTPUT VOLTAGE SETUP

APPLICATION INFORMATION

POWER SUPPLY FILTERING TECHNIQUES

As in any high speed analog circuitry, the power supply pins are vulnerable to random noise. To achieve optimum jitter performance, power supply isolation is required. The 844008I-46 provides separate power supplies to isolate any high switching noise from the outputs to the internal PLL. V_{DD}, V_{DDA}, and V_{DDO} should be individually connected to the power supply plane through vias, and 0.01µF bypass capacitors should be used for each pin. *Figure 1* illustrates this for a generic V_{CC} pin and also shows that V_{DDA} requires that an additional 10Ω resistor along with a 10µF bypass capacitor be connected to the V_{DDA} pin.

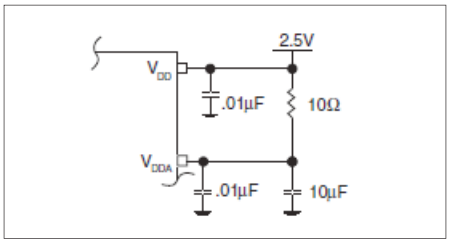


FIGURE 1. POWER SUPPLY FILTERING

Recommendations for Unused Input and Output Pins

Inputs:

LVCMOS Control Pins

All control pins have internal pull-ups or pull-downs; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

Outputs:

LVDS Outputs

All unused LVDS output pairs can be either left floating or terminated with 100Ω across. If they are left floating, there should be no trace attached.

Crystal Input Interface

The 844008I-46 has been characterized with an 18pF parallel resonant crystals. The capacitor values shown in *Figure 2* below were determined using a 25MHz parallel resonant crystal and were chosen to minimize the ppm error.

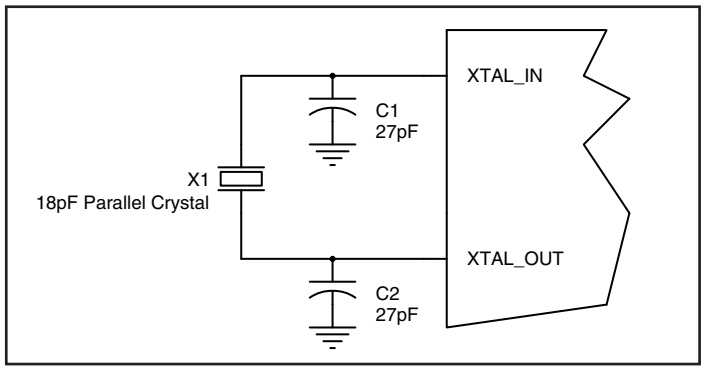


Figure 2. Crystal Input Interface

LVCMOS to XTAL Interface

The XTAL_IN input can accept a single-ended LVCMOS signal through an AC coupling capacitor. A general interface diagram is shown in *Figure 3.* The XTAL_OUT pin can be left floating. The input edge rate can be as slow as 10ns. For LVCMOS inputs, it is recommended that the amplitude be reduced from full swing to half swing in order to prevent signal interference with the power rail and to reduce noise. This configuration requires that the output impedance of the driver (Ro) plus the series resistance (Rs) equals the transmission line impedance. In addition, matched termination at the crystal input will attenuate the signal in half. This can be done in one of two ways. First, R1 and R2 in parallel should equal the transmission line impedance. For most 50Ω applications, R1 and R2 can be 100Ω. This can also be accomplished by removing R1 and making R2 50Ω.

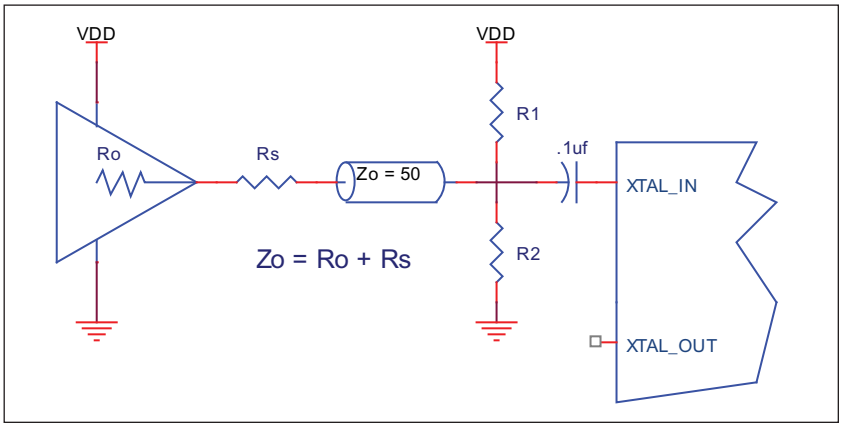


Figure 3. General Diagram for LVCMOS Driver to XTAL Input Interface

VFQFN EPAD Thermal Release Path

In order to maximize both the removal of heat from the package and the electrical performance, a land pattern must be incorporated on the Printed Circuit Board (PCB) within the footprint of the package corresponding to the exposed metal pad or exposed heat slug on the package, as shown in *Figure 4.* The solderable area on the PCB, as defined by the solder mask, should be at least the same size/ shape as the exposed pad/slug area on the package to maximize the thermal/electrical performance. Sufficient clearance should be designed on the PCB between the outer edges of the land pattern and the inner edges of pad pattern for the leads to avoid any shorts.

While the land pattern on the PCB provides a means of heat transfer and electrical grounding from the package to the board through a solder joint, thermal vias are necessary to effectively conduct from the surface of the PCB to the ground plane(s). The land pattern must be connected to ground through these vias. The vias act as "heat pipes". The number of vias (i.e. "heat pipes") are application specific and dependent upon the package power dissipation as well as electrical conductivity requirements. Thus, thermal and electrical analysis and/or testing are recommended to determine the minimum number needed. Maximum thermal and electrical performance is achieved when an array of vias is incorporated in the land pattern. It is recommended to use as many vias connected to ground as possible. It is also recommended that the via diameter should be 12 to 13mils (0.30 to 0.33mm) with 1oz copper via barrel plating. This is desirable to avoid any solder wicking inside the via during the soldering process which may result in voids in solder between the exposed pad/slug and the thermal land. Precautions should be taken to eliminate any solder voids between the exposed heat slug and the land pattern. Note: These recommendations are to be used as a guideline only. For further information, refer to the Application Note on the *Surface Mount Assembly* of Amkor's Thermally/Electrically Enhance Leadfame Base Package, Amkor Technology.

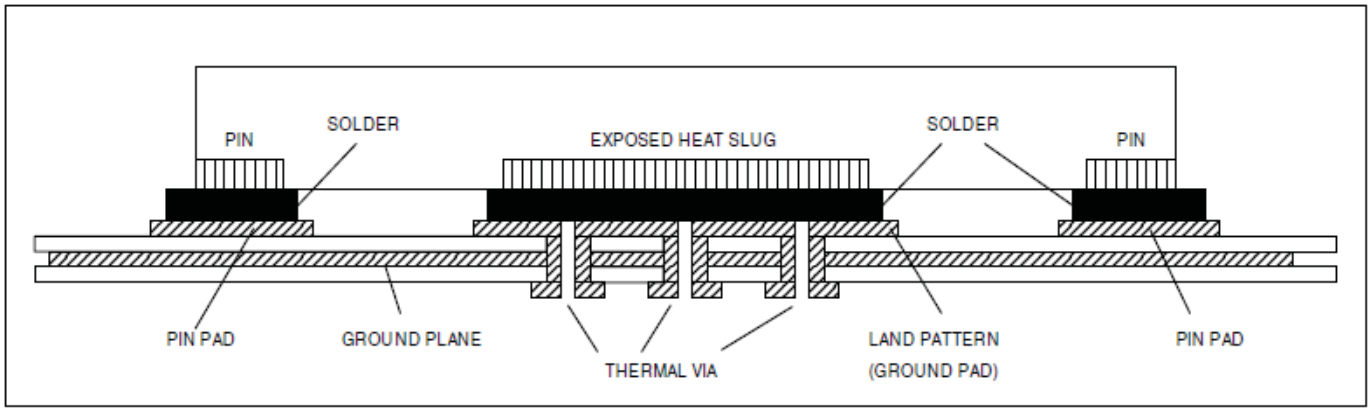


Figure 4. P.C.Assembly for Exposed Pad Thermal Release Path –Side View (Drawing not to Scale)

2.5V LVDS Driver Termination

Figure 5 shows a typical termination for LVDS driver in characteristic impedance of 100Ω differential (50Ω single) transmission line environment.

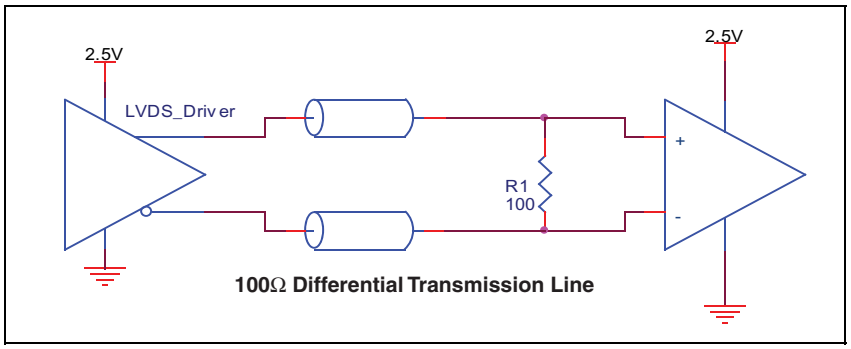


Figure 5. Typical LVDS Driver Termination

SCHEMATIC LAYOUT

Figure 6 shows an example of 844008I-46 application schematic. In this example, the device is operated at $V_{DD} = V_{DDO} = 3.3V$. The 18pF parallel resonant 25MHz crystal is used. The C1 = 27pF and C2 = 27pF are recommended for frequency accuracy. For different board layout, the C1 and C2 may be slightly adjusted for optimizing frequency accuracy. Two examples of LVDS for receiver without built-in termination are shown in this schematic.

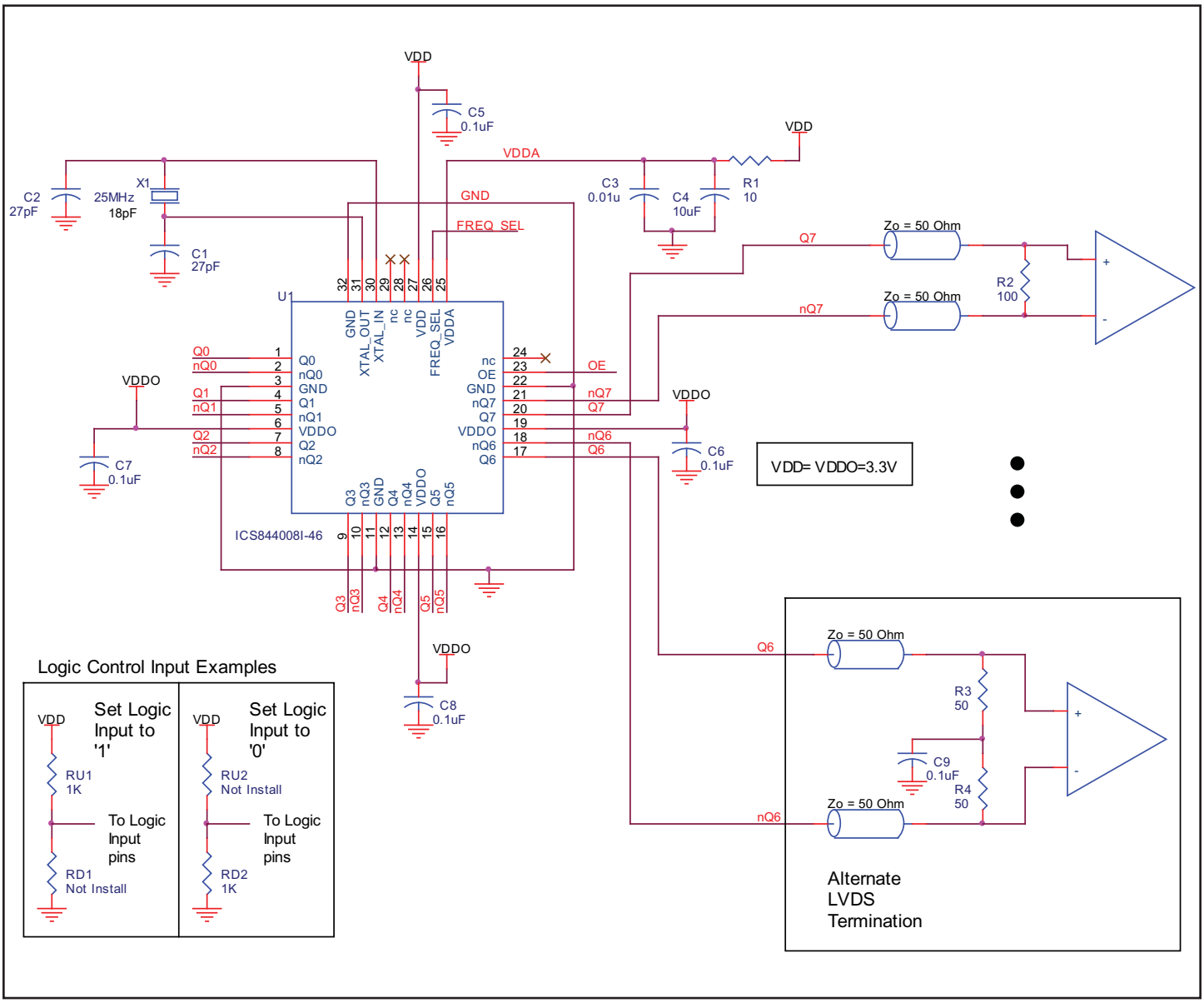


FIGURE 6. 844008I-46 SCHEMATIC LAYOUT

POWER CONSIDERATIONS

This section provides information on power dissipation and junction temperature for the 844008I-46.
Equations and example calculations are also provided.

1. Power Dissipation.
The total power dissipation for the 844008I-46 is the sum of the core power plus the analog power plus the power dissipated in the load(s). The following is the power dissipation for V_{DD} = 2.5V + 5% = 2.625V, which gives worst case results.

- Power (core)$_{MAX}$ = V_{DD_MAX} * (I_{DD_MAX} + I_{DDA_MAX} + I_{DDO_MAX}) = 2.625V * (60mA + 25mA + 140mA) = **590.625mW**

2. Junction Temperature.
Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad and directly affects the reliability of the device. The maximum recommended junction temperature for HiPerClockS™ devices is 125°C.

The equation for Tj is as follows: $Tj = \theta_{JA} * Pd\_total + T_A$

Tj = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)
T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming no air flow and a multi-layer board, the appropriate value is 37°C/W per Table 7 below.

Therefore, Tj for an ambient temperature of 85°C with all outputs switching is:
85°C + 0.591W * 37°C/W = 106.8°C. This is well below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow, and the type of board (single layer or multi-layer).

TABLE 7. THERMAL RESISTANCE θ_{JA} FOR 32-LEAD VFQFN, FORCED CONVECTION

θ_{JA} vs. Air Flow (Meters per Second)			
	0	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	37.0°C/W	32.4°C/W	29.0°C/W

Reliability Information

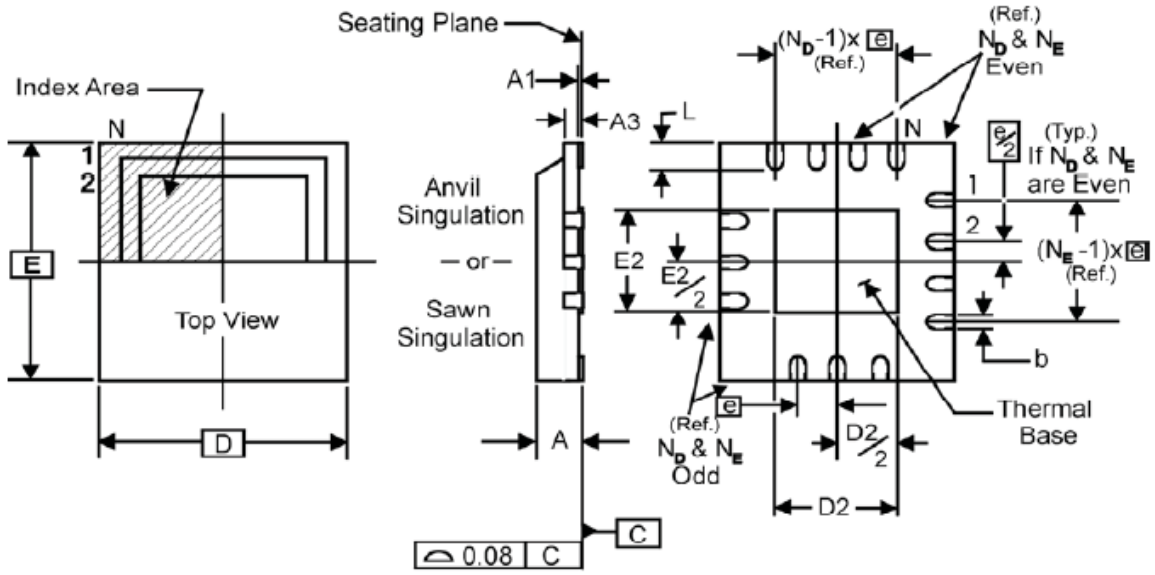
Table 8. θ_{JA} vs. Air Flow Table for 32 Lead VFQFN

θ_{JA} vs. Air Flow (Meters per Second)			
	0	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	37.0°C/W	32.4°C/W	29.0°C/W

Transistor Count

The transistor count for 844008I-46 is: 2993

Package Outline - K Suffix for 32 Lead VFQFN



NOTE: The following package mechanical drawing is a generic drawing that applies to any pin count VFQFN package. This drawing is not intended to convey the actual pin count or pin layout of this device. The pin count and pinout are shown on the front page. The package dimensions are in Table 9 below.

Table 9. Package Dimensions

JEDEC VARIATION ALL DIMENSIONS IN MILLIMETERS (VHHD -2/ -4)		
SYMBOL	**Minimum**	**Maximum**
N	32	
A	0.80	1.0
A1	0	0.05
A3	0.25 Reference	
b	0.18	0.30
e	0.50 BASIC	
N_D	8	
N_E	8	
D, E	5.0 BASIC	
D2, E2	3.0	3.3
L	0.30	0.50

Reference Document: JEDEC Publication 95, MO-220

TABLE 10. ORDERING INFORMATION

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
844008AKI-46LF	ICS008AI46L	32 Lead “Lead-Free” VFQFN	Tray	-40°C to 85°C
844008AKI-46LFT	ICS008AI46L	32 Lead “Lead-Free” VFQFN	1000 Tape & Reel	-40°C to 85°C

NOTE: Parts that are ordered with an “LF” suffix to the part number are the Pb-Free configuration and are RoHS compliant.

Revision History Sheet

Rev	Table	Page	Description of Change	Date
A		1	Product Discontinuation Notice - Last time buy expires November 2, 2016. PDN# CQ-15-05	11/6/15

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