

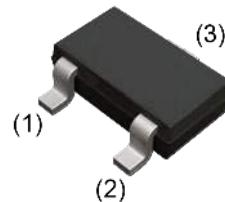
$V_{DSS}$	-20V
$R_{DS(on)}$ (Max.)	59m $\Omega$
$I_D$	$\pm 3.5A$
$P_D$	1W

### ●Outline

TSMT3

SOT-346T

SC-96



### ●Features

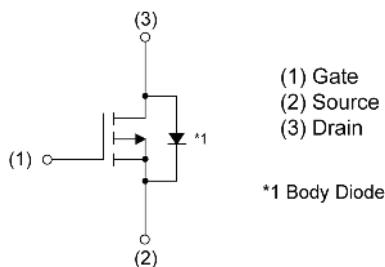
- 1) Low on - resistance.
- 2) High Power small mold Package (TSMT3).
- 3) Pb-free lead plating ; RoHS compliant.
- 4) Halogen Free.

### ●Application

Switching

Load switch

### ●Inner circuit



### ●Packaging specifications

Type	Packing	Embossed Tape
	Reel size (mm)	180
	Tape width (mm)	8
	Basic ordering unit (pcs)	3000
	Taping code	TCL
	Marking	JJ

### ●Absolute maximum ratings ( $T_a = 25^\circ\text{C}$ )

Parameter	Symbol	Value	Unit
Drain - Source voltage	$V_{DSS}$	-20	V
Continuous drain current	$I_D$ <sup>*1</sup>	$\pm 3.5$	A
Pulsed drain current	$I_{D,pulse}$ <sup>*2</sup>	$\pm 12$	A
Gate - Source voltage	$V_{GSS}$	$\pm 8$	V
Avalanche energy, single pulse	$E_{AS}$ <sup>*3</sup>	9.3	mJ
Avalanche current	$I_{AS}$ <sup>*3</sup>	-3.5	A
Power dissipation	$P_D$ <sup>*4</sup>	1	W
	$P_D$ <sup>*5</sup>	0.55	W
Junction temperature	$T_j$	150	°C
Range of storage temperature	$T_{stg}$	-55 to +150	°C

### ● Thermal resistance

Parameter	Symbol	Values			Unit
		Min.	Typ.	Max.	
Thermal resistance, junction - ambient	$R_{thJA}^{*4}$	-	-	125	°C/W
	$R_{thJA}^{*5}$	-	-	227	°C/W

### ● Electrical characteristics ( $T_a = 25^\circ\text{C}$ )

Parameter	Symbol	Conditions	Values			Unit
			Min.	Typ.	Max.	
Drain - Source breakdown voltage	$V_{(BR)DSS}$	$V_{GS} = 0\text{V}, I_D = -1\text{mA}$	-20	-	-	V
Breakdown voltage temperature coefficient	$\frac{\Delta V_{(BR)DSS}}{\Delta T_j}$	$I_D = -1\text{mA}$ referenced to $25^\circ\text{C}$	-	-10.3	-	mV/°C
Zero gate voltage drain current	$I_{DSS}$	$V_{DS} = -20\text{V}, V_{GS} = 0\text{V}$	-	-	-1	μA
Gate - Source leakage current	$I_{GSS}$	$V_{GS} = \pm 8\text{V}, V_{DS} = 0\text{V}$	-	-	$\pm 100$	nA
Gate threshold voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = -1\text{mA}$	-0.5	-	-1.2	V
Gate threshold voltage temperature coefficient	$\frac{\Delta V_{GS(th)}}{\Delta T_j}$	$I_D = -1\text{mA}$ referenced to $25^\circ\text{C}$	-	1.7	-	mV/°C
Static drain - source on - state resistance	$R_{DS(on)}^{*6}$	$V_{GS} = -4.5\text{V}, I_D = -3.5\text{A}$	-	42	59	mΩ
		$V_{GS} = -2.5\text{V}, I_D = -3.5\text{A}$	-	54	76	
		$V_{GS} = -1.8\text{V}, I_D = -0.9\text{A}$	-	84	135	
Gate input resistance	$R_G$	$f = 1\text{MHz}$ , open drain	-	9.5	-	Ω
Forward Transfer Admittance	$ Y_{fs} ^{*6}$	$V_{DS} = -5\text{V}, I_D = -3.5\text{A}$	4.3	-	-	S

\*1  $V_{GS} \geq 2.5\text{V}$

\*2  $P_w \leq 10\mu\text{s}$ , Duty cycle  $\leq 1\%$

\*3  $L \approx 1\text{mH}$ ,  $V_{DD} = -10\text{V}$ ,  $R_G = 25\Omega$ , STARTING  $T_j = 25^\circ\text{C}$  Fig.3-1,3-2

\*4 Mounted on a ceramic board (30×30×0.8mm)

\*5 Mounted on a FR4 (12×20×0.8mm)

\*6 Pulsed

● Electrical characteristics ( $T_a = 25^\circ\text{C}$ )

Parameter	Symbol	Conditions	Values			Unit
			Min.	Typ.	Max.	
Input capacitance	$C_{iss}$	$V_{GS} = 0\text{V}$ $V_{DS} = -10\text{V}$ $f = 1\text{MHz}$	-	460	-	pF
Output capacitance	$C_{oss}$		-	90	-	
Reverse transfer capacitance	$C_{rss}$		-	80	-	
Turn - on delay time	$t_{d(on)}^{\ast 6}$	$V_{DD} \approx -10\text{V}, V_{GS} = -4.5\text{V}$ $I_D = -1.75\text{A}$ $R_L \approx 5.7\Omega$ $R_G = 10\Omega$	-	9	-	ns
Rise time	$t_r^{\ast 6}$		-	30	-	
Turn - off delay time	$t_{d(off)}^{\ast 6}$		-	50	-	
Fall time	$t_f^{\ast 6}$		-	30	-	

● Gate charge characteristics ( $T_a = 25^\circ\text{C}$ )

Parameter	Symbol	Conditions	Values			Unit
			Min.	Typ.	Max.	
Total gate charge	$Q_g^{\ast 6}$	$V_{DD} \approx -10\text{V},$ $I_D = -3.5\text{A},$ $V_{GS} = -4.5\text{V}$	-	6.5	-	nC
Gate - Source charge	$Q_{gs}^{\ast 6}$		-	0.9	-	
Gate - Drain charge	$Q_{gd}^{\ast 6}$		-	2.2	-	

● Body diode electrical characteristics (Source-Drain) ( $T_a = 25^\circ\text{C}$ )

Parameter	Symbol	Conditions	Values			Unit
			Min.	Typ.	Max.	
Body diode continuous forward current	$I_S$	$T_a = 25^\circ\text{C}$	-	-	-0.8	A
Body diode pulse current	$I_{SP}^{\ast 2}$		-	-	-12	
Forward voltage	$V_{SD}^{\ast 6}$	$V_{GS} = 0\text{V}, I_S = -0.8\text{A}$		-	-1.2	V

## ● Electrical characteristic curves

Fig.1 Power Dissipation Derating Curve

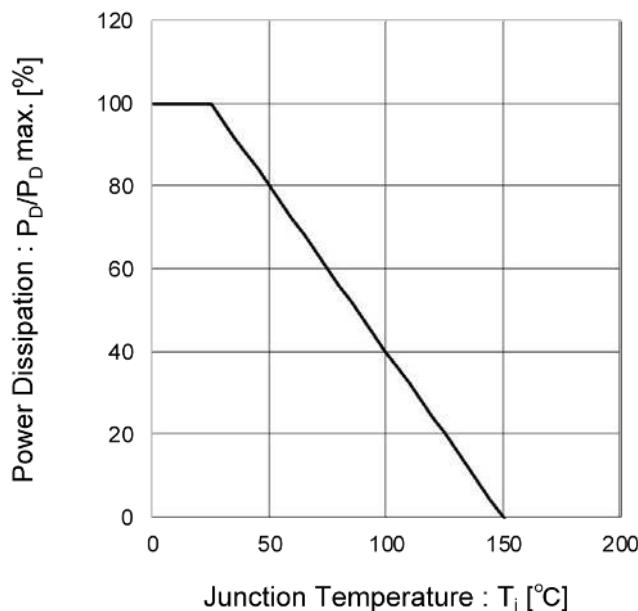


Fig.2 Maximum Safe Operating Area

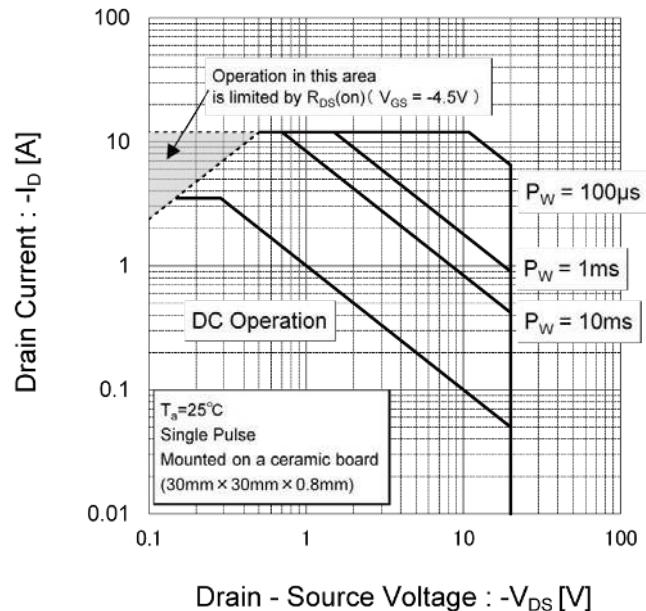


Fig.3 Normalized Transient Thermal Resistance vs. Pulse Width

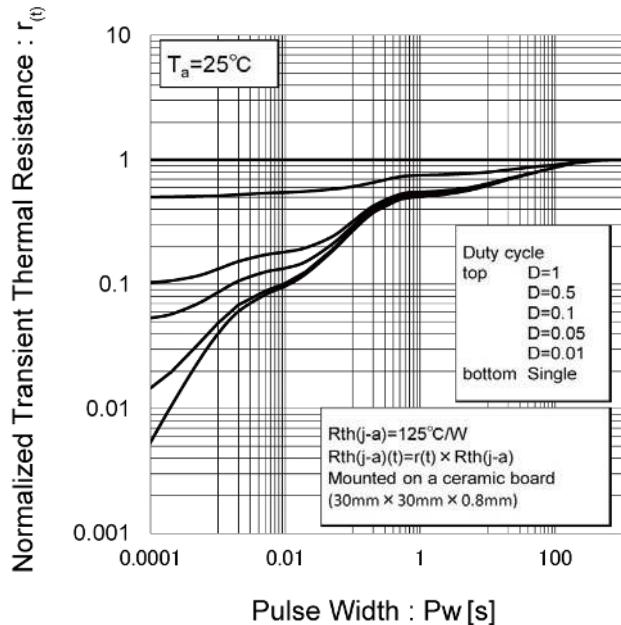
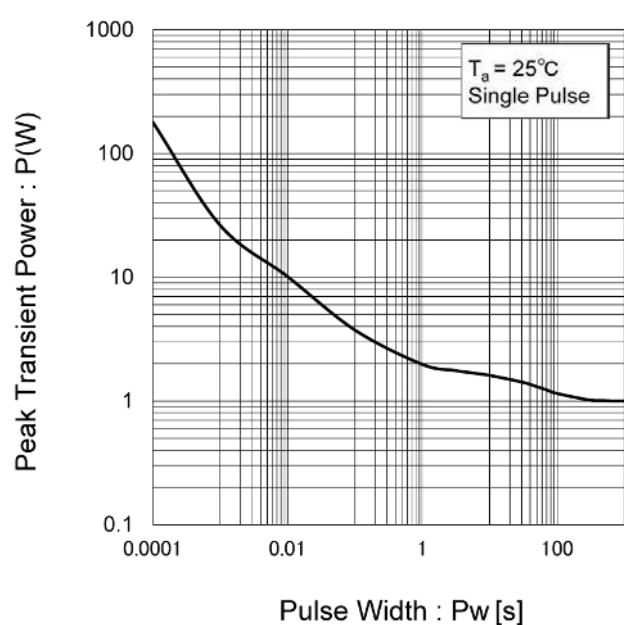


Fig.4 Single Pulse Maximum Power dissipation



## ●Electrical characteristic curves

Fig.5 Typical Output Characteristics(I)

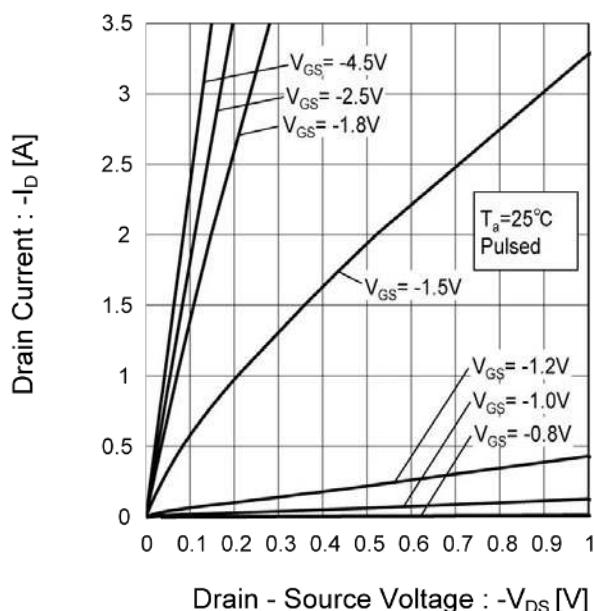


Fig.6 Typical Output Characteristics(II)

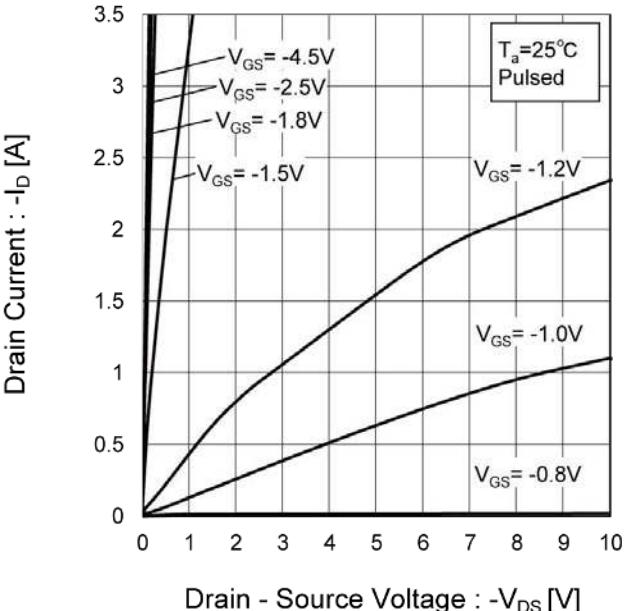
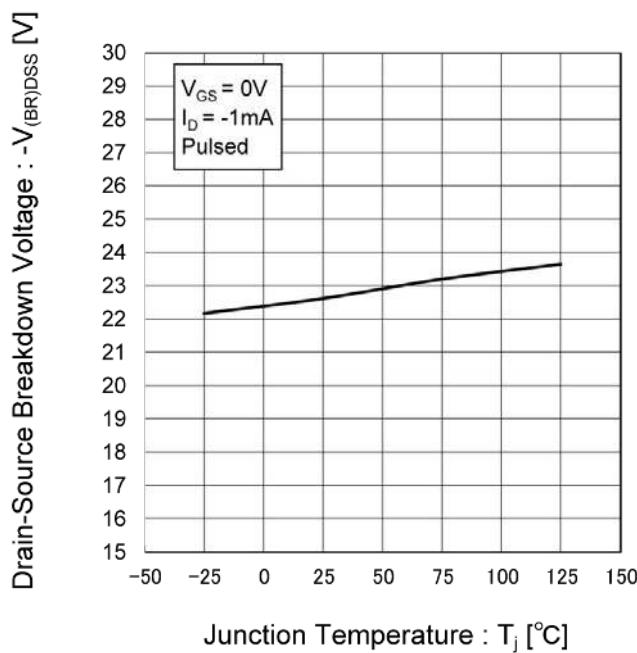


Fig.7 Breakdown Voltage vs. Junction Temperature



## ●Electrical characteristic curves

Fig.8 Typical Transfer Characteristics

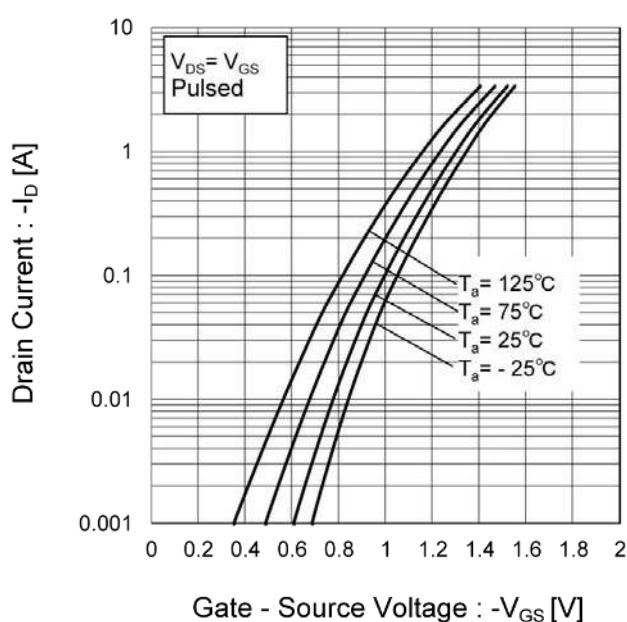


Fig.9 Gate Threshold Voltage vs. Junction Temperature

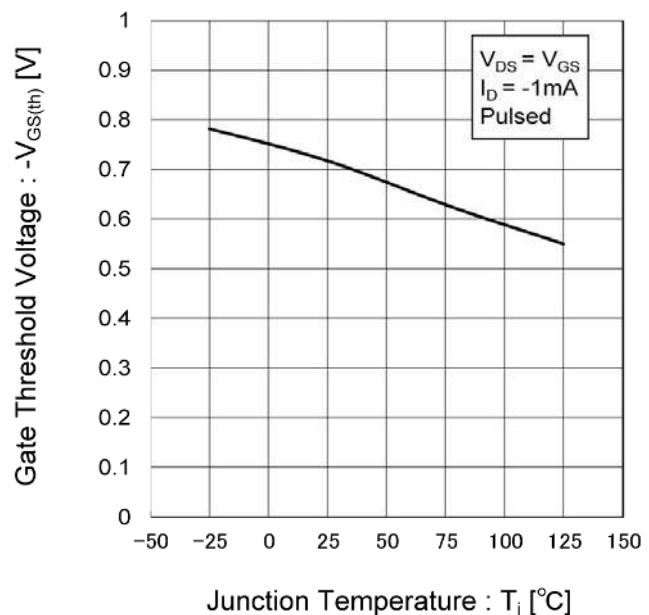
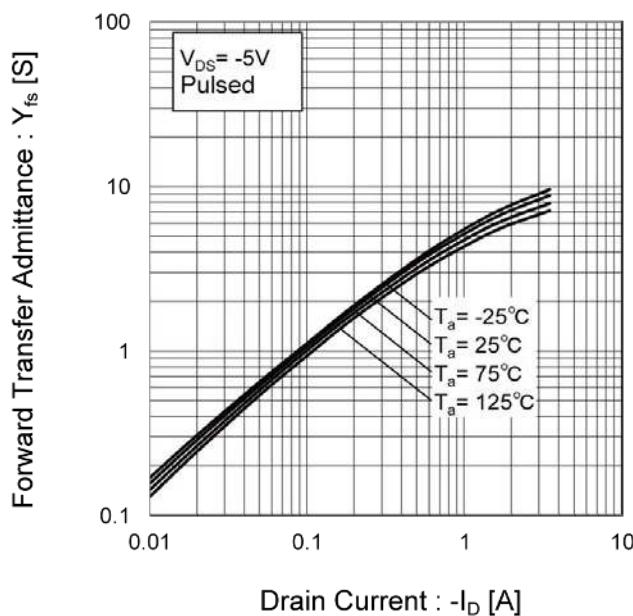


Fig.10 Forward Transfer Admittance vs. Drain Current



● Electrical characteristic curves

Fig.11 Drain Current Derating Curve

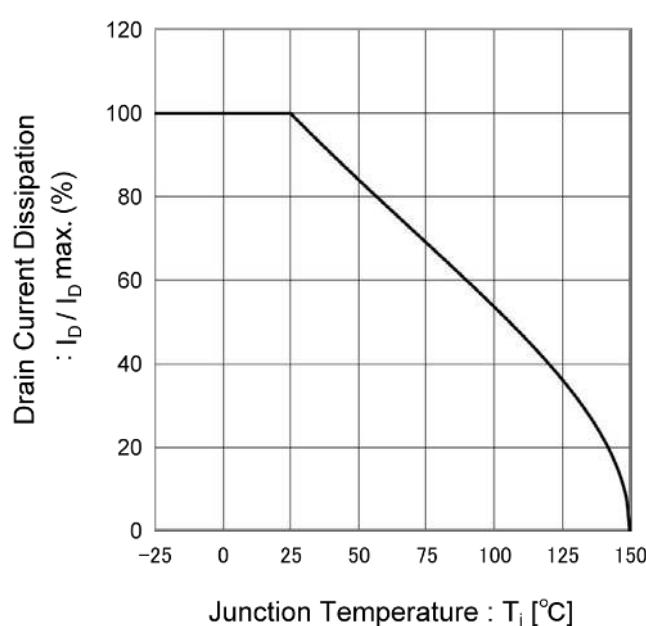


Fig.12 Static Drain - Source On - State Resistance vs. Gate Source Voltage

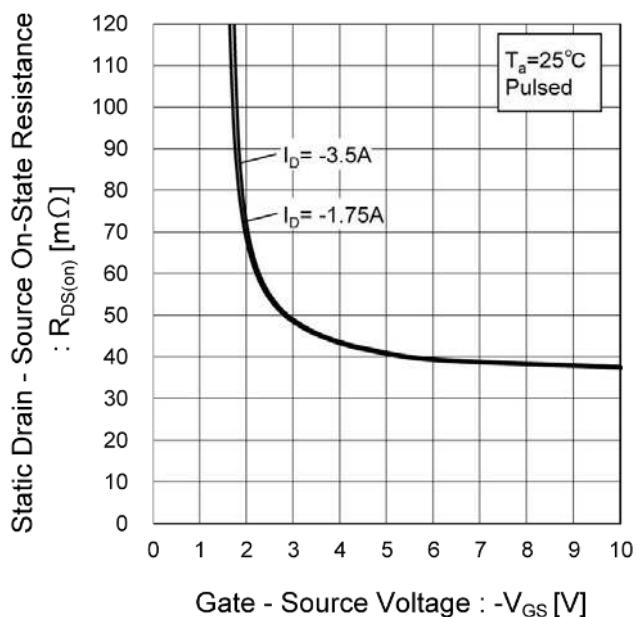
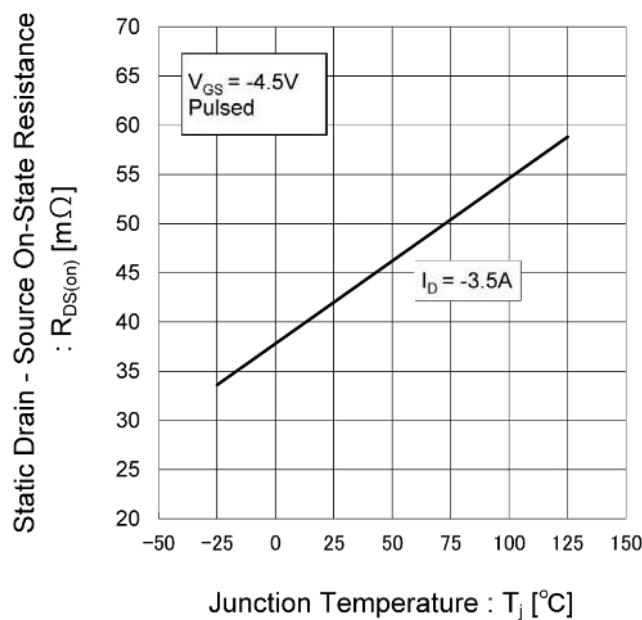


Fig.13 Static Drain - Source On - State Resistance vs. Junction Temperature



## ● Electrical characteristic curves

Fig.14 Static Drain - Source On - State  
Resistance vs. Drain Current( $I_D$ )

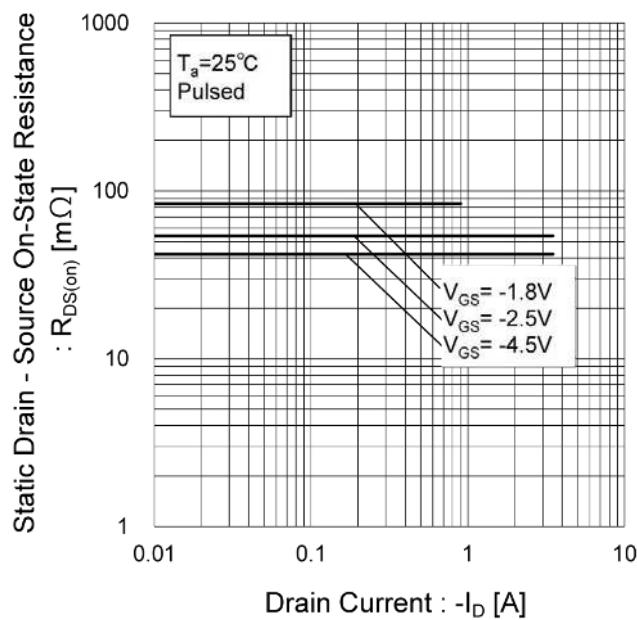


Fig.15 Static Drain - Source On - State  
Resistance vs. Drain Current( $I_D$ )

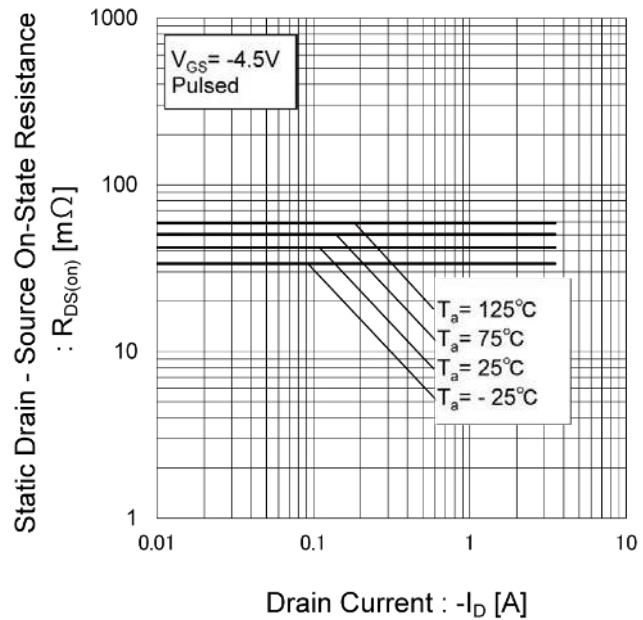


Fig.16 Static Drain - Source On - State  
Resistance vs. Drain Current(III)

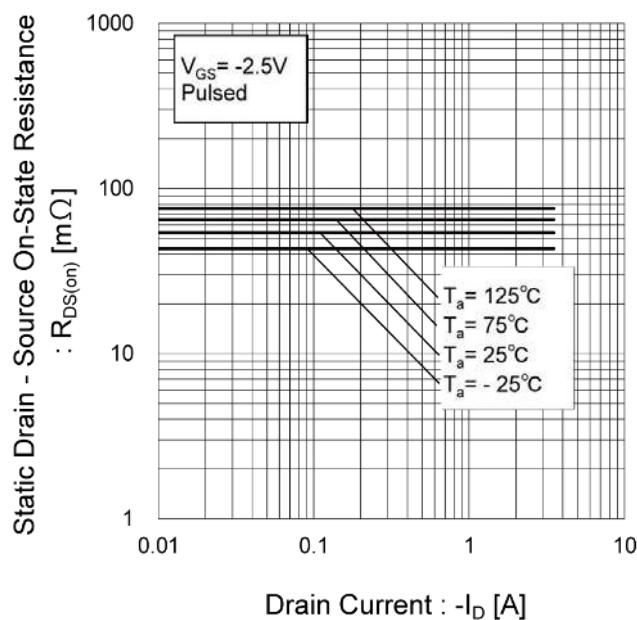
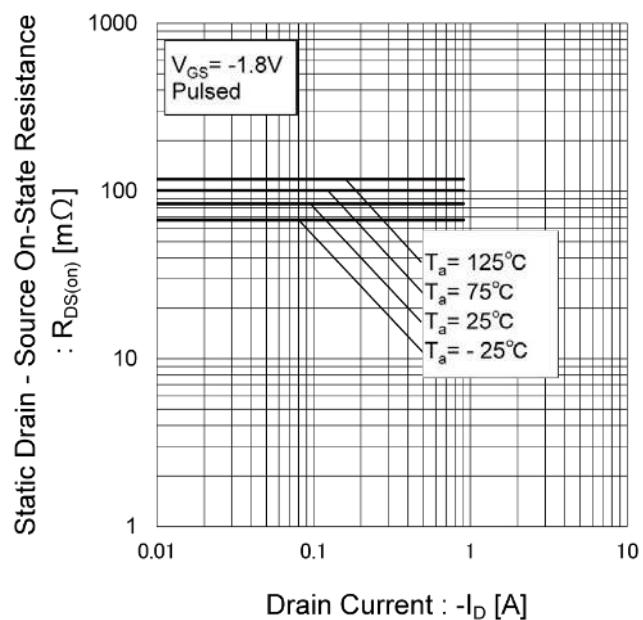


Fig.17 Static Drain - Source On - State  
Resistance vs. Drain Current(IV)



## ●Electrical characteristic curves

Fig.18 Typical Capacitance vs. Drain - Source Voltage

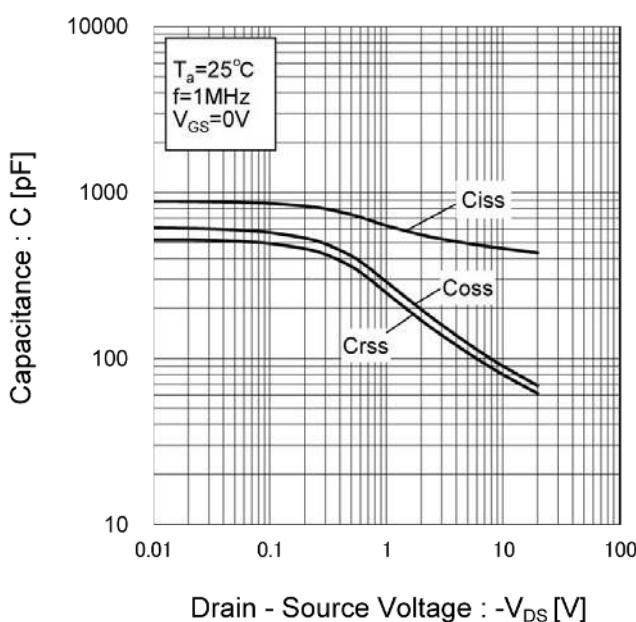


Fig.19 Switching Characteristics

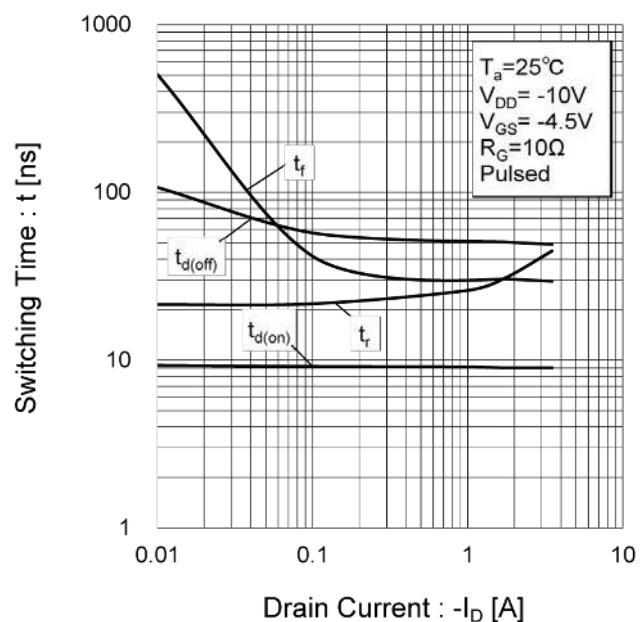


Fig.20 Dynamic Input Characteristics

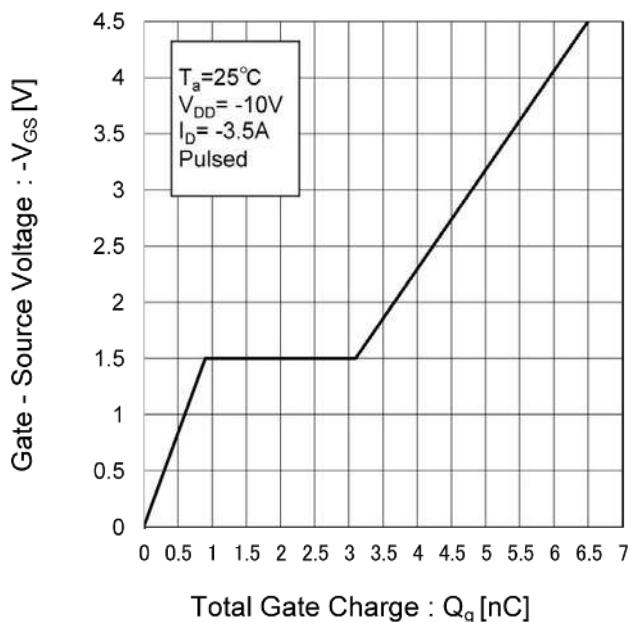
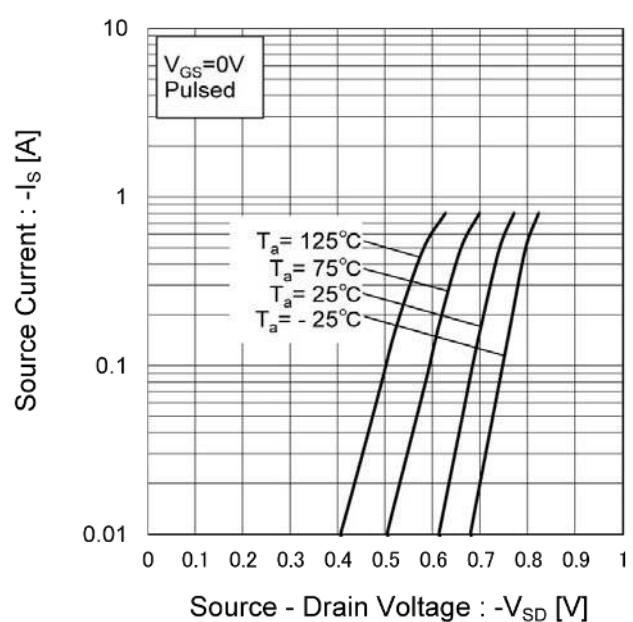


Fig.21 Source Current vs. Source Drain Voltage



## ● Measurement circuits

Fig.1-1 Switching Time Measurement Circuit

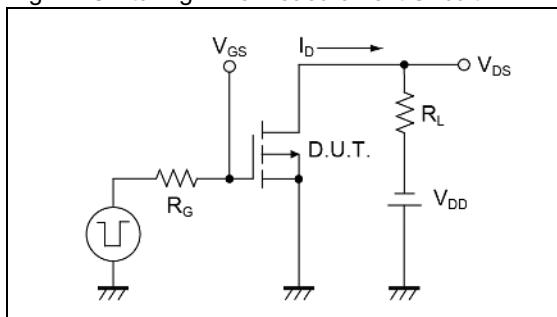


Fig.1-2 Switching Waveforms

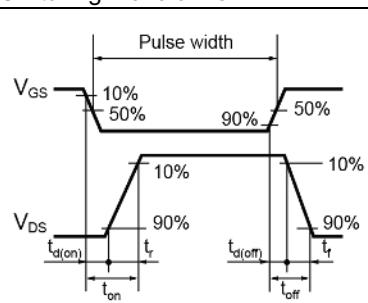


Fig.2-1 Gate Charge Measurement Circuit

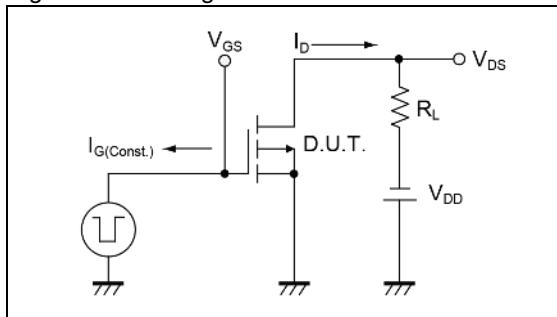


Fig.2-2 Gate Charge Waveform

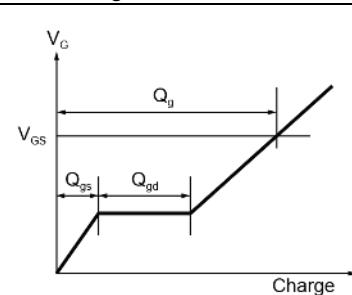


Fig.3-1 Avalanche Measurement Circuit

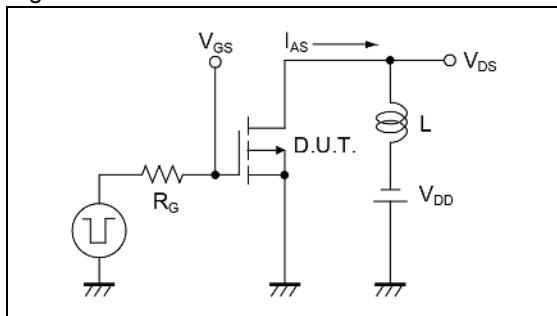
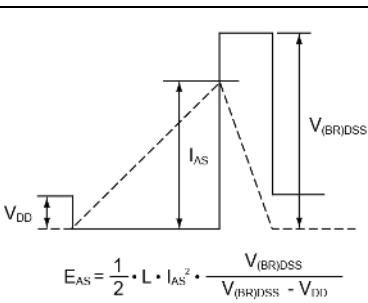


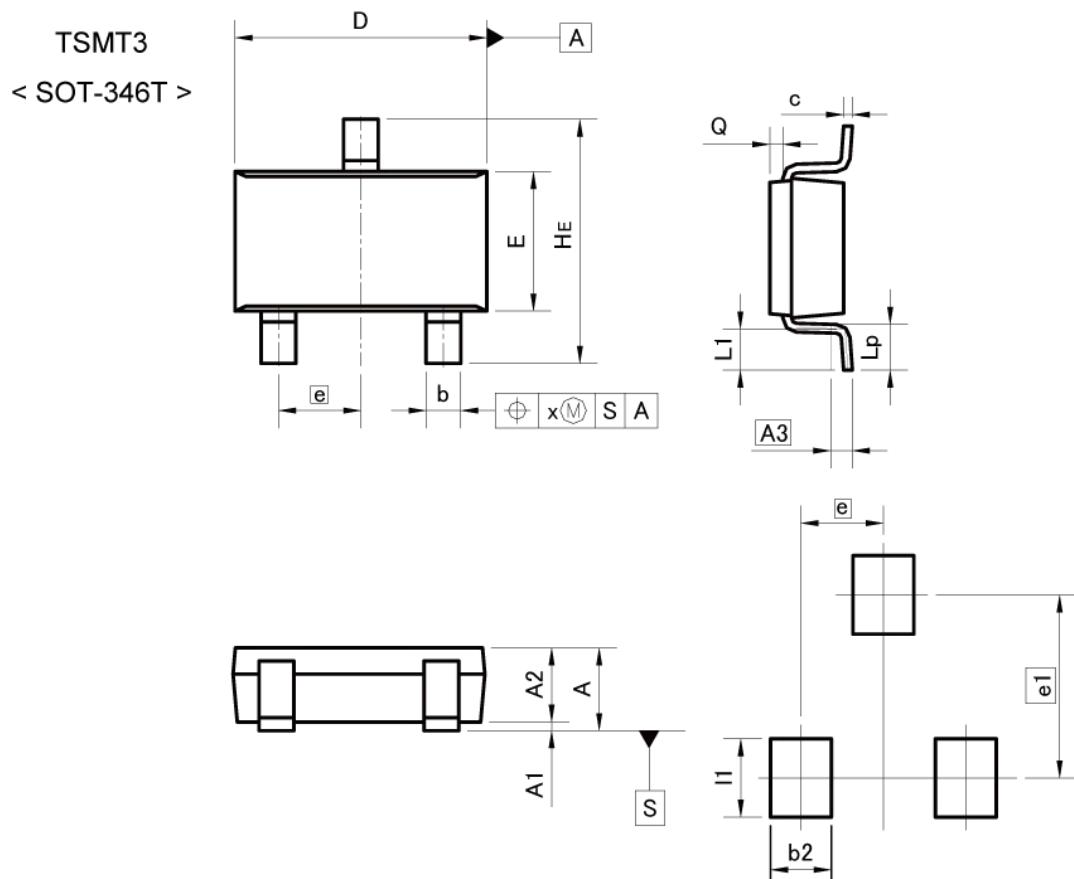
Fig.3-2 Avalanche Waveform



## ● Notice

This product might cause chip aging and breakdown under the large electrified environment.  
Please consider to design ESD protection circuit.

## ●Dimensions



Pattern of terminal position areas  
[Not a pattern of soldering pads]

DIM	MILIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	—	1.00	—	0.039
A1	0.00	0.10	0.000	0.004
A2	0.75	0.95	0.030	0.037
A3	0.25		0.010	
b	0.35	0.50	0.014	0.020
c	0.10	0.26	0.004	0.010
D	2.80	3.00	0.110	0.118
E	1.50	1.80	0.059	0.071
e	0.95		0.037	
HE	2.60	3.00	0.102	0.118
L1	0.30	0.60	0.012	0.024
Lp	0.40	0.70	0.016	0.028
Q	0.05	0.25	0.002	0.010
x	—	0.20	—	0.008

DIM	MILIMETERS		INCHES	
	MIN	MAX	MIN	MAX
b2		0.70	—	0.028
e1	2.10		0.083	
l1	—	0.90	—	0.035

Dimension in mm/inches

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