BLP15M9S70

Power LDMOS transistor

Rev. 4 — 12 January 2023

AMPLEON

Product data sheet

1. Product profile

1.1 General description

A 70 W general purpose LDMOS RF power transistor for broadcast and ISM applications in HF to 2 GHz band.

Table 1. Application performance

Test signal	f	P_L	G_p	η_D	RL_{in}
	(MHz)	(W)	(dB)	(%)	(dB)
pulsed CW	1400	70	17.6	70	–14
CW	915	70	17	75	–17

1.2 Features and benefits

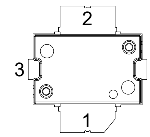
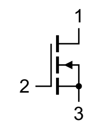
- High efficiency
- Integrated dual sided ESD protection
- Excellent ruggedness
- High power gain
- Excellent reliability
- Easy power control
- For RoHS compliance see the product details on the Ampleon website

1.3 Applications

- RF power amplifiers for CW applications
- Industrial, scientific and medical applications
- Broadcast transmitter applications

2. Pinning information

Table 2. Pinning

Pin	Description	Simplified outline	Graphic symbol
1	drain		 sym112
2	gate		
3	source [1]		

[1] Connected to flange.

3. Ordering information

Table 3. Ordering information

Package name	Orderable part number	12NC	Packing description	Min. orderable quantity (pieces)
TO-270-2F-1	BLP15M9S70Z	9349 602 43515	TR13; 500-fold; 24 mm; dry pack	500
	BLP15M9S70XY	9349 602 43538	TR7; 100-fold; 24 mm; dry pack	100

4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage		-	65	V
V_{GS}	gate-source voltage		–6	+13	V
T_{stg}	storage temperature		–65	+150	°C
T_j	junction temperature	[1]	-	225	°C

[1] Continuous use at maximum temperature will affect the reliability, for details refer to the online MTF calculator.

5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j-c)}$	thermal resistance from junction to case	T_{case} = 85 °C; V_{DS} = 32 V; P_L = 70 W	1.0	K/W

6. Characteristics

Table 6. DC characteristics

T_j = 25 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.66 mA	65	70	-	V
$V_{GS(th)}$	gate-source threshold voltage	V_{DS} = 10 V; I_D = 66 mA	1.5	2.0	2.5	V
I_{DSS}	drain leakage current	V_{GS} = 0 V; V_{DS} = 32 V	-	-	1.4	μA
I_{DSX}	drain cut-off current	V_{GS} = $V_{GS(th)}$ + 3.75 V; V_{DS} = 10 V	-	12.6	-	A
I_{GSS}	gate leakage current	V_{GS} = 11 V; V_{DS} = 0 V	-	-	140	nA
$R_{DS(on)}$	drain-source on-state resistance	V_{GS} = $V_{GS(th)}$ + 3.75 V; I_D = 2.31 A	-	185	-	mΩ

Table 7. AC characteristics

T_j = 25 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
C_{iss}	input capacitance	V_{GS} = 0 V; V_{DS} = 50 V; f = 1 MHz	-	61	-	pF
C_{oss}	output capacitance	V_{GS} = 0 V; V_{DS} = 50 V; f = 1 MHz	-	22	-	pF
C_{rss}	reverse transfer capacitance	V_{GS} = 0 V; V_{DS} = 50 V; f = 1 MHz	-	0.45	-	pF

Table 8. RF characteristics

RF characteristics in Ampleon production test circuit; typical RF performance at T_{case} = 25 °C; V_{DS} = 32 V: I_{Dq} = 300 mA; t_p = 100 μs; δ = 10 %.

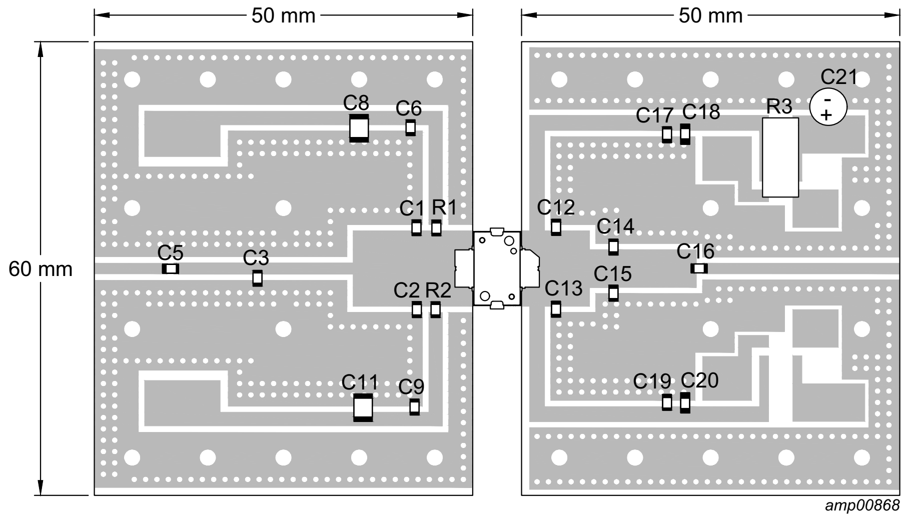
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Pulsed RF, class-AB						
G_p	power gain	f = 1400 MHz; P_L = 70 W	16.5	17.8	-	dB
η_D	drain efficiency	f = 1400 MHz; P_L = 70 W	61	65.5	-	%
RL_{in}	input return loss	f = 1400 MHz; P_L = 70 W	-	−17	-	dB

7. Test information

7.1 Ruggedness in class-AB operation

The BLP15M9S70 is capable of withstanding a load mismatch corresponding to a VSWR = 10 : 1 through all phases under the following conditions: V_{DS} = 32 V; f = 1400 MHz at rated load power on RF development board using a pulsed CW RF signal which has ~150 ns rise and fall time.

7.2 Test circuit



Printed-Circuit Board (PCB): Rogers RO4350B; ε_r = 3.66 F/m; height = 0.762 mm; Cu (top/bottom metalization); thickness copper plating = 35 μm.

See Table 9 for a list of components.

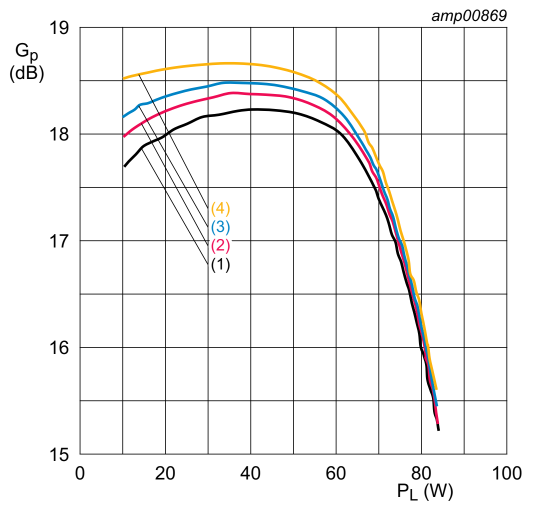
Fig 1. Component layout for production RF Test Circuit

Table 9. List of components

See Figure 1 for component layout.

Component	Description	Value	Remarks
C1, C2	multilayer ceramic chip capacitor	6.2 pF	ATC 800A
C3	multilayer ceramic chip capacitor	2 pF	ATC 800A
C5, C6, C9, C17, C19, C16	multilayer ceramic chip capacitor	100 pF	ATC 800A
C8, C11, C18, C20	multilayer ceramic chip capacitor	100 nF, 100 V	
C12, C13	multilayer ceramic chip capacitor	3 pF	ATC 800A
C14, C15	multilayer ceramic chip capacitor	2.1 pF	ATC 800A
C21	electrolytic capacitor	220 μF, 63 V	
R1, R2	chip resistor	10 Ω	SMD 0805
R3	shunt resistor	10 mΩ	for current monitoring

7.3 Graphical data



V_{DS} = 32 V; f = 1400 MHz; t_p = 100 μs; δ = 10 %.

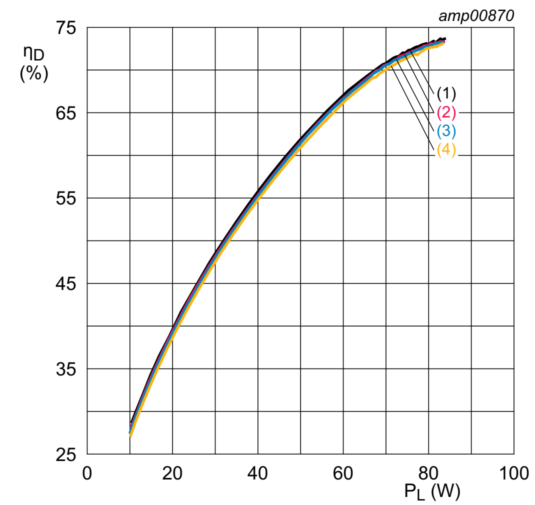
(1) I_{Dq} = 200 mA

(2) I_{Dq} = 250 mA

(3) I_{Dq} = 300 mA

(4) I_{Dq} = 400 mA

Fig 2. Power gain as a function of output power; typical values



V_{DS} = 32 V; f = 1400 MHz; t_p = 100 μs; δ = 10 %.

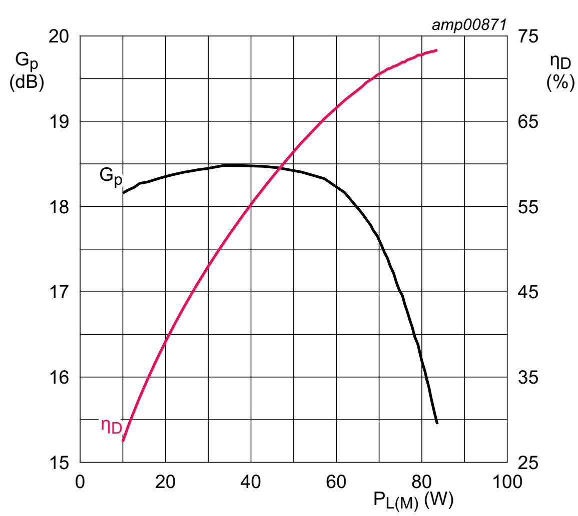
(1) I_{Dq} = 200 mA

(2) I_{Dq} = 250 mA

(3) I_{Dq} = 300 mA

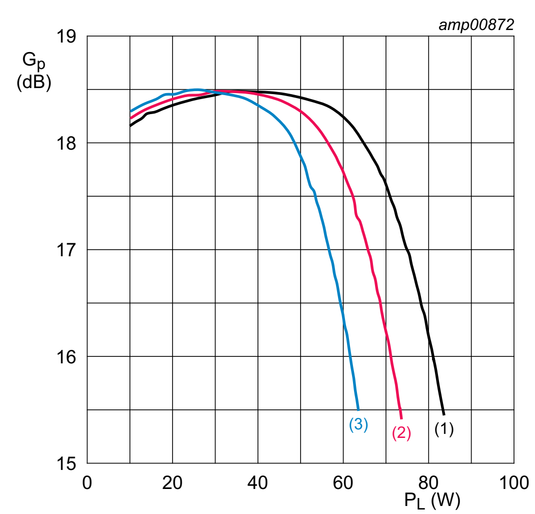
(4) I_{Dq} = 400 mA

Fig 3. Drain efficiency as a function of output power; typical values



V_{DS} = 32 V; I_{Dq} = 300 mA; f = 1400 MHz; t_p = 100 μs; δ = 10 %.

Fig 4. Power gain and drain efficiency as function of peak output power; typical values



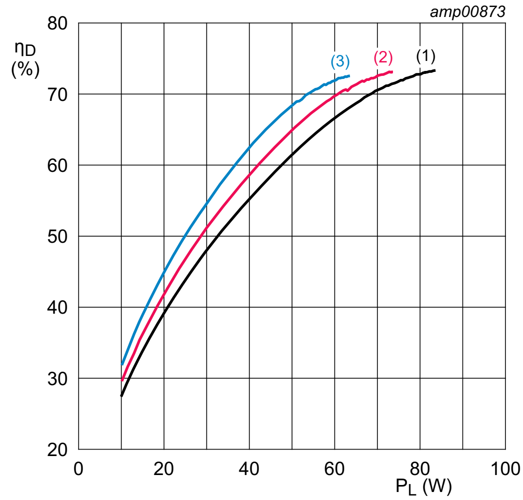
I_{Dq} = 300 mA; f = 1400 MHz; t_p = 100 μs; δ = 10 %.

(1) V_{DS} = 32 V

(2) V_{DS} = 30 V

(3) V_{DS} = 28 V

Fig 5. Power gain as a function of output power; typical values



I_{Dq} = 300 mA; f = 1400 MHz; t_p = 100 μs; δ = 10 %.

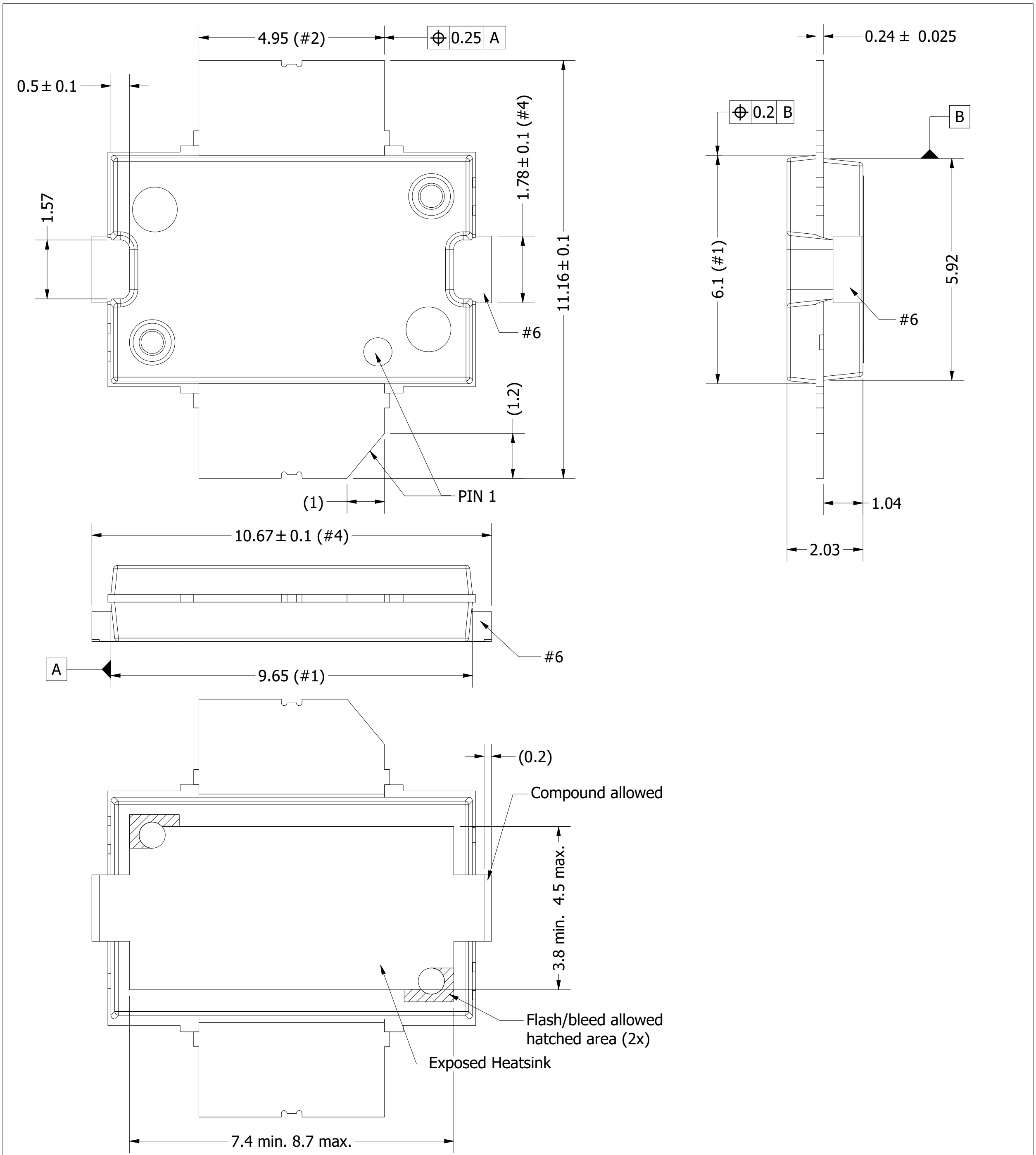
(1) V_{DS} = 32 V

(2) V_{DS} = 30 V

(3) V_{DS} = 28 V

Fig 6. Drain efficiency as a function of output power; typical values

8. Package outline

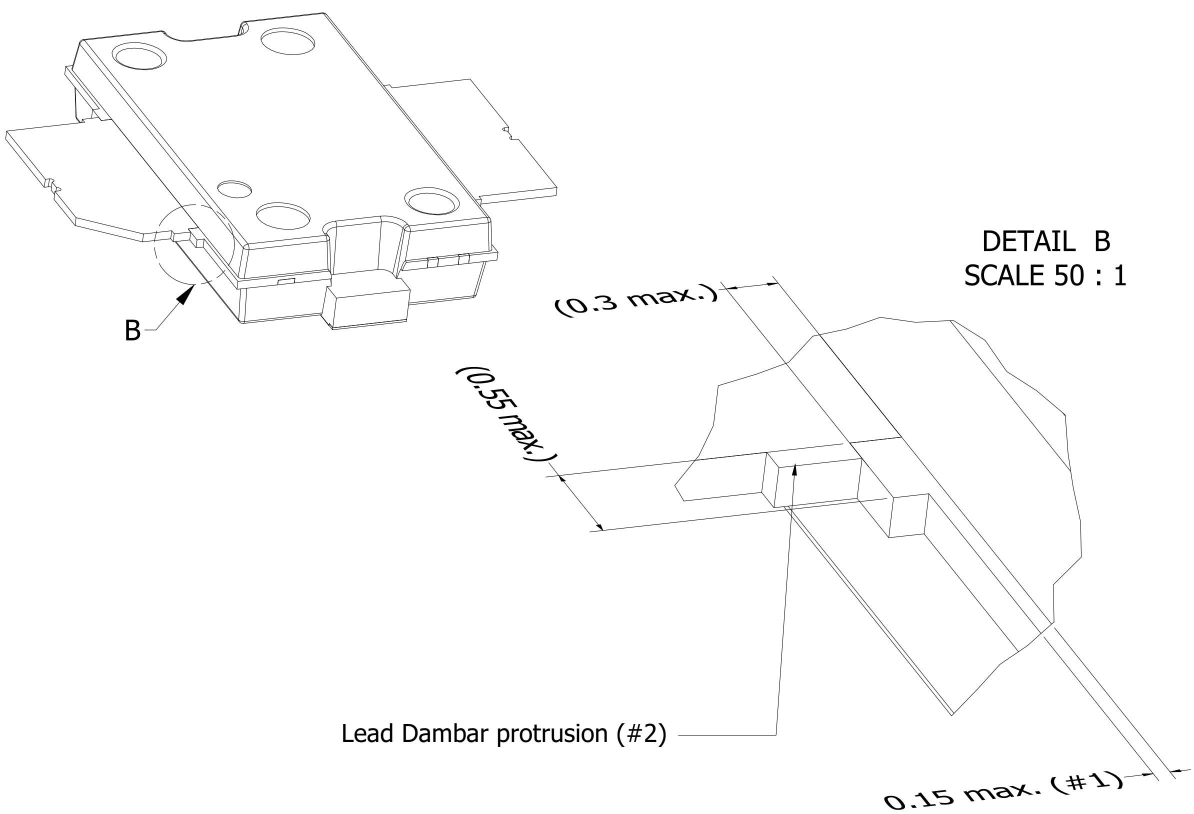


Package outline drawing: TO-270-2F-1	units in mm.	Tolerances unless otherwise stated: Dimension: ± 0.05 Angle: ± 1°	Revision: 0 Revision date: 11/7/2022
		Third angle projection	Sheet 1 of 2

Fig 7. Package outline TO-270-2F-1 (sheet 1 of 2)

TO-270-2F-1

Drawing Notes	
Items	Description
(1)	Dimensions are excluding mold protrusion. The mold protrusion is maximum 0.15 mm per side. See also detail B. In the dambar area max. protrusion is 0.55 mm. max. in length and 0.3 mm. max. in width (4x). See also detail B.
(2)	The lead dambar (metal) protrusions are not included. Add 0.14 mm max to the total lead dimension at the dambar location.
(3)	The leads and exposed heatsink are plated with matte Tin (Sn).
(4)	Dimensions (Heatsink ears) 10,67 and 1,78 do not include mouldprotrusion. Overall Max. dimensions incl. mould protrusions is 10.92 mm. (max.) and 2.03 mm. (max.).
(5)	Lead coplanarity over the leads is 0,1 mm. maximum.
(6)	Surfaces may remain unplated (not solderable surfaces).



Package outline drawing: TO-270-2F-1	units in mm.	Tolerances unless otherwise stated: Dimension: ± 0.05 Angle: ± 1°	Revision: 0 Revision date: 11/7/2022
		Third angle projection	Sheet 2 of 2

Fig 8. Package outline TO-270-2F-1 (sheet 2 of 2)

9. Handling information

CAUTION	
	This device is sensitive to ElectroStatic Discharge (ESD). Observe precautions for handling electrostatic sensitive devices. Such precautions are described in the *ANSI/ESD S20.20*, *IEC/ST 61340-5*, *JESD625-A* or equivalent standards.

Table 10. ESD sensitivity

ESD model	Class
Charged Device Model (CDM); According to ANSI/ESDA/JEDEC standard JS-002	C2A [1]
Human Body Model (HBM); According to ANSI/ESDA/JEDEC standard JS-001	2 [2]

[1] CDM classification C2A is granted to any part that passes after exposure to an ESD pulse of 500 V.

[2] HBM classification 2 is granted to any part that passes after exposure to an ESD pulse of 2000 V.

10. Abbreviations

Table 11. Abbreviations

Acronym	Description
CW	Continuous Wave
ESD	ElectroStatic Discharge
ISM	Industrial, Scientific and Medical
LDMOS	Laterally Diffused Metal-Oxide Semiconductor
MTF	Median Time to Failure
RoHS	Restriction of Hazardous Substances
SMD	Surface Mounted Device
VSWR	Voltage Standing Wave Ratio

11. Revision history

Table 12. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BLP15M9S70 v.4	20230112	Product data sheet	-	BLP15M9S70 v.3
Modifications:	• Table 3 on page 2: package name changed from SOT1482-1 to TO-270-2F-1 • Table 5 on page 2: value changed from 1.44 K/W to 1.0 K/W • Section 8 on page 7: package outline drawing changed from SOT1482-1 to TO-270-2F-1 • Section 12 on page 10: updated section			
BLP15M9S70 v.3	20210716	Product data sheet	-	BLP15M9S70 v.2
BLP15M9S70 v.2	20210223	Product data sheet	-	BLP15M9S70 v.1
BLP15M9S70 v.1	20200807	Product data sheet	-	-

12. Legal information

12.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.ampleon.com.

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14. Contents

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