Dual H-Bridge Driver with Boost Converter

■ GENERAL DESCRIPTION

The **NJW4814** is a dual H-bridge driver with boost converter IC.

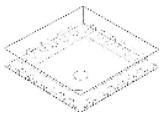
It can boost the output voltage from Li-ion battery and/or a 5V power supply and drives a piezo device by two H- bridge drivers.

48ms of internal fixed soft start function of the boost circuit sets a limit to startup current.

The dual H-bridge drivers have independent signal inputs and a fault output function, therefore the NJW4814 improves controllability from a microcomputer.

The input frequency of H-bridge driver is up to 300kHz.

■ PACKAGE OUTLINE

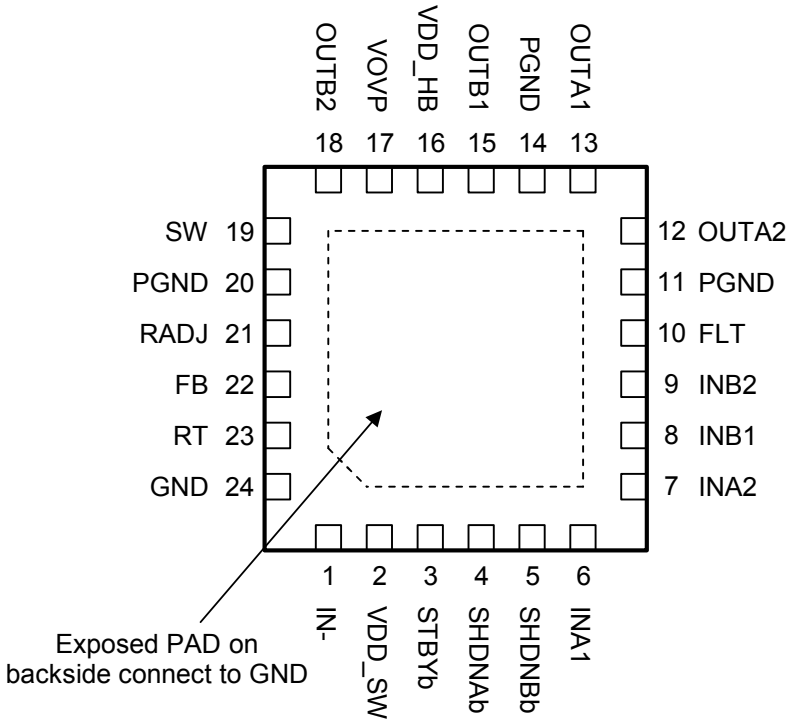


NJW4814MLE

■ FEATURES

● Boost Converter Block	Output Switch Voltage	40V max.
	Switching Current	1.5A min.
	PWM Control	
	Operating Voltage Range	2.7 to 5.5V
	Oscillation Frequency Range	380k to 1MHz
	Soft Start Function	48ms typ.
	Over Current Protection	
	Over Voltage Protection	
● H-Bridge Driver Block	Internal 2 Channel H-Bridge	
	Each Channel Operates Individually	
	Over Current Protection	±300mA typ.
	Operating Voltage Range	7.0 to 35V
	Switching Frequency	300kHz max.
	Output Shut Down Control	
	Fault Indicator Output	
● Under Voltage Lockout		
● Built-in Thermal Shutdown		
● Standby Function		
● Package Outline	NJW4814MLE : EQFN24-LE	

■ PIN CONFIGURATION



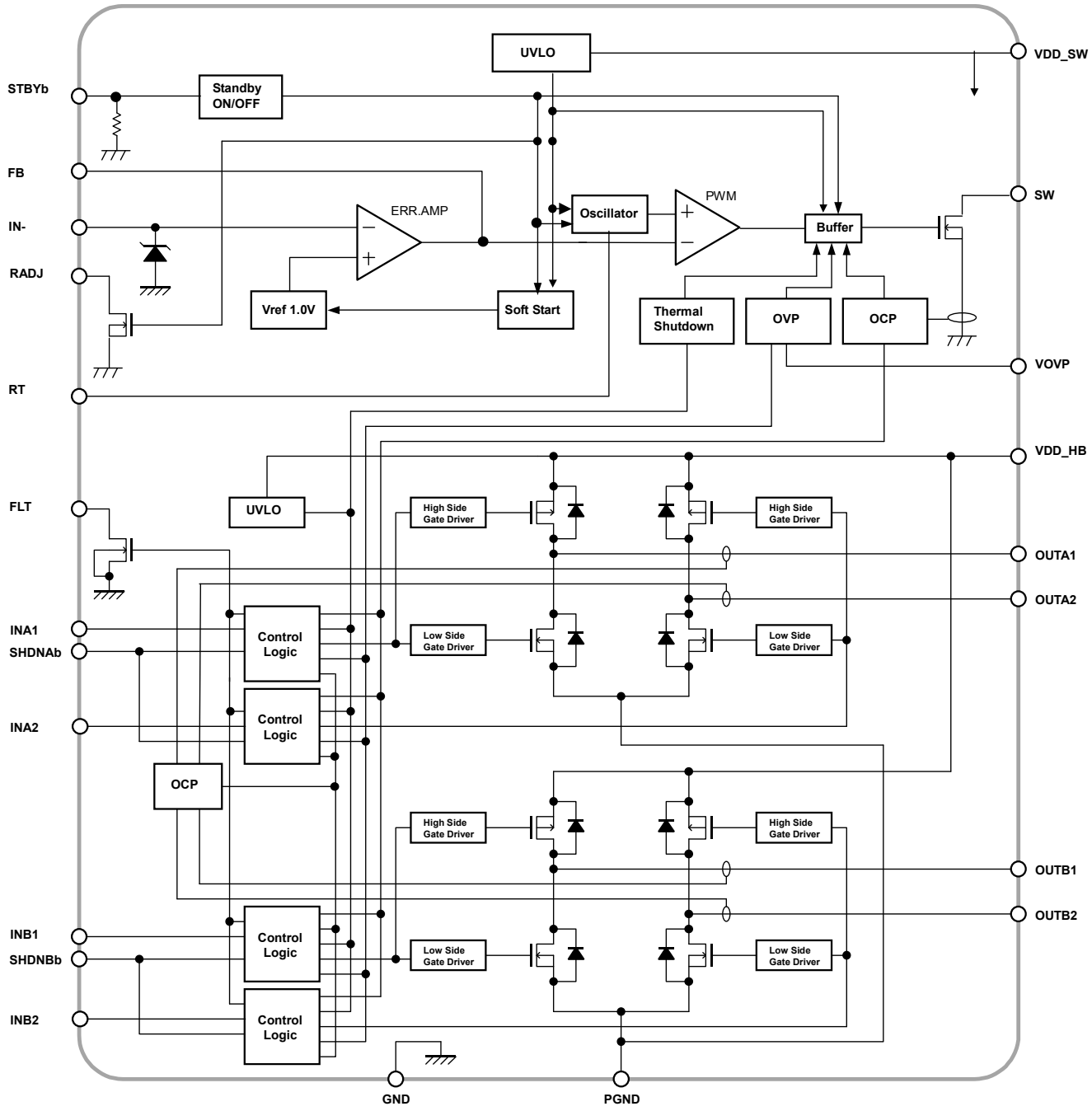
< Top View>

NJW4814MLE

PIN FUNCTION

1. IN-	13. OUTA1
2. VDD_SW	14. PGND
3. STBYb	15. OUTB1
4. SHDNAb	16. VDD_HB
5. SHDNBb	17. VOVP
6. INA1	18. OUTB2
7. INA2	19. SW
8. INB1	20. PGND
9. INB2	21. RADJ
10. FLT	22. FB
11. PGND	23. RT
12. OUTA2	24. GND

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATINGS (Ta=25°C)

PARAMETER	SYMBOL	MAXIMUM RATINGS	UNIT
Boost Converter Block			
Supply Voltage	V_{DD_SW}	-0.3 to +6	V
SW pin Voltage	V_{SW}	-0.3 to +40	V
RADJ pin Voltage	V_{RADJ}	-0.3 to +6 (*1)	V
IN- pin Voltage	V_{IN-}	-0.3 to +6 (*1)	V
STBYb pin Voltage	V_{STBYb}	-0.3 to +6 (*1)	V
VOVP pin Voltage (*2)	V_{OVP}	-0.3 to +40	V
H-Bridge Driver Block			
Supply Voltage	V_{DD_HB}	-0.3 to +40	V
SHDNAb, SHDNBb pin Voltage	V_{SHDNAb} V_{SHDNBb}	-0.3 to +6 (*1)	V
INA1, INA2, INB1, INB2 pin Voltage	V_{INA1} , V_{INA2} V_{INB1} , V_{INB2}	-0.3 to +6 (*1)	V
General			
FLT pin Voltage	V_{FLT}	-0.3 to +6	V
Power Dissipation	P_D	910 (*3) 2,100 (*4)	mW
Junction Temperature Range	T_j	-40 to +150	°C
Operating Temperature Range	T_{opr}	-40 to +85	°C
Storage Temperature Range	T_{stg}	-40 to +150	°C

(*1): When Supply voltage is less than +6V, the absolute maximum voltage is equal to the Supply voltage.

(*2): VOVP pin should be connected to VDD_HB pin.

(*3): Mounted on glass epoxy board. (101.5×114.5×1.6mm: based on EIA/JEDEC standard, 2Layers FR-4, with Exposed Pad)

(*4): Mounted on glass epoxy board. (101.5×114.5×1.6mm: based on EIA/JEDEC standard, 4Layers FR-4, with Exposed Pad)
(For 4Layers: Applying 99.5×99.5mm inner Cu area and a thermal via hole to a board based on JEDEC standard JESD51-5)

■ RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Boost Converter Block					
Supply Voltage	V_{DD_SW}	2.7	–	5.5	V
STBYb pin Voltage	V_{STBYb}	0	–	V_{DD_SW}	V
Timing Resistor	R_T	68	100	200	kΩ
Oscillating Frequency	f_{OSC}	380	700	1,000	kHz
H-Bridge Driver Block					
Supply Voltage	V_{DD_HB}	7	–	35	V
Output Switch DC Current	I_{OM}	0	20	–	mA
SHDNAb, SHDNBb pin Voltage	V_{SHDNAb} V_{SHDNBb}	0	–	V_{DD_SW}	V
IN1A, IN1B, IN2A, IN2B pin Voltage	V_{INA1} , V_{INA2} V_{INB1} , V_{INB2}	0	–	V_{DD_SW}	V
FLT pin Voltage	V_{FLT}	0	–	5.5	V

■ ELECTRICAL CHARACTERISTICS

Boost Converter Block

(Unless otherwise noted, V_{DD_SW}=V_{STBYb}=3.7V, R_T=100kΩ, Ta=25°C)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Under Voltage Lockout Block						
UVLO Release Voltage	V_{RUVLO_SW}		2.1	2.4	2.7	V
UVLO Operate Voltage	V_{DUVLO_SW}		2.0	2.2	2.5	V
UVLO Hysteresis Voltage	ΔV_{UVLO_SW}	V_{RUVLO_SW} - V_{DUVLO_SW}	–	0.2	–	V
Soft Start Block						
Soft Start Time	T_{SS}	V_B=0.95V	34	48	60	ms
Oscillator Block						
Oscillation Frequency	f_{OSC}	R_T=100kΩ	630	700	770	kHz
Oscillation Frequency deviation (Supply voltage)	f_{DV}	V_{DD_SW}=3.0V to 5.5V	–	1	–	%
Oscillation Frequency deviation (Temperature)	f_{DT}	Ta= -40°C to +85°C	–	3	–	%
Error Amplifier Block						
Reference Voltage	V_B	Short IN- and FB, Measuring IN- Pin	-1.0%	1.00	+1.0%	V
Input Bias Current	I_B	V_B=1.0V	-0.1	–	+0.1	μA
IN- pin Clamp Voltage	V_{CLIN-}	V_{STBYb}=0V, V_{DD_SW}=5.5V, I_{CLIN-}=10μA	4.8	5.2	5.6	V
RADJ pin FET ON Resistance	R_{ON_RADJ}	I_{RADJ}=10mA	–	6	12	Ω
RADJ pin FET Leak Current	I_{LEAK_RADJ}	V_{STBYb}=0V, V_{RADJ}=3.3V	–	–	1	μA
PWM Comparate Block						
Maximum Duty Cycle	$M_{AX}D_{UTY}$	V_{IN-}=0.9V	90	93	98	%
Output Block						
Switching FET ON Resistance	R_{ON_SW}	I_{SW}=100mA	–	0.6	1.2	Ω
Switching Current Limit	I_{LMT_SW}		1.5	2	–	A
Switching FET Leak Current	I_{LEAK_SW}	V_{STBYb}=0V, V_{SW}=40V	–	–	1	μA
Overvoltage Protection Block						
OVP Operate Voltage	V_{DOVP}		36	38	40	V
OVP Release Voltage	V_{ROVP}		31	33	35	V
OVP Hysteresis Voltage	ΔV_{OVP}	V_{DOVP} -V_{ROVP}	–	5	–	V
OVP pin Input Current 1	I_{OVP1}	V_{OVP}= V_{DD_HB}=35V, OVP Release	–	60	120	μA
OVP pin Input Current 2	I_{OVP2}	V_{OVP}= V_{DD_HB}=40V, OVP Operate	1,200	2,400	4,000	μA
OVP pin Leak Current	I_{OVP_LEAK}	V_{STBYb}=0V, V_{OVP}= V_{DD_HB}=40V	–	–	1	μA

■ ELECTRICAL CHARACTERISTICS

H-Bridge Driver Block

(Unless otherwise noted, V_{DD_SW}=V_{STBYb}=V_{SHDNAb}=V_{SHDNBb}=3.7V, V_{DD_HB}=25V, R_T=100kΩ, Ta=25°C)
INA1, INA2, INB1, INB2 pin, OUTA1, OUTA2, OUTB1, OUTB2 pin and SHDNAb, SHDNBb pin are common

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Under Voltage Lockout Block						
UVLO Release Voltage	V_{RUVLO_HB}		5.6	6.2	6.8	V
UVLO Operate Voltage	V_{DUVLO_HB}		5.0	5.6	6.2	V
UVLO Hysteresis Voltage	ΔV_{UVLO_HB}	V_{RUVLO_HB} - V_{DUVLO_HB}	–	0.6	–	V
Input Block						
IN pin High Voltage	V_{IHIN}		1.0	–	V_{DD_SW}	V
IN pin Low Voltage	V_{ILIN}		0	–	0.4	V
IN pin Input Current	I_{IIN}	V_{IN} = 3.3 V	–	–	1	μA
SHDNb pin High Voltage (Operating Mode)	$V_{IHSHDNb}$		1.0	–	V_{DD_SW}	V
SHDNb pin Low Voltage (Shutdown Mode)	$V_{ILSHDNb}$		0	–	0.4	V
SHDNb pin Pull-down Resistance	$R_{PDSHDNb}$	V_{SHDNb}=3.3V	210	300	390	kΩ
Output Block						
High Side SW ON Resistance	R_{DSH}	$I_{OSOURCE}$=20mA	4.0	6.0	8.0	Ω
Low Side SW ON Resistance	R_{DSL}	I_{OSINK}=20mA	4.0	6.0	8.0	Ω
High Side Over Current Detection	I_{DCTH}	High-Side	200	300	400	mA
Low Side Over Current Detection	I_{DCTL}	Low-Side	200	300	400	mA
Output Rise Time	tr	V_{IN}=0 to 3.3V	–	400	–	ns
Output Fall Time	tf	V_{IN}=0 to 3.3V	–	340	–	ns
Rise Dead Time	D_{tr}	V_{IN}=0 to 3.3V	–	200	–	ns
Fall Dead Time	D_{tf}	V_{IN}=0 to 3.3V	–	180	–	ns
Rise Delay Time	t_{d_ON}	V_{IN}=0 to 3.3V	–	310	–	ns
Fall Delay Time	t_{d_OFF}	V_{IN}=0 to 3.3V	–	270	–	ns
Input Frequency	f_{IN}		–	–	300	kHz
High Side SW OFF Leak Current	$I_{OLEAKOUTH}$	V_{STBYb}=V_{SHDNb}=0V, V_{OUT}=0V	–	–	1	μA
Low Side SW OFF Leak Current	$I_{OLEAKOUTL}$	V_{STBYb}=V_{SHDNb}=0V, V_{OUT}=25V	–	–	1	μA
OUT pin – VDD pin Potential Difference	V_{PDOV}	V_{STBYb}=V_{SHDNb}=0V, I_{ORH}=20mA	–	0.7	1.0	V
GND pin – OUT pin Potential Difference	V_{PDGO}	V_{STBYb}=V_{SHDNb}=0V, I_{ORL}=20mA	–	0.7	1.0	V

■ ELECTRICAL CHARACTERISTICS

General Characteristics

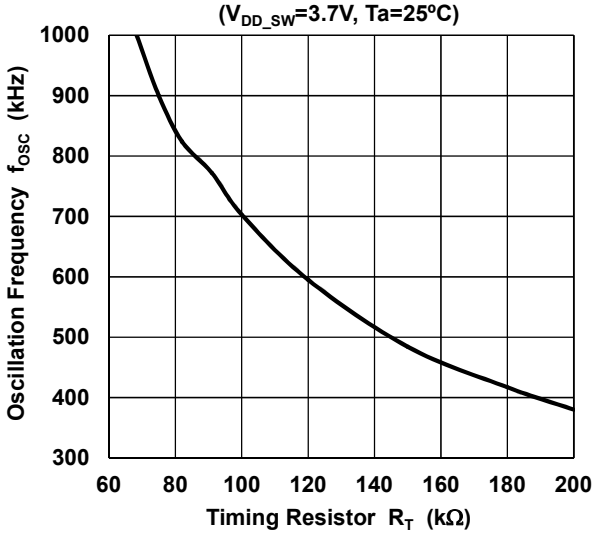
(Unless otherwise noted, V_{DD_SW}=V_{STBYb}=V_{SHDNAb}=V_{SHDNBb}=3.7V, V_{DD_HB}=25V, R_T=100kΩ, Ta=25°C)

INA1, INA2, INB1, INB2 pin, OUTA1, OUTA2, OUTB1, OUTB2 pin and SHDNAb, SHDNBb pin are common

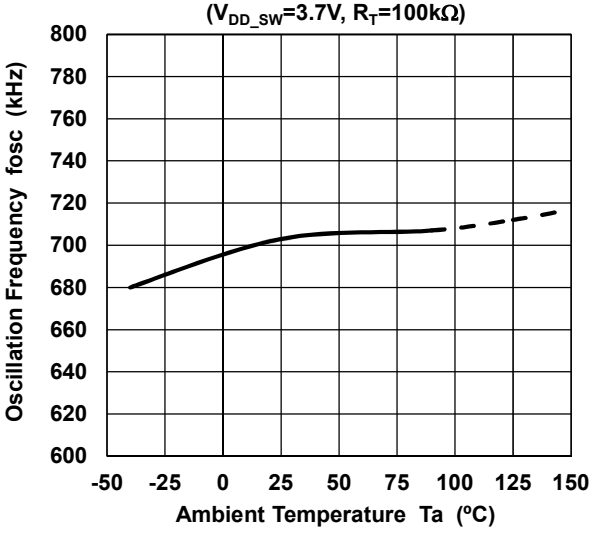
PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
STBYb pin High Voltage (Operating Mode)	$V_{IHSTBYb}$		1.0	–	V_{DD_SW}	V
STBYb pin Low Voltage (Standby Mode)	$V_{ILSTBYb}$		0	–	0.4	V
STBYb pin Pull Down Resistance	$R_{PDSTBYb}$	V_{STBYb}=3.3V	210	300	390	kΩ
FLT pin Low Level Output Voltage	V_{LFLT}	I_{FLT}=500μA	–	0.20	0.40	V
FLT pin OFF Leak Current	$I_{OLEAKFLT}$	V_{FLT}=5.5V	–	–	1	μA
Quiescent Current (Switching Regulator Block)	I_{QSW}	No Load	–	1.9	2.8	mA
Quiescent Current (H-Bridge Driver Block)	I_{QHB}	f_{INA}= f_{INB}=10kHz antiphase 50% Duty Cycle	–	1.0	2.0	mA
Quiescent Current (Standby)	I_{QSTBY}	V_{STBYb}=V_{SHDNb}=0V V_{DD_HB}=0V,	–	1.6	3.6	μA

■ TYPICAL CHARACTERISTICS (Boost Converter Block)

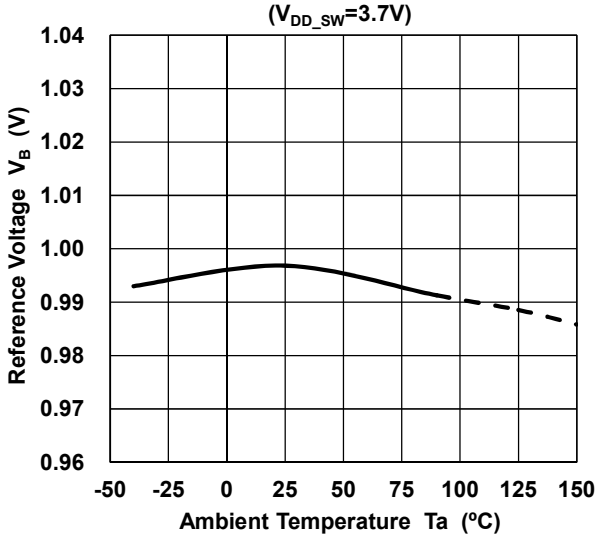
Oscillation Frequency vs. Timing Resistor
(V_{DD_SW}=3.7V, Ta=25ºC)



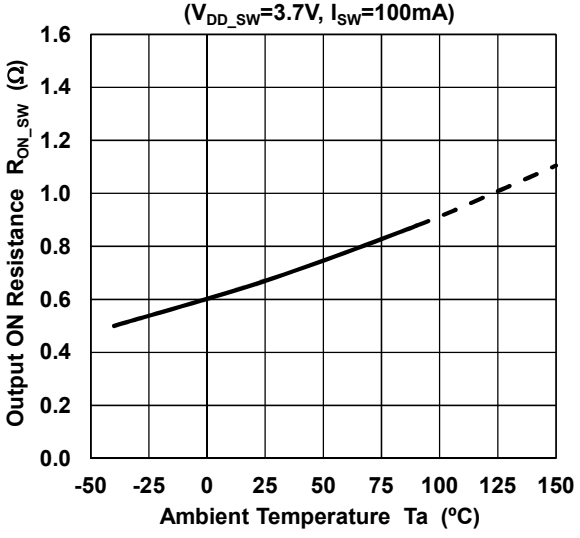
Oscillation Frequency vs. Temperature
(V_{DD_SW}=3.7V, R_T=100kΩ)



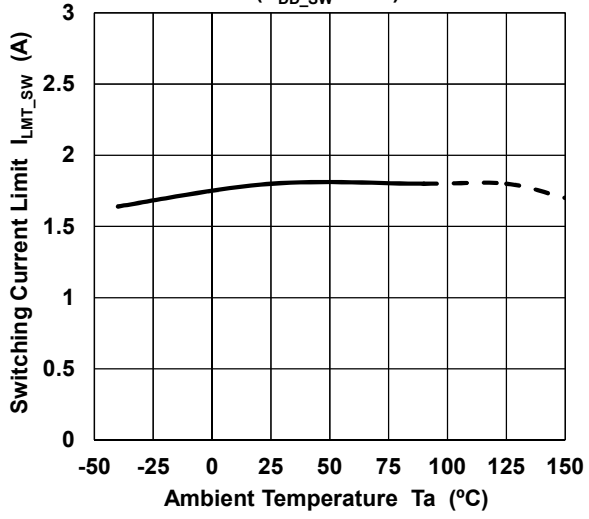
Reference Voltage vs. Temperature
(V_{DD_SW}=3.7V)



Output ON Resistance vs. Temperature
(V_{DD_SW}=3.7V, I_{SW}=100mA)

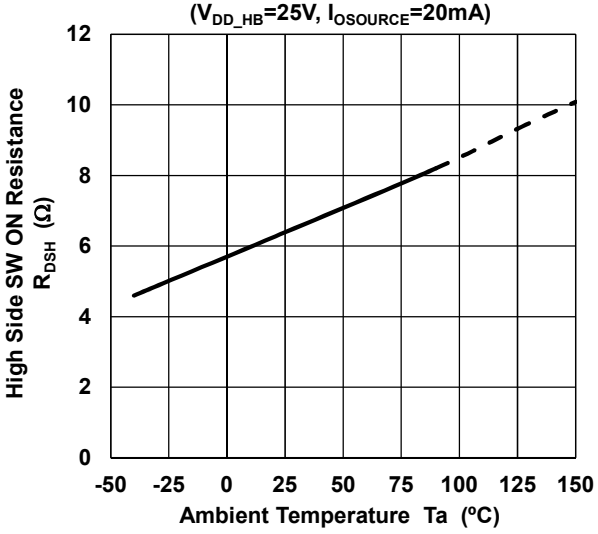


Switching Current Limit vs. Temperature
(V_{DD_SW}=3.7V)

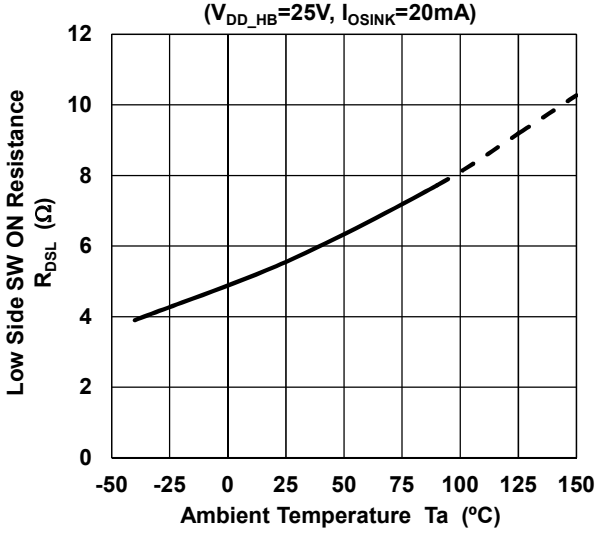


■ TYPICAL CHARACTERISTICS (H-Bridge Driver Block)

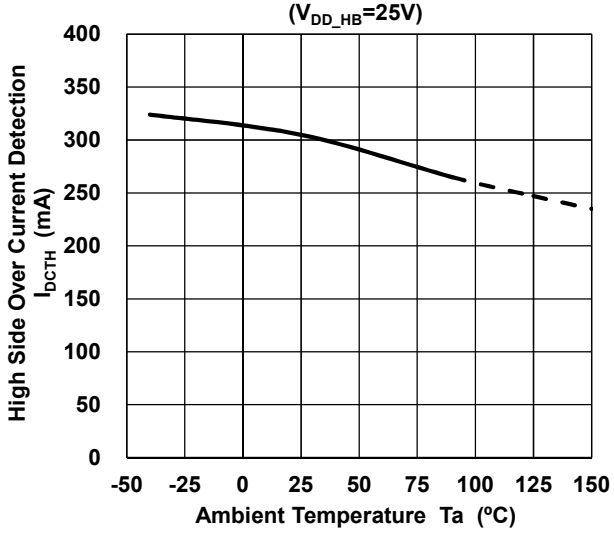
High Side SW ON Resistance vs. Temperature
(V_{DD_HB}=25V, $I_{OSOURCE}$=20mA)



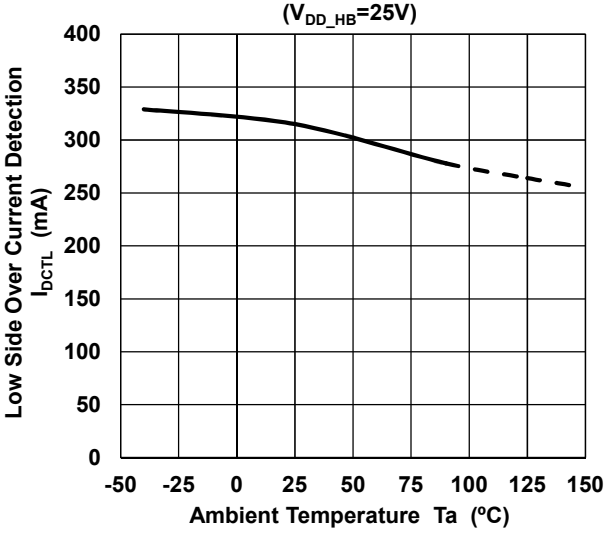
Low Side SW ON Resistance vs. Temperature
(V_{DD_HB}=25V, I_{OSINK}=20mA)



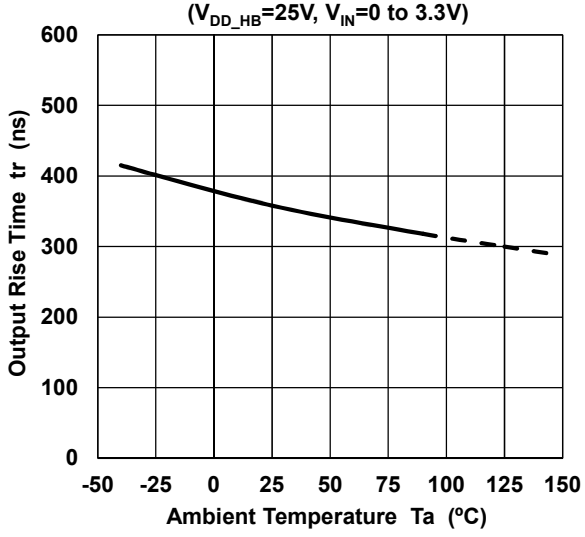
High Side Over Current Detection vs. Temperature
(V_{DD_HB}=25V)



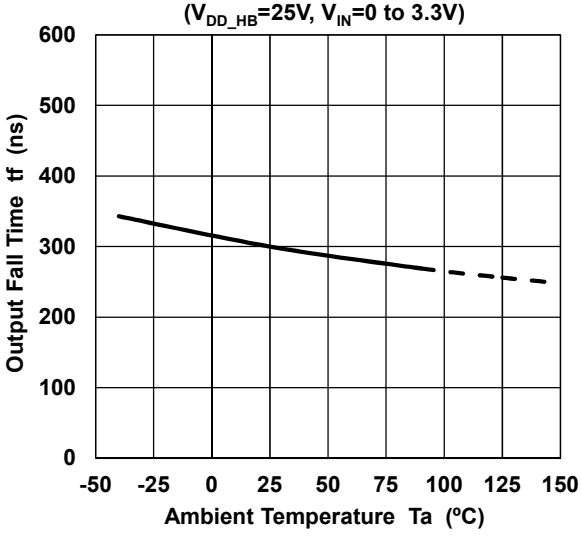
Low Side Over Current Detection vs. Temperature
(V_{DD_HB}=25V)



Output Rise Time vs. Temperature
(V_{DD_HB}=25V, V_{IN}=0 to 3.3V)

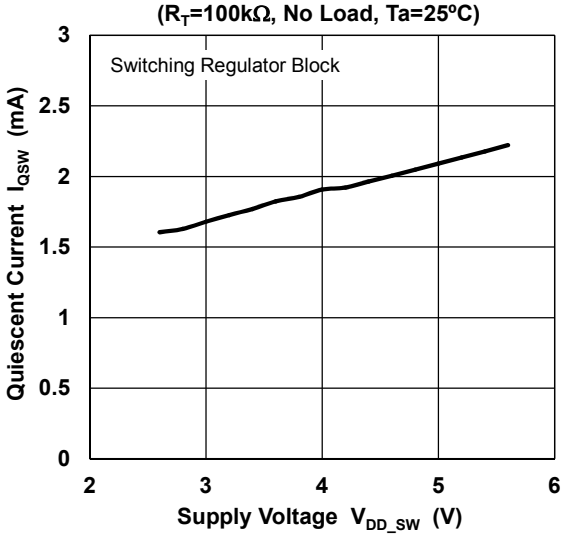


Output Fall Time vs. Temperature
(V_{DD_HB}=25V, V_{IN}=0 to 3.3V)

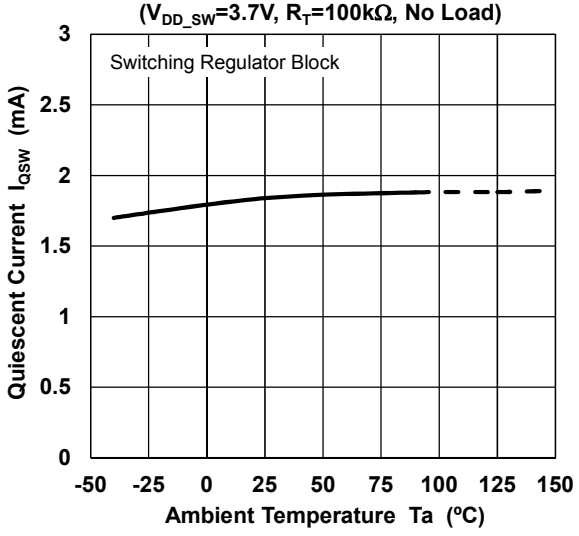


■ TYPICAL CHARACTERISTICS (General Characteristics)

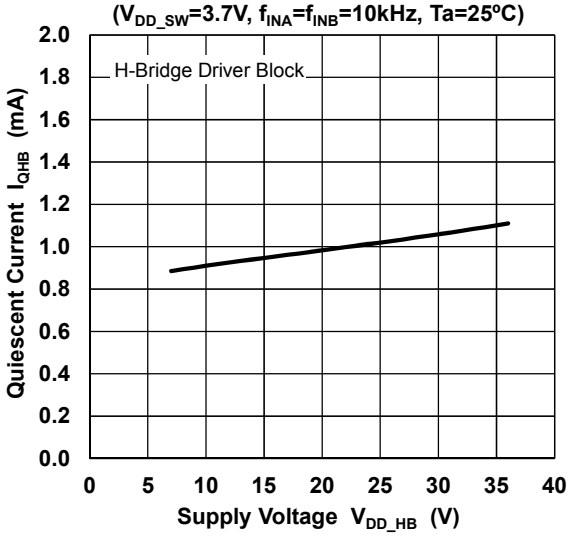
Quiescent Current vs. Supply Voltage
(R_T=100kΩ, No Load, Ta=25ºC)



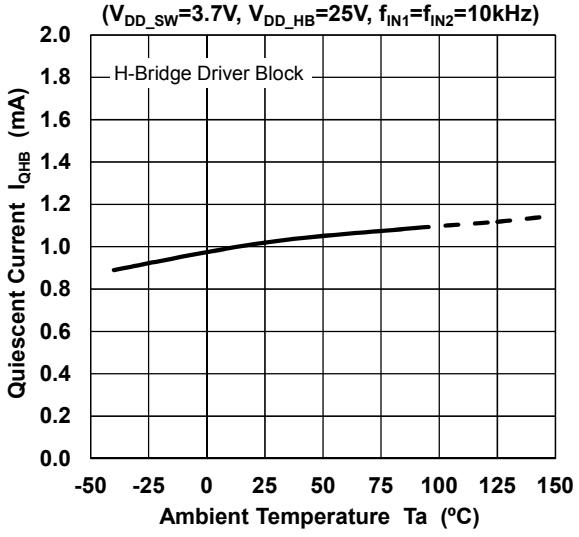
Quiescent Current vs. Temperature
(V_{DD_SW}=3.7V, R_T=100kΩ, No Load)



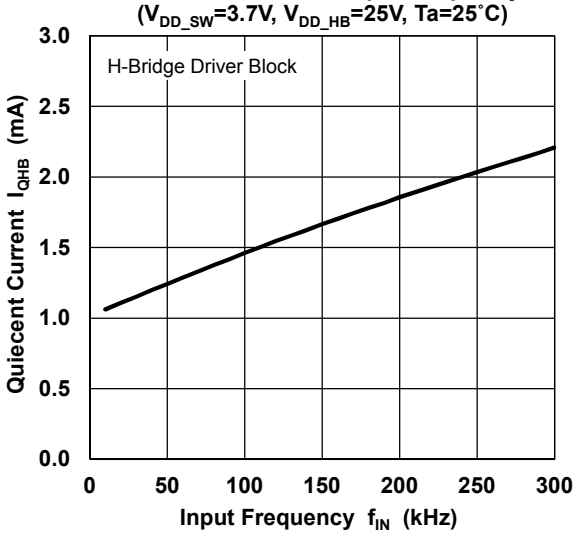
Quiescent Current vs. Supply Voltage
(V_{DD_SW}=3.7V, f_{INA}=f_{INB}=10kHz, Ta=25ºC)



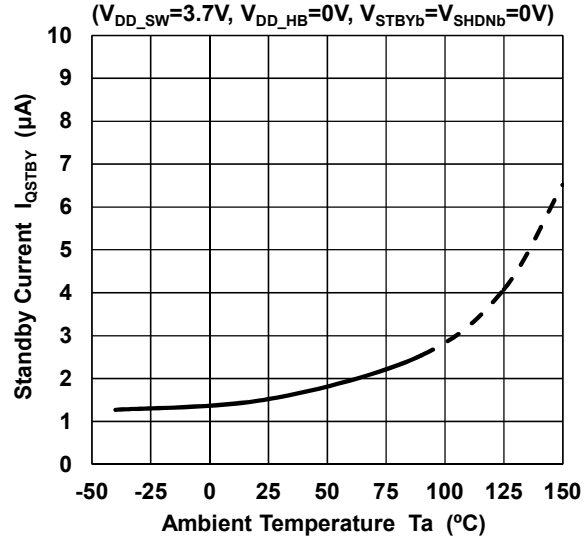
Quiescent Current vs. Temperature
(V_{DD_SW}=3.7V, V_{DD_HB}=25V, f_{IN1}=f_{IN2}=10kHz)



Quiecent Current vs. Input Frequency
(V_{DD_SW}=3.7V, V_{DD_HB}=25V, Ta=25˚C)



Standby Current vs. Temperature
(V_{DD_SW}=3.7V, V_{DD_HB}=0V, V_{STBYb}=V_{SHDNb}=0V)



■ H-Bridge Driver Block Pin Operation Table

Ach

INPUT			OUTPUT	
SHDNAb	INA1	INA2	OUTA1	OUTA2
Low	*	*	Hi-Z	Hi-Z
High	Low	*	Low	*
High	High	*	High	*
High	*	Low	*	Low
High	*	High	*	High

* Don't Care

Bch

INPUT			OUTPUT	
SHDNBb	INB1	INB2	OUTB1	OUTB2
Low	*	*	Hi-Z	Hi-Z
High	Low	*	Low	*
High	High	*	High	*
High	*	Low	*	Low
High	*	High	*	High

* Don't Care

■ Timing Chart

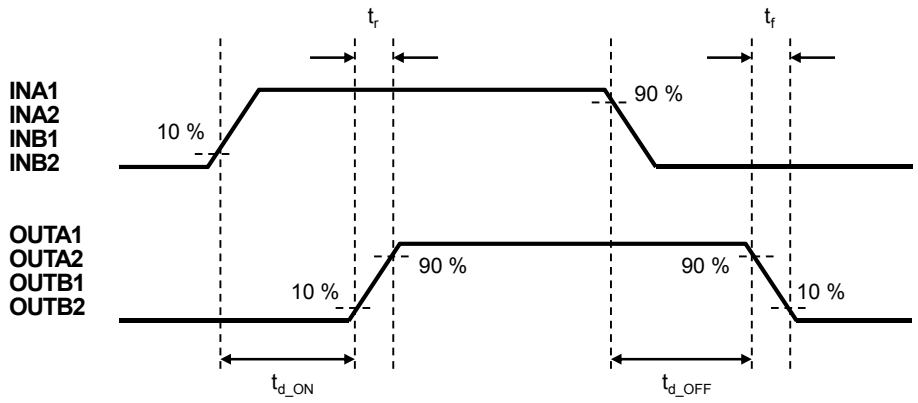


Fig. 1. Output Rise/Fall Time, Rise/Fall Delay Time

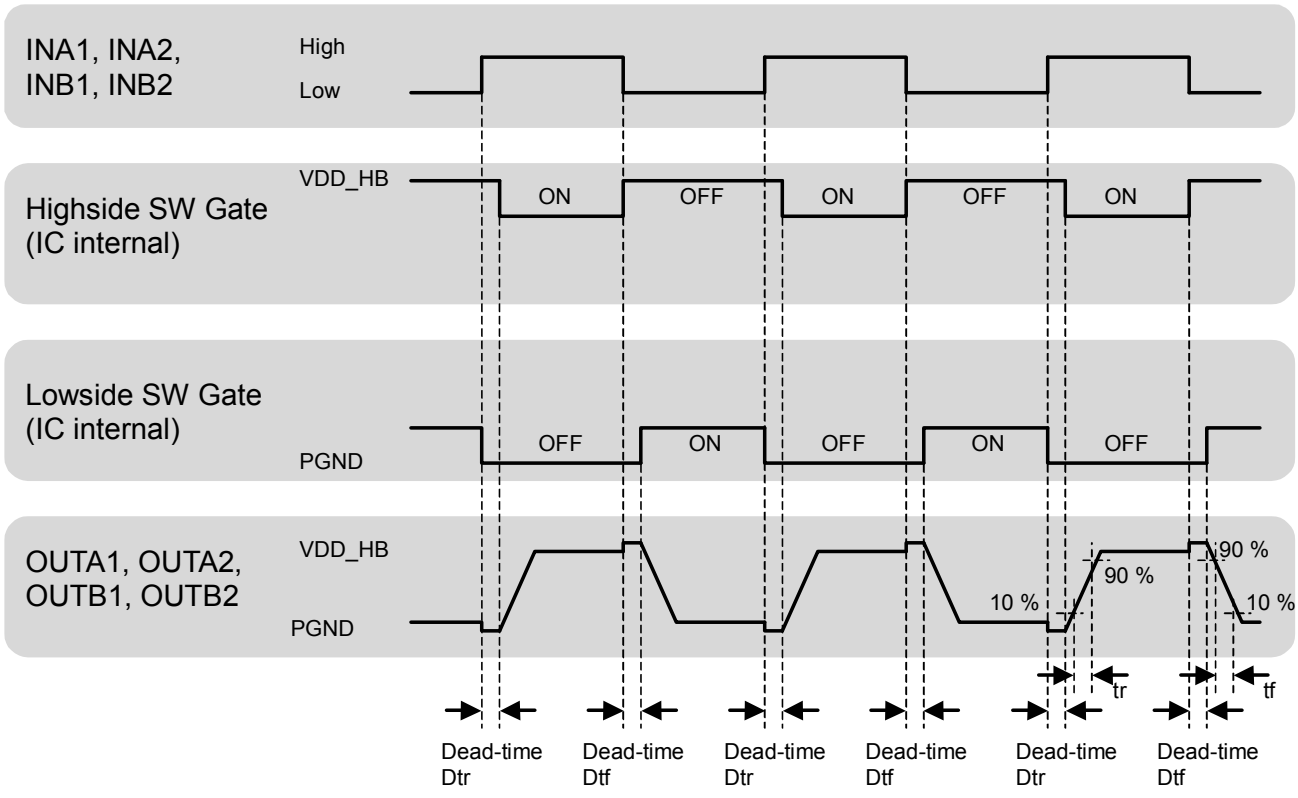


Fig. 2. H-Bridge Driver Block

■ PIN DESCRIPTIONS

PIN NAME	PIN NUMBER	FUNCTION
IN-	1	Output Voltage Detecting pin. Connects output voltage through the resistor divider tap to this pin in order to voltage of the IN- pin become 1.0V (typ.).
VDD_SW	2	Power Supply pin for SW.REG. block. Insert a bypass capacitor close to the VDD_SW pin – the GND pin connection in order to lower high frequency impedance.
STBYb	3	Standby Control pin. The STBYb pin is pulled down with 300kΩ (typ.) internally. Normal Operation at the time of High Level. Standby Mode at the time of Low Level or OPEN.
SHDNAb	4	Shutdown Control pin for H-Bridge driver Ach. The SHDNAb pin is pulled down with 300kΩ (typ.) internally. Normal Operation at the time of High Level. The FET of H-Bridge driver Ach becomes OFF (Hi-Z) by Low Level or OPEN.
SHDNBb	5	Shutdown Control pin for H-Bridge driver Bch. The function is same as 4pin.
INA1	6	Control input pin for H-Bridge driver Ach (one side). High Side SW Operation at the time of High Level. Low Side SW Operation at the time of Low Level.
INA2	7	Control input pin for H-Bridge driver Ach (one side). The function is same as 6pin.
INB1	8	Control input pin for H-Bridge driver Bch (one side). The function is same as 6pin.
INB2	9	Control input pin for H-Bridge driver Bch (one side). The function is same as 6pin.
FLT	10	FLT pin outputs a signal at the time of abnormality. You should be connected to the outside power supply through pull up resistance. Normally: FET is OFF (Output voltage High Level) Abnormality: FET is ON (Output voltage Low Level)
PGND	11	Power GND pin for H-Bridge driver (Note 1)
OUTA2	12	Output pin of H-Bridge driver Ach (one side). The output current is limited to 300mA (typ.) by the overcurrent protection function.
OUTA1	13	Output pin of H-Bridge driver Ach (one side). The function is same as 12pin.
PGND	14	Power GND pin for H-Bridge driver (Note 1)
OUTB1	15	Output pin of H-Bridge driver Bch (one side). The function is same as 12pin.

■ PIN DESCRIPTIONS (Continued)

PIN NAME	PIN NUMBER	FUNCTION
VDD_HB	16	Power Supply pin for H-Bridge driver block. Insert a bypass capacitor close to the VDD_HB pin – the GND pin connection in order to lower high frequency impedance.
VOVP	17	Overvoltage detection pin of SW.REG. When it detected overvoltage, the VOVP pin sinks a current and discharges the output voltage. VOVP pin should be connected to VDD_HB pin.
OUTB2	18	Output pin of H-Bridge driver Bch (one side). The function is same as 12pin.
SW	19	Switch Output pin for SW.REG. Power MOSFET
PGND	20	Power GND pin for SW.REG. (Note 1)
RADJ	21	The RADJ pin becomes the high impedance at standby. It prevents a current flowing into the output voltage setting resistor.
FB	22	Feedback Setting pin The feedback resistor and capacitor are connected between the FB pin and the IN- pin.
RT	23	Oscillating Frequency Setting pin by Timing Resistor. Oscillating Frequency should set between 380kHz and 1MHz.
GND	24	GND pin (Note 1)
Exposed PAD	–	Connect to GND.

(Note 1) GND and PGND are connected inside.

■ H Bridge Driver Block Over Current Protection

The overcurrent protection function operates when the high side SW current flows more than I_{DCTH} or the low side SW current flows more than I_{DCTL}. The overcurrent protection operates in three steps.

(1) Sensing step

·Turn off power MOSFET of the switching regulator
·Turn off power MOSFET of the H-bridge driver
·Reset a soft start
·Reset an FB pin voltage
·Connect a dummy road between VOVP pin-GND pin

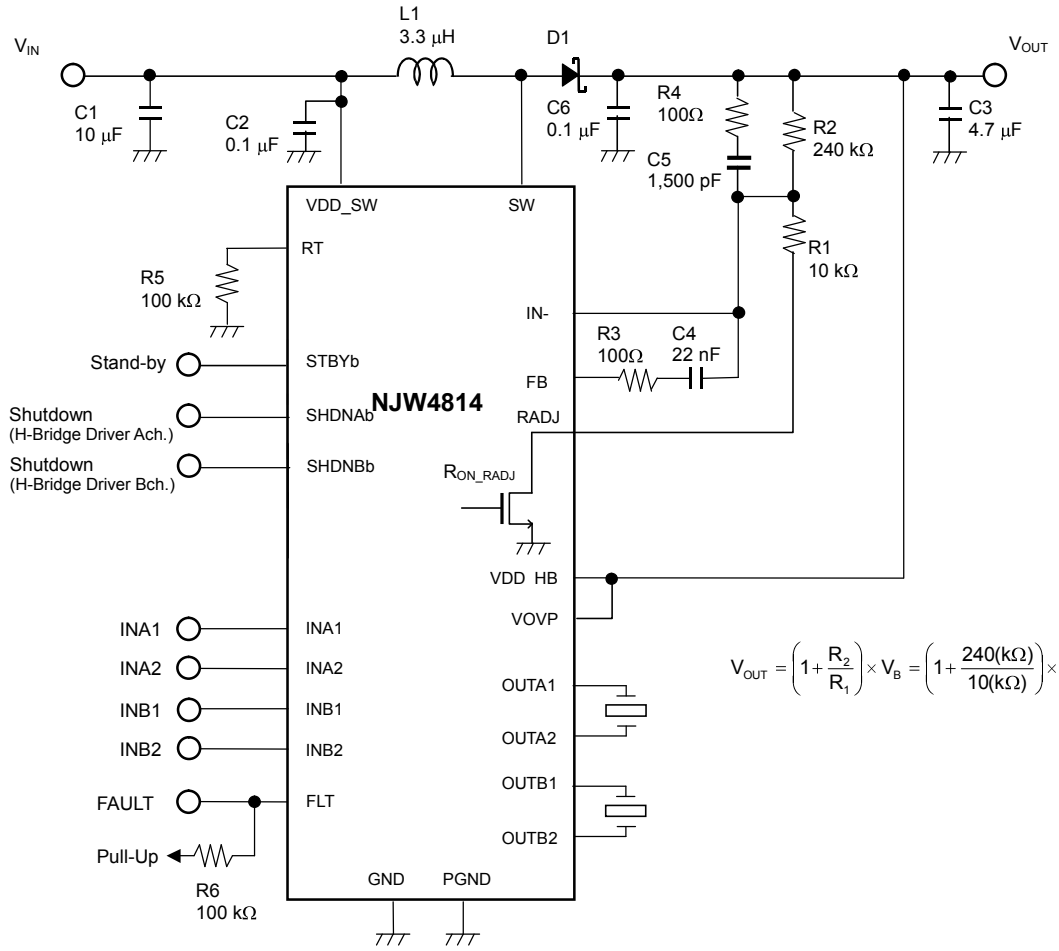
(2) Output stop step

After the overcurrent detection, 500 ms (typ.) continues an output stop.

(3) Return step

After an output stop, the soft start operates. Then the IC operation shifts to normal operation.

■ APPLICATION EXAMPLE



$$V_{OUT} = \left(1 + \frac{R_2}{R_1}\right) \times V_B = \left(1 + \frac{240(k\Omega)}{10(k\Omega)}\right) \times 1(V) = 25.0(V)$$