GENLINX™ GS9000C
Serial Digital Decoder

DATA SHEET

FEATURES

- **fully compatible with SMPTE 259M**
- **decodes 8 and 10 bit serial digital signals for data rates to 370Mb/s**
- **pin and function compatible with GS9000S, GS9000 and GS9000B**
- **325mW power dissipation at 270MHz clock rates**
- **incorporates an automatic standards selection**
- **function with the GS9005A Receiver or GS9015A Reclocker**
- **Pb-free and Green**
- **operates from single +5 or -5 volt supply**
- **enables an adjustment-free Deserializer system when used with GS9010A and GS9005A or GS9015A**
- **28 pin PLCC packaging**

APPLICATIONS

- $4f_{SC}$, 4:2:2 and 360Mb/s serial digital interfaces
- Automatic standards select controller for serial routing and distribution applications using GS9005A Receiver or GS9015A Reclocker

DEVICE DESCRIPTION

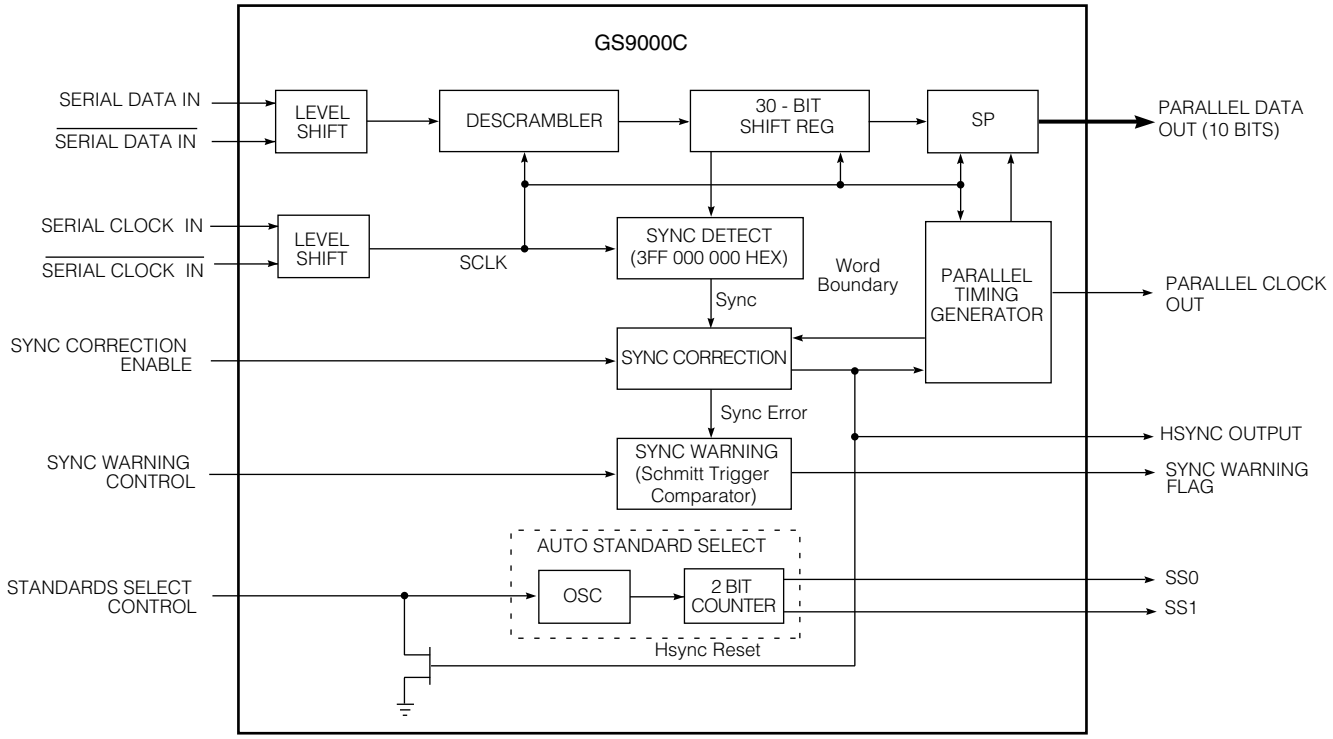
The GS9000C is a CMOS integrated circuit specifically designed to deserialize SMPTE 259M serial digital signals at data rates to 370Mb/s.

The device incorporates a descrambler, serial to parallel convertor, sync processing unit, sync warning unit and automatic standards select circuitry.

Differential pseudo-ECL inputs for both serial clock and data are internally level shifted to CMOS levels. Digital outputs such as parallel data, parallel clock, HSYNC, Sync Warning and Standard Select are all TTL compatible.

The GS9000C is designed to directly interface with the GS9005A Reclocking Receiver to form a complete SMPTE-serial-in to CMOS level parallel-out deserializer. The GS9000C may also be used with the GS9010A and the GS9005A to form an adjustment-free receiving system which automatically adapts to all serial digital data rates. The GS9015A can replace the GS9005A in GS9000C applications where cable equalization is not required.

The GS9000C is packaged in a 28 pin PLCC and operates from a single 5 volt, ±5% power supply.



FUNCTIONAL BLOCK DIAGRAM

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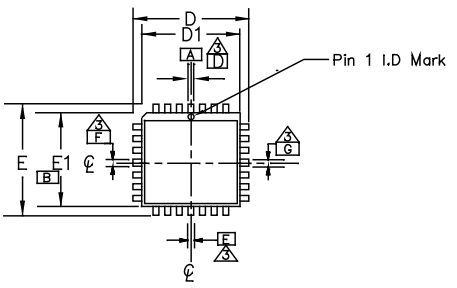
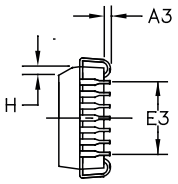
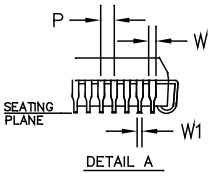
PACKAGE OUTLINE DRAWING







SYMBOL	28 PLCC	
	MIN	MAX
A	0.165	0.180
A1	0.090	0.120
A3	0.020	0.040
D	0.485	0.495
D1	0.450	0.456
D3	0.300 REF	
E	0.485	0.495
E1	0.450	0.456
E3	0.300 REF	
H	0.042	0.048
P	0.050 BSC	
R	0.025	0.045
W	0.026	0.032
W1	0.013	0.021

NOTE:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ANSI Y14.5M-1982.
2. DATUM PLANE [H] LOCATED AT TOP OF LEAD AND IS COINCIDENT WITH THE LEAD EXITS THE PLASTIC BODY AT THE TOP OF THE PARTING LINE.
3. DATUM [D-E] AND [F-G] TO BE DETERMINED AT DATUM PLANE [H].
4. DIMENSION D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION ALLOWABLE PROTRUSION IS 0.010 PER SIDE DIMENSION D1 AND E1 DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE [H].
5. DETAILS OF PIN NO.1 IDENTIFICATION ARE OPTIONAL BUT LOCATED WITHIN THE ZONE INDICATED.
6. DATUM [A] AND [B] TO BE DETERMINED AT PLANE [H].

GS9000C DECODER - DC ELECTRICAL CHARACTERISTICS

V_{DD} = 5V, T_A = 0°C to 70°C unless otherwise shown

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES	TEST LEVEL
Supply Voltage	V_S	Operating range	4.75	5.00	5.25	V		1
Power Consumption (outputs unloaded)	P_C	f = 143MHz	-	235	-	mW		7
		f = 270MHz	-	325	-	mW		7
		f = 360MHz	-	385	-	mW		1
CMOS Input Voltage	VIH_{MIN}	T_A = 25°C	3.4	-	-	V		1
	VIL_{MAX}		-	-	1.5	V		1
Output Voltage	VOH_{MIN}	I_{OH} = 4mA, 25°C	2.4	4.5	-	V		1
	VOH_{MAX}	I_{OL} = 4mA, 25°C	-	0.2	0.5	V		1
Input Leakage Current	I_{IN}	V_{IN} = V_{DD} or V_{SS}	-	-	±10	µA		1
Serial Clock and Data Inputs Signal Swing	V_{IN}	T_A = 25°C	700	800	1200	mVpp		1
Signal Offset	V_{INOS}	T_A = 25°C, V_{IN} = 700 to 1000mVpp	3.0	-	4.05	V	Centre of Swing	1

TEST LEVELS

1. Production test at room temperature and nominal supply voltage with guardbands for supply and temperature ranges.
2. Production test at room temperature and nominal supply voltage with guardbands for supply and temperature ranges using correlated test.
3. Production test at room temperature and nominal supply voltage.
4. QA sample test.
5. Calculated result based on Level 1,2, or 3.
6. Not tested. Guaranteed by design simulations.
7. Not tested. Based on characterization of nominal parts.
8. Not tested. Based on existing design/characterization data of similar product.

V_{DD} = 5V, T_A = 0°C to 70°C unless otherwise shown

Serial Input Clock Frequency	f_{SCI}		100	-	370	MHz		1
Serial Input Data Rate	DR_{SDI}		100	-	370	Mb/s		1
Serial Data and Clock Inputs:		T_A = 25°C						
Risetime	t_R		-	600	-	ps		7
Setup	t_{SU}		1.0	-	-	ns		7
Hold	t_{HOLD}		1.0	-	-	ns		7
Parallel Clock: Jitter	t_{JCLK}	T_A = 25°	-	1.0	-	ns p-p		7
Parallel Data: Risetime and Falltime	t_{R-PDn}	T_A = 25°C, C_L = 10pF	-	3	-	ns	20% to 80%	7
PDn to PCLK Delay Tolerance	t_D		-	-	±3	ns	Rising edge of PCLK to bit period centre	7

TEST LEVELS

1. Production test at room temperature and nominal supply voltage with guardbands for supply and temperature ranges.
2. Production test at room temperature and nominal supply voltage with guardbands for supply and temperature ranges using correlated test.
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	PACKAGE	TEMPERATURE	Pb-FREE AND GREEN
GS9000CCPJ	28 Pin PLCC	0°C to 70°C	No
GS9000CCTJ	28 Pin PLCC Tape	0°C to 70°C	No
GS9000CCPJE3	28 Pin PLCC	0°C to 70°C	Yes
GS9000CCTJE3	28 Pin PLCC Tape	0°C to 70°C	Yes

ABSOLUTE MAXIMUM RATINGS

	+ 0.3)
DC Input Current (any one input)	±10µA
Operating Temperature Range	0°C to 70°C
Storage Temperature Range	-65°C to +150C
Lead Temperature (Soldering, 10 seconds)	260°C

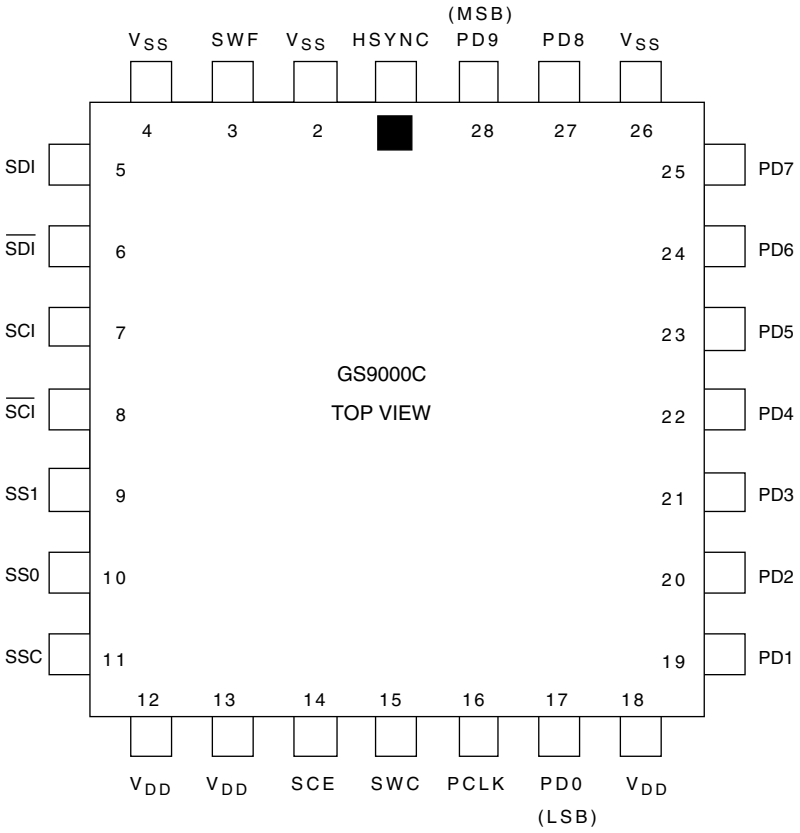


Fig. 1 GS9000C Pin Outs, 28 Pin PLCC Package

PIN NO.	SYMBOL	TYPE	DESCRIPTION
			Horizontal Sync Output.
			Power Supply
			Power Supply
			Differential, pseudo-ECL serial data inputs
			Differential, pseudo-ECL serial clock inputs.
			Standard Select Outputs
			Standards Select Control
			Power Supply
			Power Supply

PIN NO.	SYMBOL	TYPE	DESCRIPTION
			Sync Correction Enable not resetting the GS9000Cís internal parallel timing on the first sync error. If the next incoming sync is in error, internal parallel timing will be reset. This is to guard against spurious HSYNC errors. When SCE is low, a valid sync will always reset the GS9000Cís parallel timing generator
15	SWC	Input	Sync Warning Control
			Parallel Clock Output.
			Parallel Data Output - Bit 0 (LSB)
			Power Supply.
			Parallel Data Outputs - Bit 1 to Bit 7.
			Power Supply
			Parallel Data Output.
			Parallel Data Output - Bit 9 (MSB)

INPUT/OUTPUT CIRCUITS

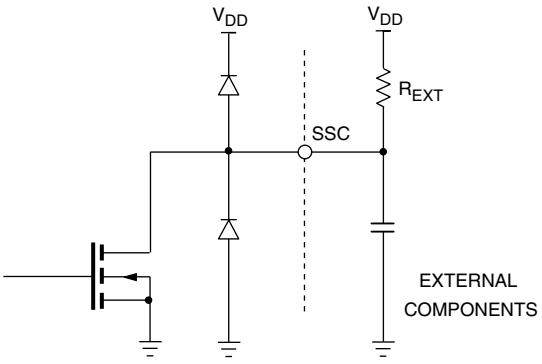


Fig. 2 Pin 11 SSC

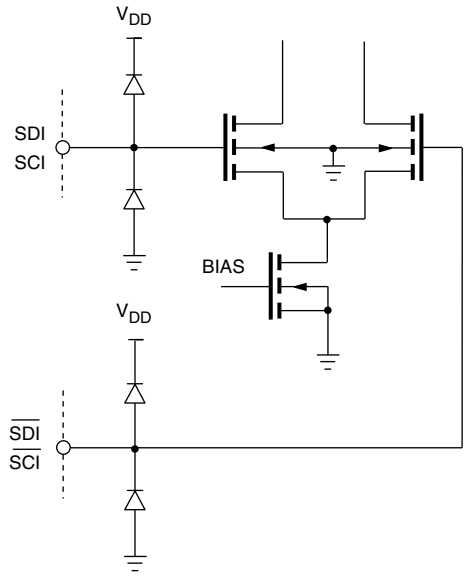


Fig. 4 Pins 5 - 8 SDI - SCI

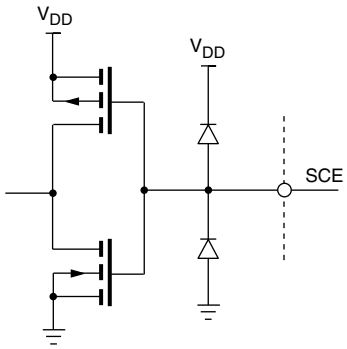


Fig. 3 Pin 14 SCE

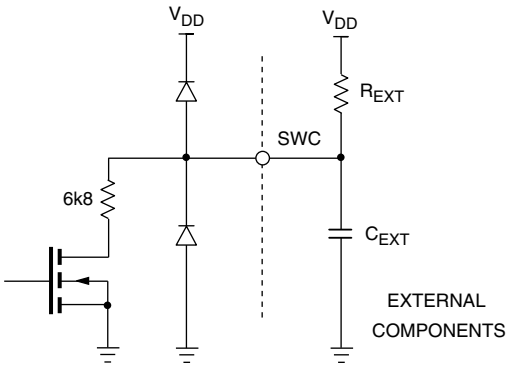


Fig. 5 Pin 15 SWC

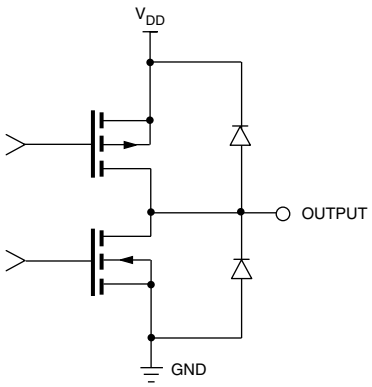


Fig. 6 Pins 3, 16, 17, 19 - 25, 27, 28
SWF, HSYNC, SSI, SSD, PCLK, PD0-9

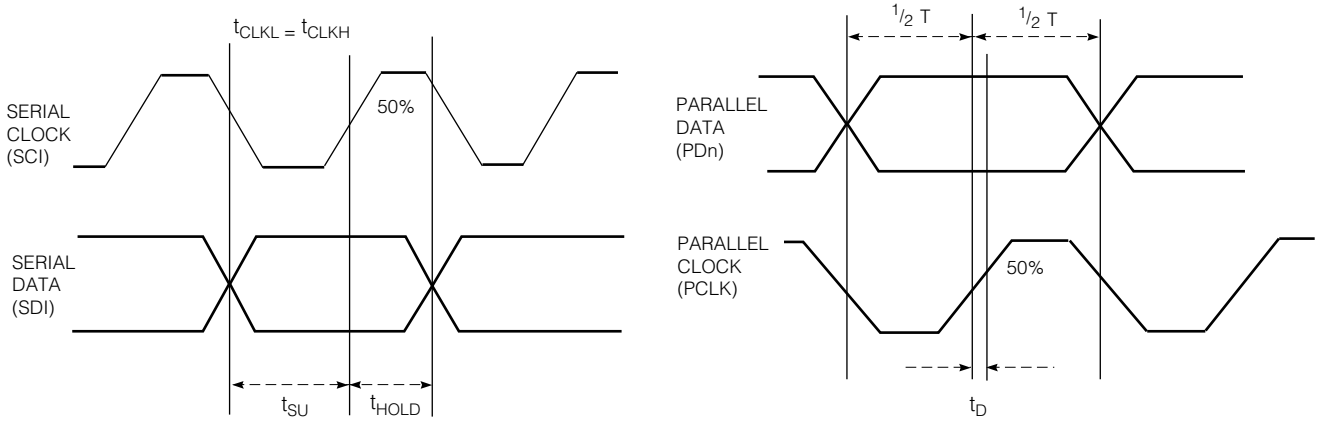


Fig. 7 Waveforms

TEST SET-UP & APPLICATION INFORMATION

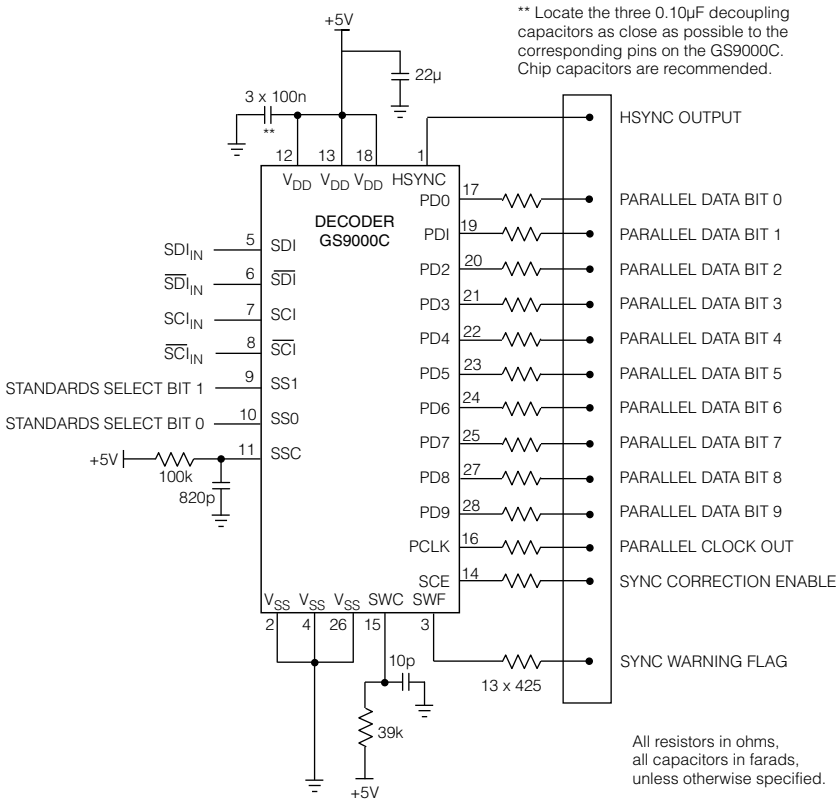
Figure 8 shows the test set-up for the GS9000C operating from a V_{DD} supply of +5 volts. The differential pseudo ECL inputs for DATA and CLOCK (pins 5,6,7 and 8) must be biased between +3.0 and +4.0 volts. In the application circuit shown in Figure 11, these inputs can be directly driven from the outputs of the GS9005A Reclocking Receiver with their resistor values set as shown.

In other cases, such as true ECL level driver outputs, two biasing resistors are needed on the DATA and CLOCK inputs and the signals must be AC coupled.

It is critical that the decoupling capacitors connected to pins 12,13 and 18 are chip types and are located as close as possible to the device pins.

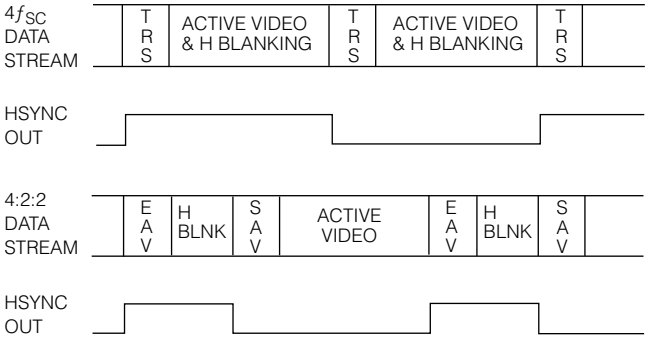
The critical high speed inputs, such as Serial Data (pins 5 and 6) and Serial Clock (pins 7 and 8), are located along one side of the device package to maintain very short interconnections when interfacing with the GS9005A Receiver.

If the automatic standard select function is not used, the Standard Select bits (pins 9 and 10) do not need to be connected, however the control input (pin 11) should be grounded.



With synchronized serial data and clock connected to the GS9000C, the HSYNC output (pin 1) will toggle for each HSYNC detected. The Parallel Data bits PD0 through PD9 and the Parallel Clock can be observed on an oscilloscope or fed to a logic analyzer. To directly drive parallel inputs to receiving equipment, such as monitors or digital to analog converters, these outputs can be fed through a suitable TTL to ECL converter.

In operation, the HSYNC output from the GS9000C decoder toggles on each occurrence of the timing reference signal (TRS). The state of the HSYNC output is not significant, but the time at which it toggles is significant.



The HSYNC output toggles to indicate the presence of the TRS on the falling edge of PCLK, one data symbol prior to the output of the first word in the TRS. In the following diagram, data is indicated in 10-bit Hex.

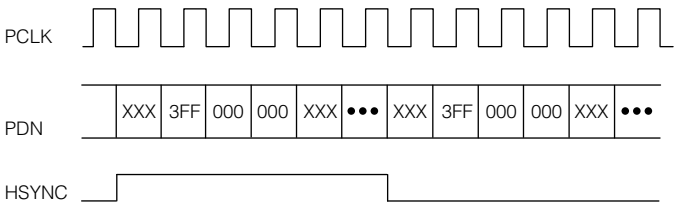
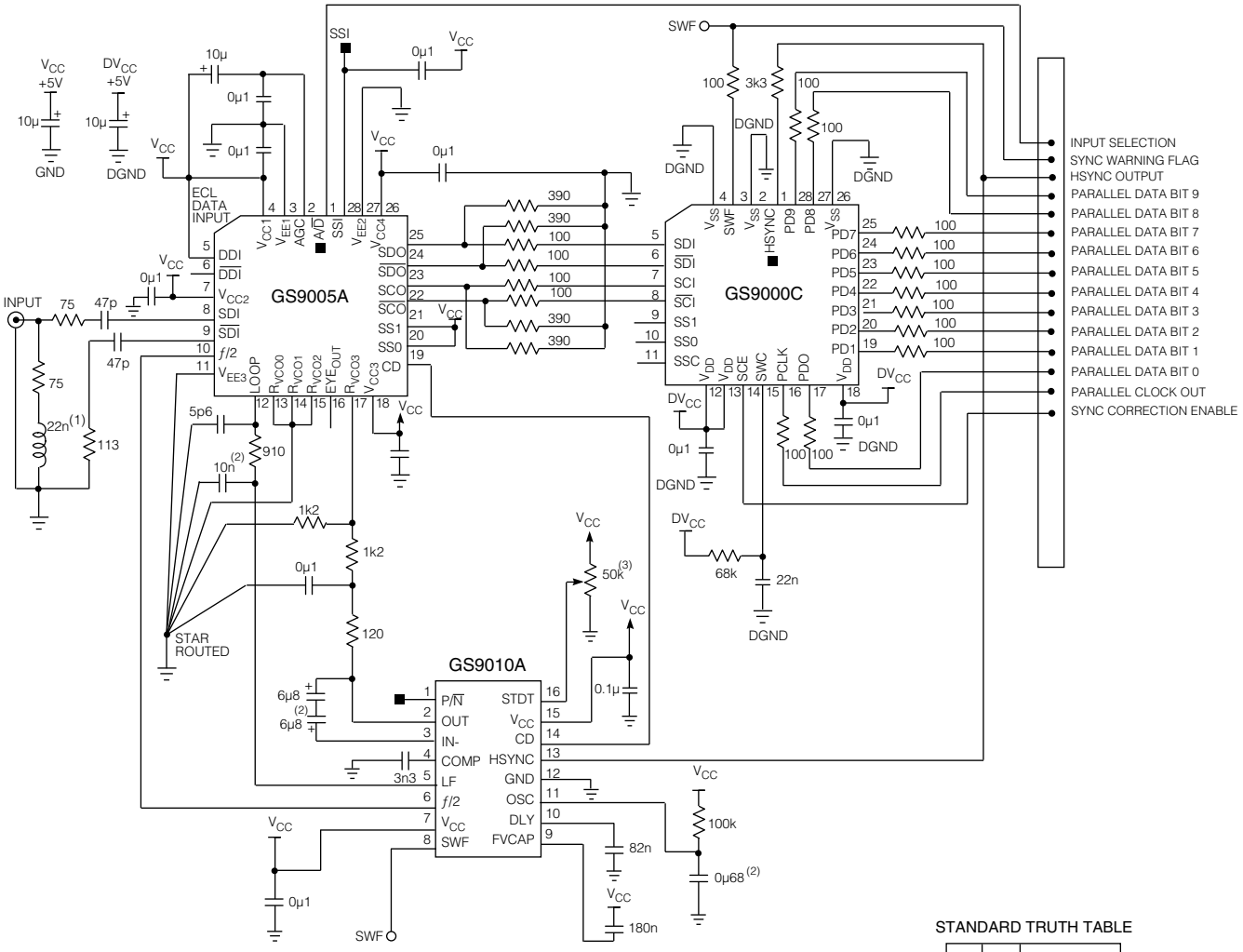


Fig. 10 Operation of HSYNC with Respect to PCLK

TYPICAL APPLICATION CIRCUIT - Adjustment Free Multi-standard Serial To Parallel Convertor

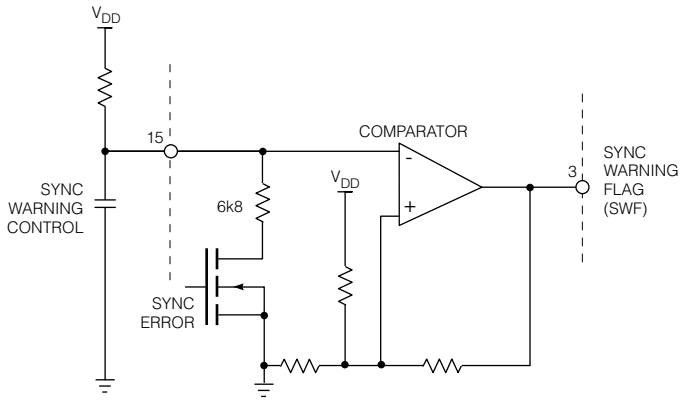


STANDARD TRUTH TABLE

f/2	P/$\overline{N}$	STANDARD
0	0	4:2:2 - 270
0	1	4:2:2 - 360
1	0	4*f*sc - NTSC
1	1	4*f*sc - PAL

(1) Typical value for input return loss matching
(2) To reduce board space, the two anti-series 6.8µF capacitors (connected across pins 2 and 3 of the GS9010A) may be replaced with a 1.0µF non-polarized capacitor provided that
(a) the 0.68µF capacitor connected to the OSC pin (11) of the GS9010A is replaced with a 0.33µF capacitor and
(b) the GS9005A /15A Loop Filter Capacitor is 10nF.
(3) Remove this potentiometer if P/N function is not required, and ground pin 16 of the GS9010A.

GS9000C, GS9005A and GS9010A INTERCONNECTIONS



Genlinx™ GS9000 series of devices are Serial Digital Decoders for the SMPTE-259M Standard. They all perform Serial to Parallel Conversion, Sync Detection, Parallel Word Alignment and Parallel Clock Generation. The three devices are in identical packages and are pin for pin compatible.

The table below highlights the small differences in the devices.

TABLE 1: Differences Between Devices

$_{CC}$ = 5.0V, T_A=25°C (unless otherwise shown)

			GS9000SCPJ	GS9000BCPJ	GS9000CCPJ
Power Consumption	P_D	D.R. = 270Mb/s	350mW	350mW	325mW
Maximum Serial Input Data Rate	D.R.		300Mb/s	370Mb/s	370Mb/s
Static Output Current of Parallel Outputs* (Maximum)	$I_{OUT-MAX}$		32mA	32mA	12mA
Static Output Voltage of Parallel Outputs (typical)	(VOH_{MIN} and VOL_{MAX})	I_{OH} = 4mA	4.5V and 0.2V	4.5V and 0.2V	4.5V and 0.2V
Static Output Voltage of Parallel Outputs (Worst Case)		$I_{OH} = I_{OUT-MAX}$	2.4V and 0.5V	2.4V and 0.5V	2.4V and 0.5V
Slew Rate of Parallel Outputs	S.R.	C_L = 10pF	3V/ns	3V/ns	1V/ns

*the lower drive current reduces the noise generated by these outputs.

CAUTION

DO NOT OPEN PACKAGES OR HANDLE
EXCEPT AT A STATIC-FREE WORKSTATION

DOCUMENT IDENTIFICATION

The product is in production. Gennum reserves the right to make changes at any time to improve reliability, function or design, in order to provide the best product possible.

REVISION NOTES:

NOVEMBER 2007 - VERSION 4
ADDED PACKAGE OUTLINE DRAWING (ECR #148310)

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