

μ PA2812T1L

P-channel MOS FIELD EFFECT TRANSISTOR

RK-UD-11-0117 Rev.1.00 Apr 18, 2012

Description

The μ PA2812T1L is P-channel MOS Field Effect Transistor designed for DC/DC converter and power management applications of portable equipment.

Features

- $V_{DSS} 30 \text{ V } (T_A = 25^{\circ}\text{C})$
- Low on-state resistance
 - --- R_{DS(on)} = 4.8 mΩ MAX. (V_{GS} = -10 V, I_D = -30 A)
- 4.5 V Gate-drive available
- Small & thin type surface mount package with heat spreader (8-pin HVSON)
- Pb-free and Halogen free

Ordering Information

Part No.	LEAD PLATING	PACKING	Package	
μ PA2812T1L-E1-AT	Pure Sn Tape 3000 p/reel		8-pin HVSON (3333)	
μ PA2812T1L-E2-AT			typ. 0.028 g	

Absolute Maximum Ratings (T_A = 25°C)

Item	Symbol	Ratings	Unit
Drain to Source Voltage (V _{GS} = 0 V)	V _{DSS}	-30	V
Gate to Source Voltage (V _{DS} = 0 V)	V _{GSS}	±20	V
Drain Current (DC) (T _C = 25°C)	I _{D(DC)}	±30	Α
Drain Current (pulse) *1	I _{D(pulse)}	±120	Α
Total Power Dissipation *2	P _{T1}	1.5	W
Total Power Dissipation (PW = 10 sec) *2	P _{T2}	3.8	W
Total Power Dissipation (T _C = 25°C)	P _{T3}	52	W
Channel Temperature	T _{ch}	150	°C
Storage Temperature	T _{stg}	−55 to +150	°C
Single Avalanche Current *3	I _{AS}	25	A
Single Avalanche Energy *3	E _{AS}	62	mJ

Thermal Resistance

Channel to Ambient Thermal Resistance *2 R_{th(ch-A)} 83.3 °C/W Channel to Case (Drain) Thermal Resistance R_{th(ch-C)} 2.4 °C/W

Notes: *1. PW \leq 10 μ s, Duty Cycle \leq 1%

*2. Mounted on a glass epoxy board of 25.4 mm x 25.4 mm x 0.8 mmt

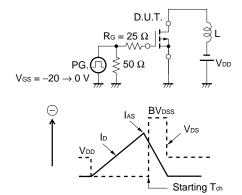
*3. Starting T_{ch} = 25°C, V_{DD} = -15 V, R_{G} = 25 Ω , V_{GS} = -20 \rightarrow 0 V, L = 100 μH

Electrical Characteristics (T_A = 25°C)

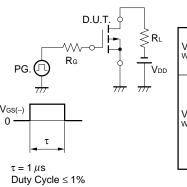
Item	Symbol	Min	Тур	Max	Unit	Test Conditions
Zero Gate Voltage Drain Current	I _{DSS}			-1	μΑ	$V_{DS} = -30 \text{ V}, V_{GS} = 0 \text{ V}$
Gate Leakage Current	I _{GSS}			±100	nA	$V_{GS} = \pm 20 \text{ V}, V_{DS} = 0 \text{ V}$
Gate Cut-off Voltage	$V_{GS(off)}$	-1.0		-2.5	V	$V_{DS} = -10 \text{ V}, I_{D} = -1 \text{ mA}$
Forward Transfer Admittance *1	y _{fs}	8.0			S	$V_{DS} = -10 \text{ V}, I_{D} = -15 \text{ A}$
Drain to Source On-state	R _{DS(on)1}		3.8	4.8	mΩ	$V_{GS} = -10 \text{ V}, I_D = -30 \text{ A}$
Resistance *1	R _{DS(on)2}		6.4	9.9	mΩ	$V_{GS} = -4.5 \text{ V}, I_D = -15 \text{ A}$
Input Capacitance	C _{iss}		3740		pF	$V_{DS} = -10 \text{ V},$
Output Capacitance	Coss		1780		pF	$V_{GS} = 0 V$,
Reverse Transfer Capacitance	C _{rss}		1500		pF	f = 1 MHz
Turn-on Delay Time	t _{d(on)}		24		ns	$V_{DD} = -15 \text{ V}, I_D = -15 \text{ A},$
Rise Time	t _r		53		ns	$V_{GS} = -10 \text{ V},$
Turn-off Delay Time	$t_{d(off)}$		180		ns	$R_G = 10 \Omega$
Fall Time	t _f		250		ns	
Total Gate Charge	Q _G		100		nC	$V_{DD} = -24 \text{ V},$
Gate to Source Charge	Q _{GS}		11		nC	$V_{GS} = -10 \text{ V},$
Gate to Drain Charge	Q_{GD}		48		nC	$I_D = -30 \text{ A}$
Body Diode Forward Voltage *1	$V_{F(S-D)}$		0.85		V	$I_F = 30 \text{ A}, V_{GS} = 0 \text{ V}$
Reverse Recovery Time	t _{rr}		196		ns	$I_F = 30 \text{ A}, V_{GS} = 0 \text{ V},$
Reverse Recovery Charge	Q _{rr}		297		nC	di/dt = 100 A/μs

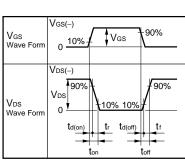
Note: *1. Pulsed

TEST CIRCUIT 1 AVALANCHE CAPABILITY



TEST CIRCUIT 2 SWITCHING TIME



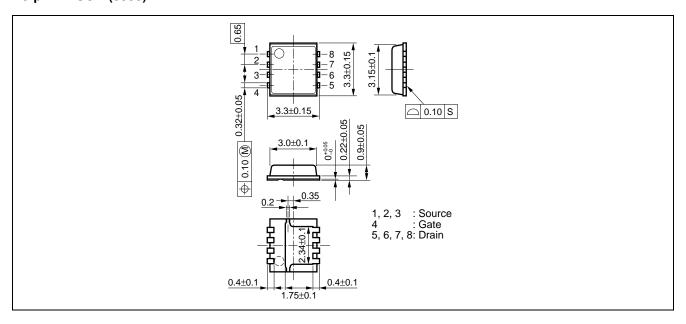


TEST CIRCUIT 3 GATE CHARGE

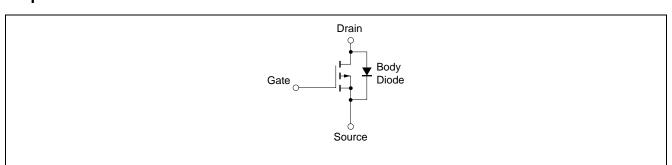
$$\begin{array}{c|c} D.U.T. \\ \hline \\ IG = -2 \text{ mA} \\ \hline \\ PG. \\ \hline \\ \end{array}$$

Package Drawings (Unit: mm)

8-pin HVSON (3333)



Equivalent Circuit



Remark Strong electric field, when exposed to this device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred.

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