

Features

- Two independent clock channels
- Two programmable digital PLLs/Numerically Controlled Oscillators (NCOs)
- Four precision synthesizers generate any clock-rate from 1 Hz to 750 MHz with low jitter for 10 G PHYs
- Programmable digital PLLs synchronize to any clock rate from 1 kHz to 750 MHz
- Automatic hitless reference switching and digital holdover on reference fail
- Nine input references configurable as single ended or differential and two single ended input references
- Phase alignment to input 1 Hz frame pulse with associated reference clock (ref/sync pairing)
 - Any input reference can be fed with sync (frame pulse) or clock
- Digital PLLs filter jitter at 5.2 Hz, 14 Hz, 28 Hz, 56 Hz, 112 Hz, 224 Hz, 448 Hz or 896 Hz

Ordering Information

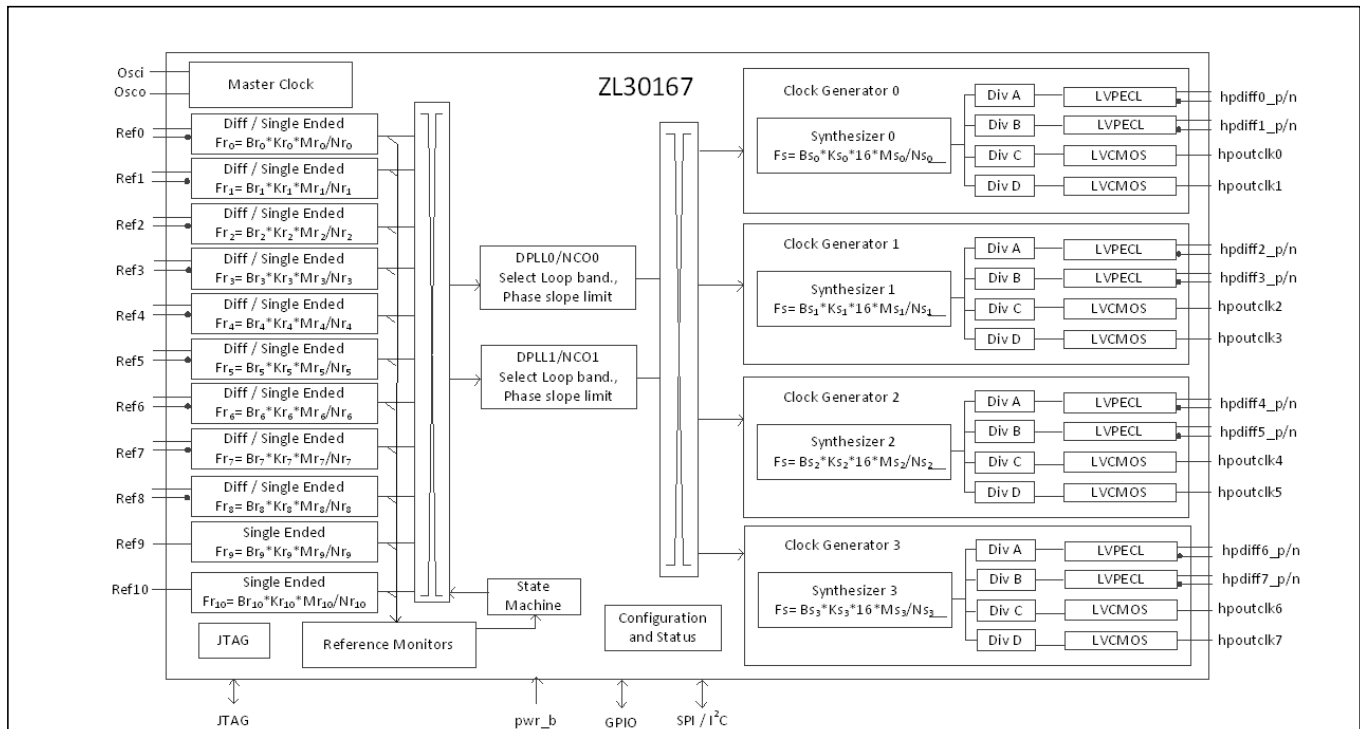
ZL30167GDG2 144 Pin LPGA Trays

 Pb Free Tin/Silver/Copper
 -40°C to +85°C
 Package Size: 13 x 13 mm

- Eight LVPECL outputs and eight LVCMOS outputs
- Operates from a single crystal resonator or clock oscillator
- Flexible two-stage architecture translates between arbitrary data rates, line coding rates and FEC rates
- Field programmable via SPI/I²C interface

Applications

- OTN muxponders and transponders
- 10 Gigabit line cards
- Synchronous Ethernet, 10 GBASE-R and 10 GBASE-W
- SONET/SDH, Fibre Channel, XAUI


Figure 1 - Functional Block Diagram



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