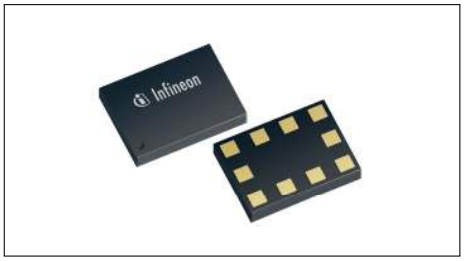
BGSA143ML10

Low Resistance Antenna Tuning Switch

Features

- Designed for high-linearity antenna tuning switching and RF tuning applications
- Ultra low R_{ON} resistance of 1.15 Ω at each port in ON state
- Each Switch chain directly controlled, R_{ON} reducable down to 0.3 Ω
- Low C_{OFF} capacitance of 140 fF at each port in OFF state
- High RF operating peak voltage handling of 42 V in OFF state
- Low harmonic generation
- MIPI RFFE control interface
- 4 USID addresses enabled by external condition at USID_Sel pin and SCLK/SDATA swap mode
- No RF parameter change within supply voltage range
- Small form factor 1.1 mm x 1.5 mm (MSL1, 260°C per JEDEC J-STD-020)
- RoHS and WEEE compliant package



1.1 x 1.5 mm^2

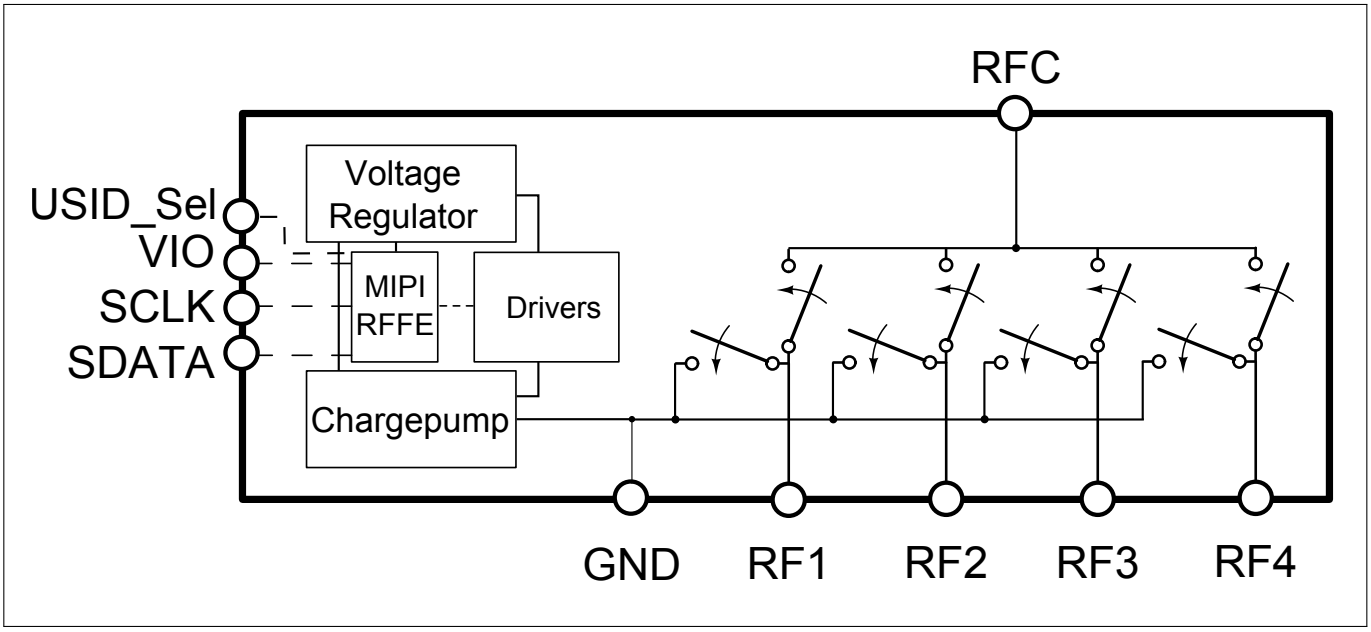
Application

- Impedance Tuning
- Antenna Tuning
- Inductance Tuning
- Tunable Filters

Product Validation

Qualified for industrial applications according to the relevant tests of JEDEC47/20/22.

Block diagram



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1 Features

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RoHS Halogen-Free Lead-Free Greer

Description

The BGSA143ML10 is a versatile Single-Pole Quad Throw (SP4T) RF antenna tuning switch featuring open or short to ground reflective OFF ports, being optimized for tuning applications up to 6.0 GHz. Including a RFFE digital control interface, this switch offers the possibility to adopt a SP4T, SP3T, SPDT along with SPST topology for a better flexibility in RF Front-End designs.

The BGSA143ML10 includes 4 ultra-low R_{on} series ports and 4 individually switchable shunt switches to enable open reflective and short-reflective behavior. As a result any type of antenna tuning switching or tuner circuits can be realized. Unlike GaAs technology, the 0.1 dB compression point exceeds the switch maximum input power level, resulting in linear performance at all signal levels and external DC blocking capacitors at the RF ports are only required if DC voltage is applied externally. Due to its high RF voltage ruggedness, it is suited for switching any reactive devices such as inductors and capacitors in RF matching circuits without significant losses in quality factors.

Product Name	Marking	Package
BGSA143ML10	AA	TSLP-10-2

2 Maximum Ratings

Table 1: Maximum Ratings, Table I at T_A = 25 °C, unless otherwise specified

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Frequency Range	f	0.4	–	–	GHz	[1]
RFFE Supply voltage [2]	V_{IO}	-0.5	–	2.2	V	Only for infrequent and short duration time periods
Storage temperature range	T_{STG}	-55	–	150	°C	–
RF input power	P_{RF_max}	–	–	39	dBm	Pulsed RF input power, duty cycle of 25 % with T_period= 4620 µs, ON-state, setup as of Fig. 2
RF peak voltage	V_{RF_max}	–	–	50	V	Short term peaks (1µs, duty cycle 0.1%), Isolation mode, test setup acc. Fig. 1 and exceeding typical linearity, R_{ON} and C_{OFF} parameters
ESD capability, CDM [3]	$V_{ESD_{CDM}}$	-1	–	+1	kV	
ESD capability, HBM [4]	$V_{ESD_{HBM}}$	-0.6	–	+0.6	kV	
ESD capability, system level (RF port) [5]	$V_{ESD_{ANT}}$	-8	–	+8	kV	RFx vs system GND, with 27 nH shunt inductor on tested port
Junction temperature	T_j	–	–	125	°C	–
Thermal resistance junction - soldering point	R_{thJS}	–	–	43	K/W	–
RFFE Control Voltage Levels	V_{SCLK}, V_{SDATA}, V_{USID_Sel}	-0.7	–	V_{IO}+0.7 (max. 2.2)	V	–

[1] Switch has a low-pass response. For higher frequencies, losses have to be considered for their impact on thermal heating. The DC voltage at RF ports V_{RFDC} has to be 0V.
[2] Note: Consider any ripple voltages on top of V_{IO}. A high RF ripple at the V_{IO} can exceed the maximum ratings by $V_{IO} = V_{DC} + V_{Ripple}$.
[3] Field-Induced Charged-Device Model ANSI/ESDA/JEDEC JS-002 Simulates charging/discharging events that occur in production equipment and processes. Potential for CDM ESD events occurs whenever there is metal-to-metal contact in manufacturing.
[4] Human Body Model ANSI/ESDA/JEDEC JS-001 (R = 1,5 kΩ, C = 100 pF).
[5] IEC 61000-4-2 (R = 330 Ω, C = 150 pF), contact discharge.

Warning: Stresses above the max. values listed here may cause permanent damage to the device. Maximum ratings are absolute ratings; exceeding only one of these values may cause irreversible damage to the integrated circuit. Exposure to conditions at or below absolute maximum rating but above the specified maximum operation conditions may affect device reliability and life time. Functionality of the device might not be given under these conditions.

Maximum Ratings

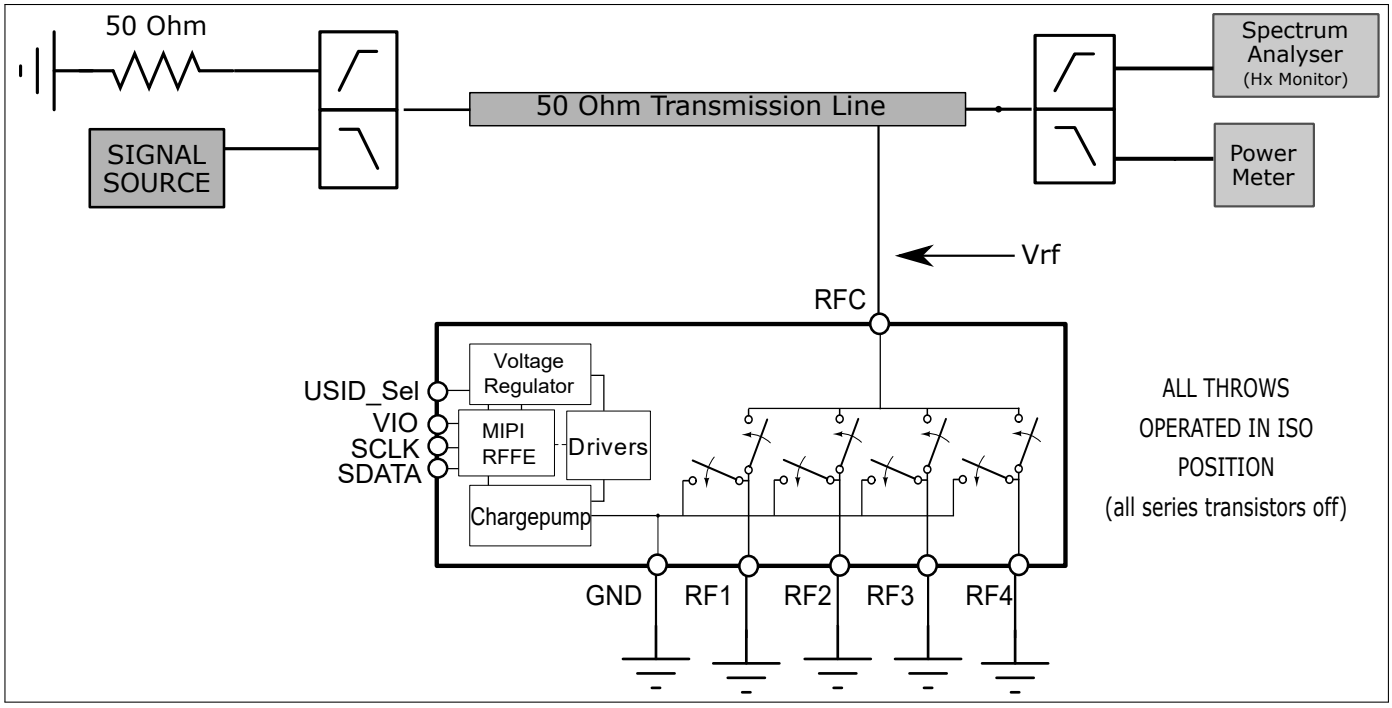

Figure 1: RF operating voltage measurement configuration - OFF mode

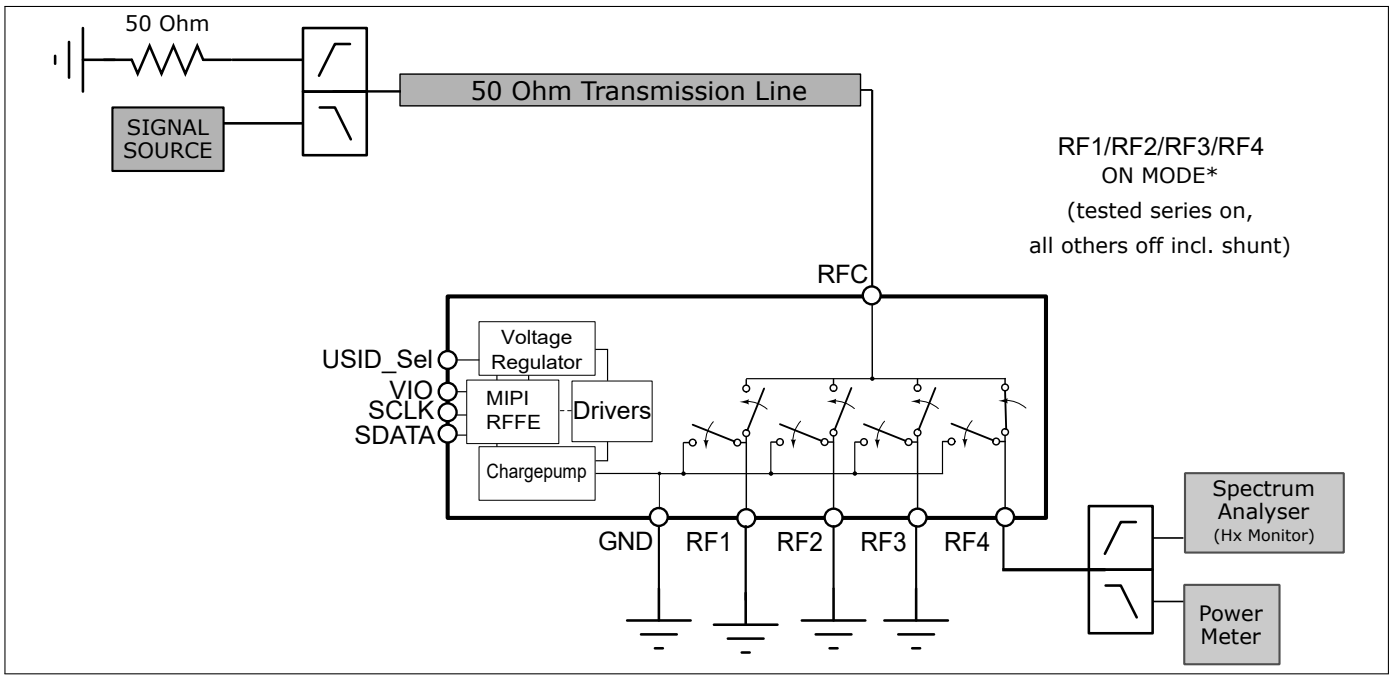

Figure 2: RF operating and Harmonics generation measurement configuration - RFx ON mode

*This example is only from RF4.

3 DC Characteristics

Table 2: DC Characteristics at T_A = −40 °C to 85 °C

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
RFFE supply voltage	V_{IO}	1.65	1.8	1.95	V	–
RFFE input high voltage[1]	V_{IH}	0.7*V_{IO}	–	V_{IO}	V	–
RFFE input low voltage[1]	V_{IL}	0	–	0.3*V_{IO}	V	–
RFFE output high voltage[1]	V_{OH}	0.8*V_{IO}	–	V_{IO}	V	–
RFFE output low voltage[1]	V_{OL}	0	–	0.2*V_{IO}	V	–
RFFE control input capacitance	C_{Ctrl}	–	–	2	pF	–
RFFE supply current	I_{VIO}	–	2.5	–	µA	Low Power Mode
		–	65	140	µA	Idle State
		–	70	200	µA	Full RF Power[2]

[1] SCLK
[2] 36dBm input power, series switch in ON mode condition

4 RF Small Signal Characteristics

Table 3: Parametric specifications

Parameter	Symbol	Values			Unit	STATE / Notes
		Min.	Typ.	Max.		
Frequency range	f	0.4		6.0	GHz	V_{IO} = 1.65 – 1.95 V, T_A = −40 °C... + 85 °C, Z_0 = 50 Ω
RFx to RFc ON DC resistance	R_{ON}		1.15		Ω	
RFx to RFc OFF DC resistance	R_{OFF}	–	200	–	kΩ	
RFx to GND ON DC resistance	$R_{ON,Shunt}$		5.9		Ω	
RFx to GND OFF DC resistance	$R_{OFF,Shunt}$	–	200	–	kΩ	
RFx to RFc[1] OFF capacitance	C_{OFF}	–	140	–	fF	

[1] C_{OFF} at 1GHz, represents the series capacitance RFx to GND. It is fitting to the Isolation Values for OPEN Shunts.

Table 4: RF electrical parameters, OFF port shunts switches open - NO Shunts

Parameter	Symbol	Values			Unit	STATE / Notes
		Min.	Typ.	Max.		
Insertion Loss: RF1 to RFc, RF2 to RFc, RF3 to RFc or RF4 to RFc (1,2)						
698 - 960 MHz	IL_{SP4T}	–	0.18	0.3	dB	V_{IO} = 1.65 – 1.95 V, Z_0 = 50 Ω at all RF-ports, T_A = −40 °C... + 85 °C
1710 - 1980 MHz		–	0.35	0.55	dB	
1981 - 2169 MHz		–	0.45	0.6	dB	
2170 - 2690 MHz		–	0.5	0.8	dB	
3400 - 3800 MHz		–	1.0	1.5	dB	
5000 - 6000 MHz		–	1.9	3.2	dB	
Return Loss: RF1, RF2, RF3 or RF4 (1,2)						
698 - 960 MHz	RL_{SP4T}	19	28	–	dB	V_{IO} = 1.65 – 1.95 V, Z_0 = 50 Ω at all RF-ports, T_A = −40 °C... + 85 °C
1710 - 1980 MHz		13	17	–	dB	
1981 - 2169 MHz		12	16	–	dB	
2170 - 2690 MHz		11.5	14	–	dB	
3400 - 3800 MHz		7.9	10	–	dB	
5000 - 6000 MHz		5.8	8.1	–	dB	
Isolation: All RF OFF(1,2)						
698 - 960 MHz	ISO_{OFF}	22	24	–	dB	V_{IO} = 1.65 – 1.95 V, Z_0 = 50 Ω at all RF-ports, T_A = −40 °C... + 85 °C
1710 - 1980 MHz		16	17	–	dB	
1981 - 2169 MHz		15	16	–	dB	
2170 - 2690 MHz		14	15	–	dB	
3400 - 3800 MHz		12	13	–	dB	
5000 - 6000 MHz		10	12	–	dB	

1) Valid for all RF power levels, no compression behavior
2) On application board without any matching components

Table 5: RF electrical parameters, OFF port shunts switches closed- WITH Shunts

Parameter	Symbol	Values			Unit	STATE / Notes
		Min.	Typ.	Max.		
Insertion Loss: RF1 to RFc, RF2 to RFc, RF3 to RFc or RF4 to RFc (1,2)						
698 - 960 MHz	IL_{SP4T}	–	0.18	0.3	dB	V_{IO} = 1.65 ... 1.95 V, Z_0 = 50 Ω at all RF-ports, T_A = −40 °C... + 85 °C
1710 - 1980 MHz		–	0.35	0.55	dB	
1981 - 2169 MHz		–	0.4	0.6	dB	
2170 - 2690 MHz		–	0.5	0.75	dB	
3400 - 3800 MHz		–	0.95	1.45	dB	
5000 - 6000 MHz		–	2.05	3.2	dB	
Return Loss: RF1, RF2, RF3 or RF4 (1,2)						
698 - 960 MHz	RL_{SP4T}	18	25	–	dB	V_{IO} = 1.65 ... 1.95 V, Z_0 = 50 Ω at all RF-ports, T_A = −40 °C... + 85 °C
1710 - 1980 MHz		13	16	–	dB	
1981 - 2169 MHz		12	15	–	dB	
2170 - 2690 MHz		11	14	–	dB	
3400 - 3800 MHz		7.1	10	–	dB	
5000 - 6000 MHz		5.0	7.4	–	dB	
Isolation: All RF OFF(1,2)						
698 - 960 MHz	ISO_{OFF}	32	38	–	dB	V_{IO} = 1.65 ... 1.95 V, Z_0 = 50 Ω at all RF-ports, T_A = −40 °C... + 85 °C
1710 - 1980 MHz		22	27	–	dB	
1981 - 2169 MHz		21	26	–	dB	
2170 - 2690 MHz		18	24	–	dB	
3400 - 3800 MHz		14	19	–	dB	
5000 - 6000 MHz		10	14	–	dB	

1) Valid for all RF power levels, no compression behavior
2) On application board without any matching components

5 RF large signal parameter

Table 6: RF large signal specifications at T_A = 25 °C

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
RF Operating Voltage	V_{RF_opr}			42	V	In Isolation mode, test condition schematic in Fig. 1 for H2/H3 <-42 dBm @50 Ω
Harmonic Generation up to 12.75 GHz						
All RF Ports - Second Order Harmonics	P_{H2}	–	-85	–	dBm	25 dBm, 50 Ω, f_0 = 698 MHz
All RF Ports - Third Order Harmonics	P_{H3}	–	-91	–	dBm	25 dBm, 50 Ω, f_0 = 698 MHz
All RF Ports - Second Order Harmonics	P_{H2}	–	-67	–	dBm	35 dBm, 50 Ω, f_0 = 824 MHz
All RF Ports - Third Order Harmonics	P_{H3}	–	-63	–	dBm	35 dBm, 50 Ω, f_0 = 824 MHz
All RF Ports - Second Order Harmonics	P_{H2}	–	-66	–	dBm	33 dBm, 50 Ω, f_0 = 1960 MHz
All RF Ports - Third Order Harmonics	P_{H3}	–	-66	–	dBm	33 dBm, 50 Ω, f_0 = 1960 MHz
All RF Ports - Second Order Harmonics	P_{H2}	–	-76	–	dBm	25 dBm, 50 Ω, f_0 = 2500 MHz
All RF Ports - Third Order Harmonics	P_{H3}	–	-85	–	dBm	25 dBm, 50 Ω, f_0 = 2500 MHz
All RF Ports	P_{Hx}	–	–	-80	dBm	25 dBm, 50 Ω
Intermodulation Distortion IMD2						
IIP2, low	$IIP2, l$	–	120	–	dBm	IIP2 conditions Tab. 7
IIP2, high	$IIP2, h$	–	130	–	dBm	
Intermodulation Distortion IMD3						
IIP3	$IIP3$	–	78	–	dBm	IIP3 conditions Tab. 8

RF large signal parameter

Table 7: IIP2 conditions table

Band	In-Band Frequency [MHz]	Blocker Frequency 1 [MHz]	Blocker Power 1 [dBm]	Blocker Frequency 2 [MHz]	Blocker Power 2 [dBm]
Band 1 Low	2140	1950	20	190	-15
Band 1 High	2140	1950	20	4090	-15
Band 5 Low	881.5	836.5	20	45	-15
Band 5 High	881.5	836.5	20	1718	-15

Table 8: IIP3 conditions table

Band	In-Band Frequency [MHz]	Blocker Frequency 1 [MHz]	Blocker Power 1 [dBm]	Blocker Frequency 2 [MHz]	Blocker Power 2 [dBm]
Band 1	2140	1950	20	1760	-15
Band 5	881.5	836.5	20	791.5	-15

6 MIPI RFFE Specification

All sequences are implemented according to the 'MIPI Alliance Specification for RF Front-End Control Interface' document version 2.0.

Table 9: MIPI Features

Feature	Supported	Comment
MIPI RFFE 1.10 and 2.0 standards	Yes	
Register 0 write command sequence	Yes	
Register read and write command sequence	Yes	
Extended register read and write command sequence	Yes	
Support for standard frequency range operations for SCLK	Yes	Up to 26 MHz
Support for extended frequency range operations for SCLK	Yes	Up to 52 MHz
Programmable Group SID	Yes	
Programmable USID	Yes	
Trigger functionality	Yes	
Broadcast / GSID write to PM TRIG register	Yes	
Reset	Yes	Via VIO, PM TRIG or software register
Status / error sum register	Yes	
Extended product ID register	Yes	
Revision ID register	Yes	
Group SID register	Yes	
USID select pin	Yes	See Tab. 13

Table 10: Startup Behavior

Feature	State	Comment
Power status	LOW POWER	The chip is in low power mode after startup
Trigger function	ENABLED	Trigger function is enabled after startup. Trigger function can be disabled via PM_TRIG register.

Table 11: Switching Time Behavior at V_{IO} = 1.65 – 1.95 V, T_A = −40 °C... + 85 °C

Parameter	Symbol	Values			Unit	STATE / Notes
		Min.	Typ.	Max.		
Power Up Settling Time	t_{PUP}	-	10	25	µs	Time from Power Up plus Switch command 50% last SCLK falling edge to 90% RF-Signal, see Fig. 3
Switching Time	t_{ST}	-	5	7	µs	Time switching between RF states 50% last SCLK falling edge to 90% RF-Signal, see Fig. 3

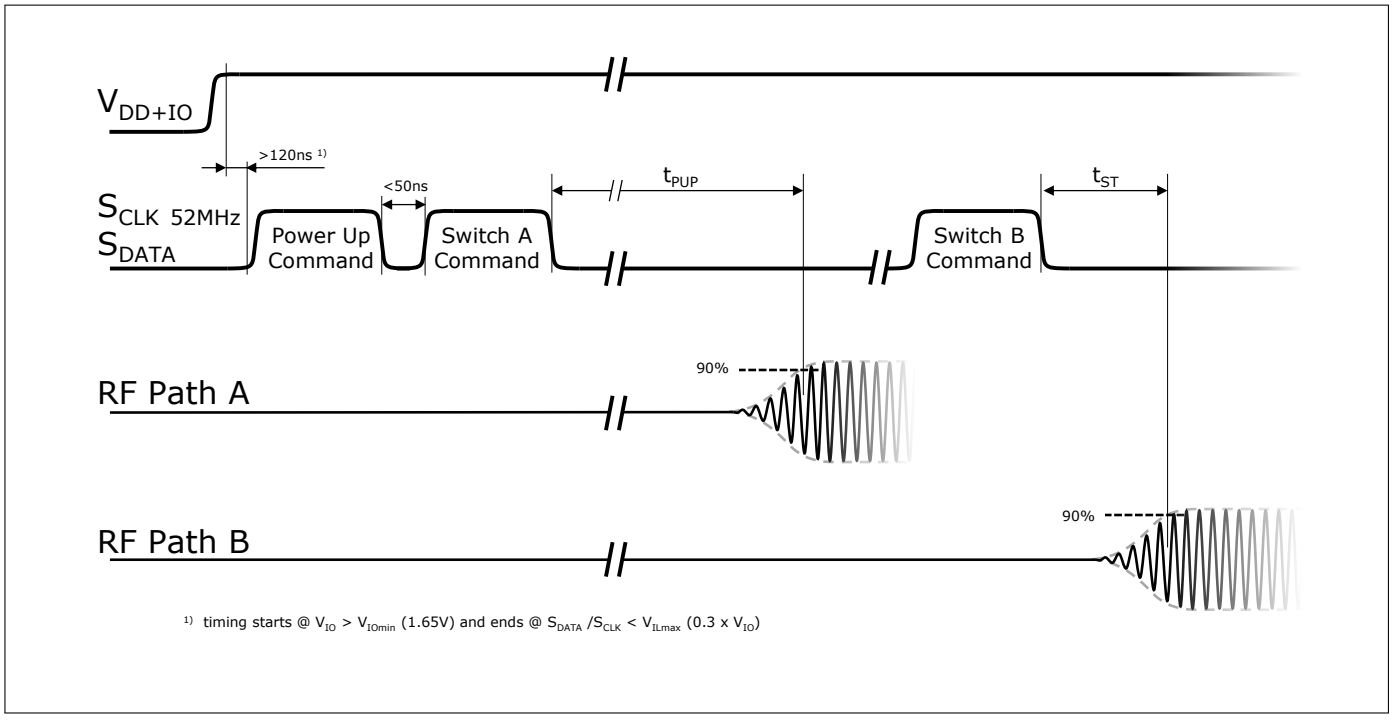

Figure 3: BGSA143ML10 Switching time behavior

Table 12: MIPI RFFE Operating Timing

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
SCLK Frequency	FSCLK	0.032	–	26	MHz	Standard frequency range
		26	–	52	MHz	Extended frequency range
SCLK Low Period	TSCLKIL	10.8	–	–	ns	Standard frequency range, see Fig. 4
		4.7	–	–	ns	Extended frequency range, see Fig. 4
SCLK High Period	TSCLKIH	10.8	–	–	ns	Standard frequency range, see Fig. 4
		4.7	–	–	ns	Extended frequency range, see Fig. 4
SDATA Setup Time	TS	1	–	–	ns	See Fig. 5
SDATA Hold Time	TH	5	–	–	ns	See Fig. 5
SDATA Release Time	TSDATAZ	–	–	10	ns	See Fig. 6
Time for Data Output	TD	–	–	22	ns	See Fig. 7
SDATA Rise/Fall Time	TSDATAOTR	2.1	–	10	ns	See Fig. 7
VIO Rise Time	TVIO-R	50	–	450	µs	See Fig. 8
VIO Reset Time	TVIO-RST	10	–	–	µs	See Fig. 8
Reset Delay Time	TSIGOL	0.12	–	–	µs	See Fig. 8

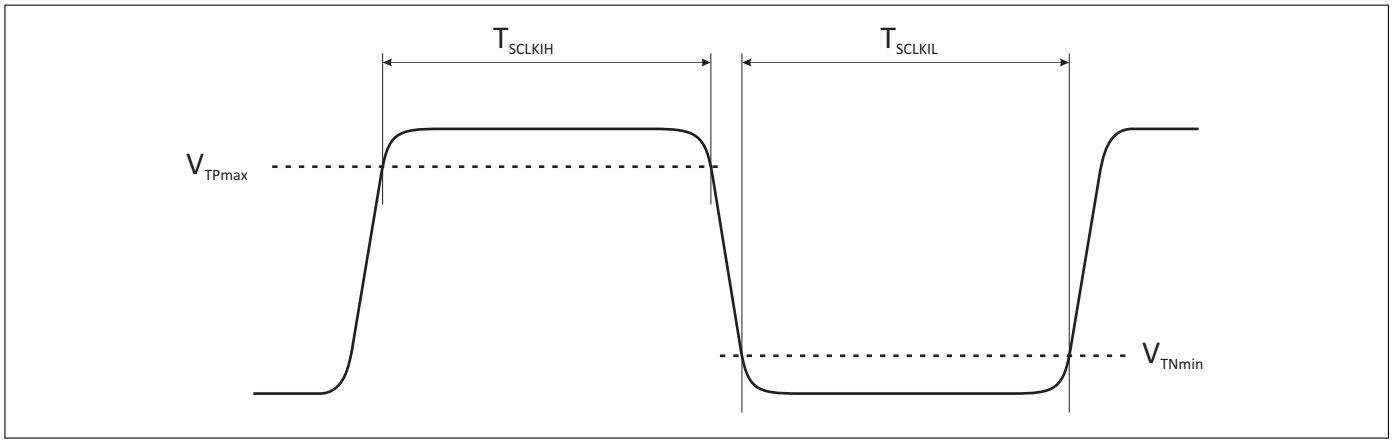

Figure 4: Received clock signal constraints

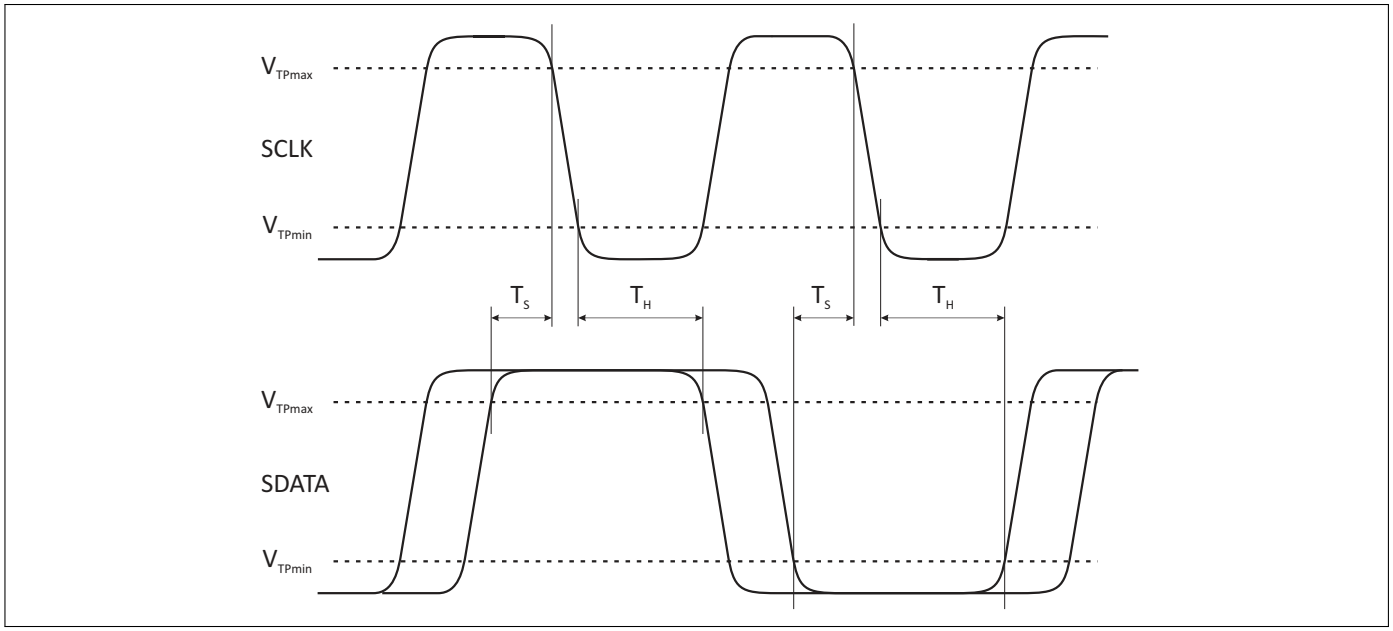

Figure 5: Bus active data receiver timing requirements

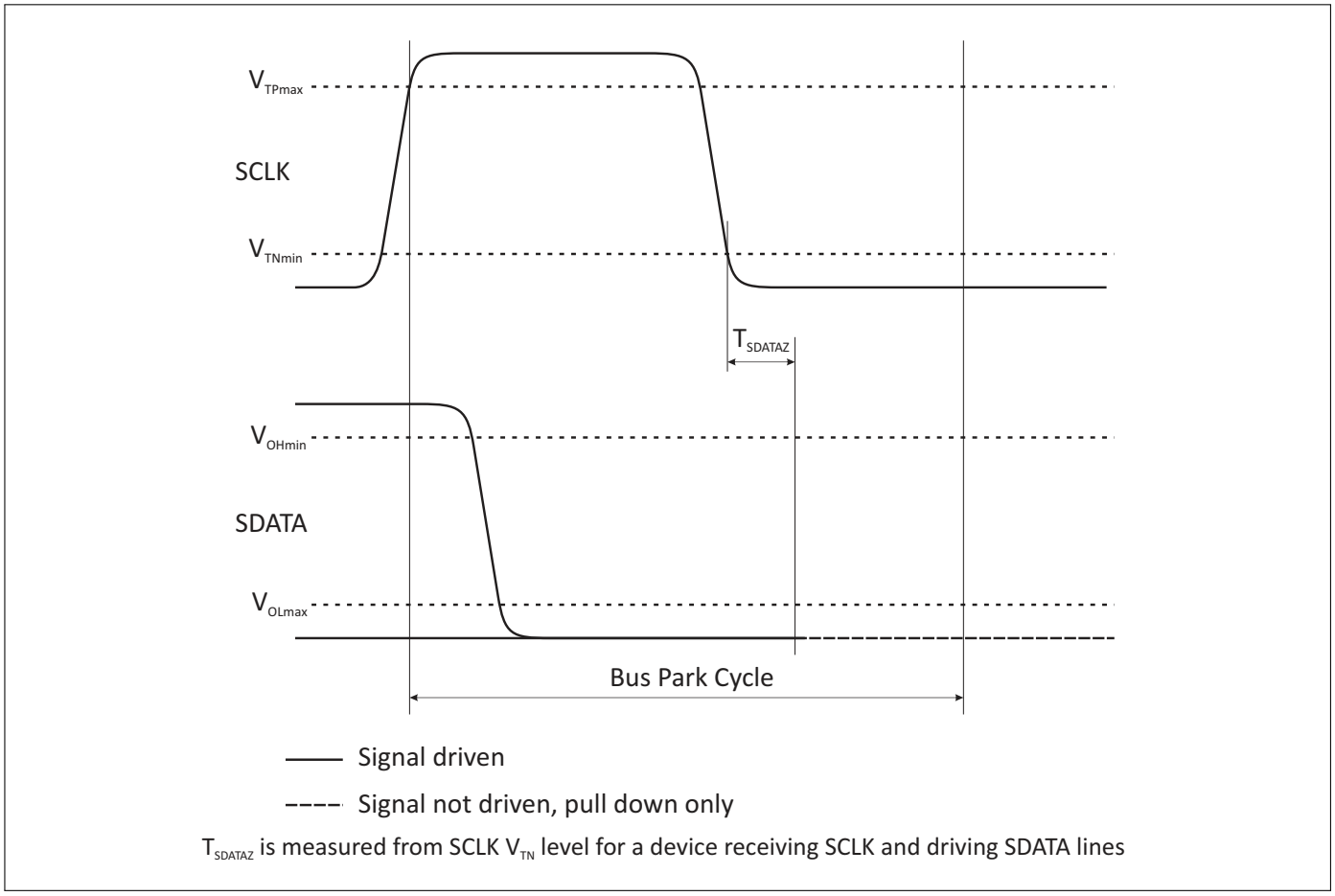

Figure 6: Bus park cycle timing

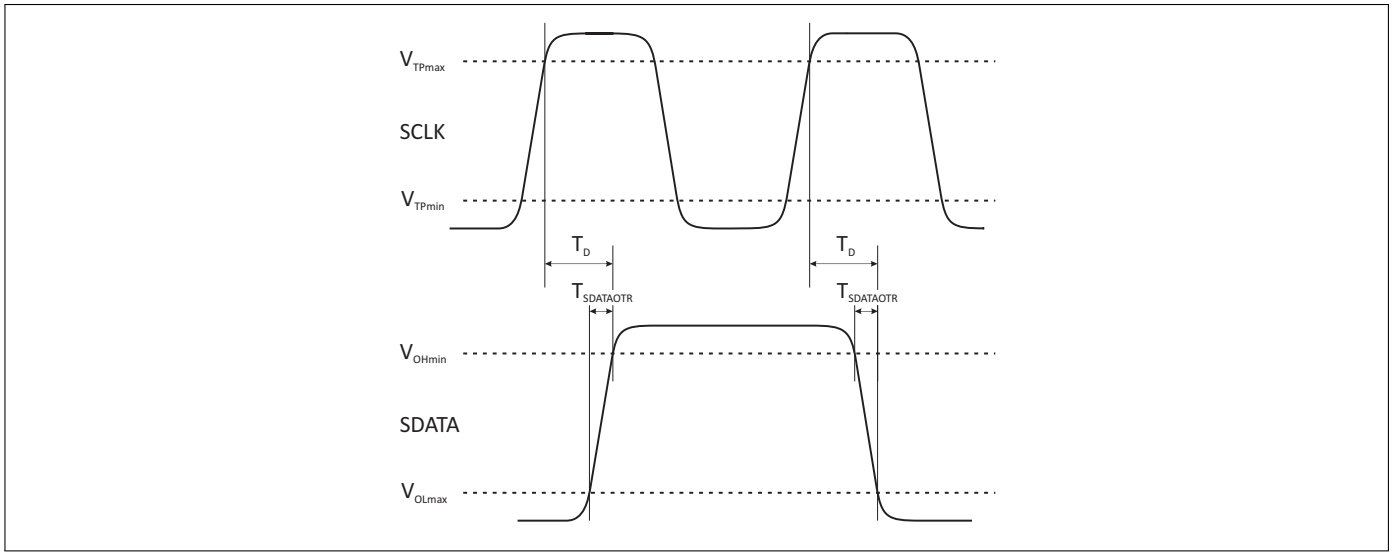

Figure 7: Bus active data transmission timing specification

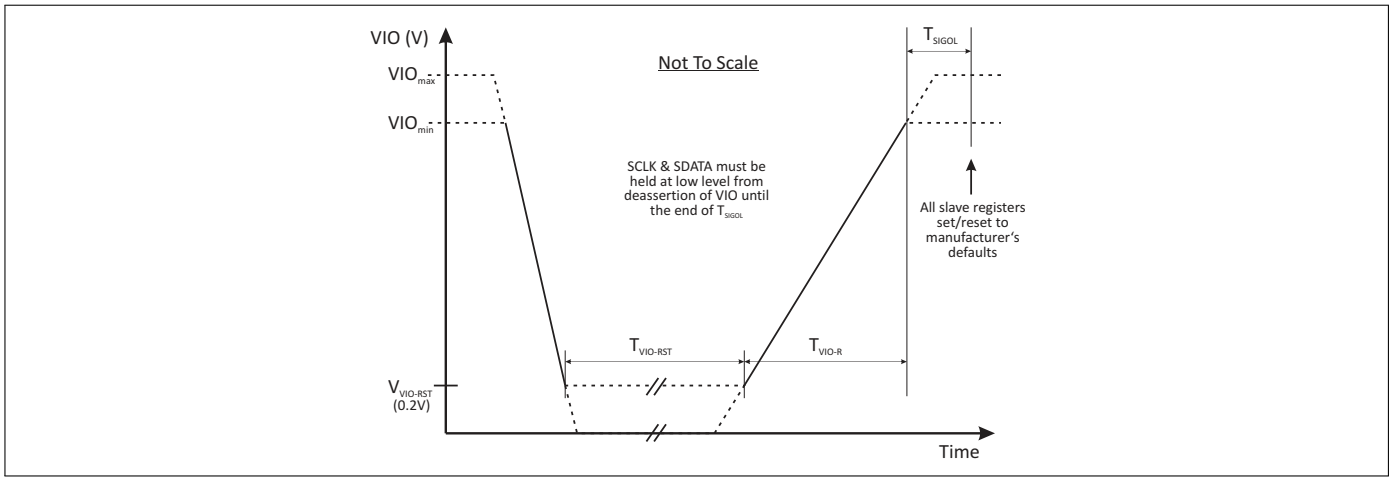

Figure 8: Requirements for VIO-initiated reset

Table 13: USID Selection

Address	Symbol	SCLK/SDATA lines routing	External Condition at USID_Sel Pin
USID=0111	$Addr_7$	SCLK routed to pin 6, SDATA routed to pin 5	Ground
USID=0110	$Addr_6$	SCLK routed to pin 6, SDATA routed to pin 5	to V_{IO}
USID=1100	$Addr_{12}$	SCLK routed to pin 5, SDATA routed to pin 6	Ground (SCLK/SDATA Swap Mode)
USID=0010	$Addr_2$	SCLK routed to pin 5, SDATA routed to pin 6	to V_{IO} (SCLK/SDATA Swap Mode)

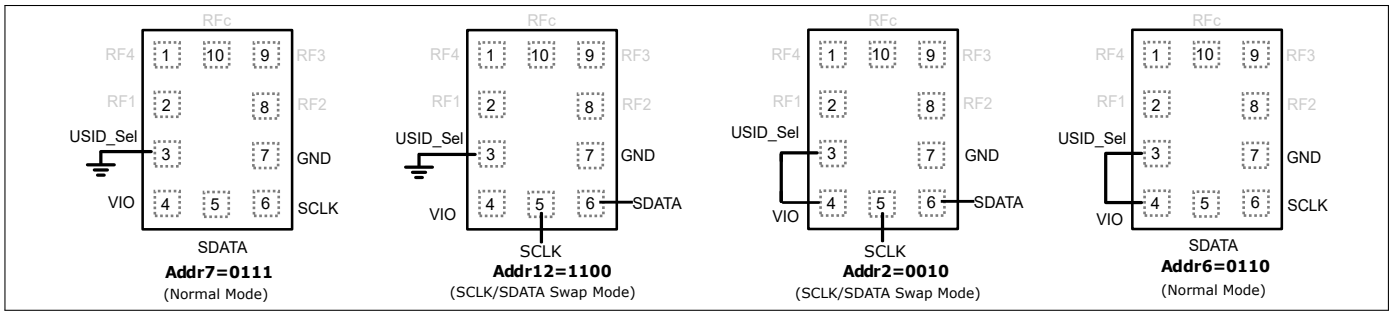

Figure 9: BGSA143ML10 USID_Sel Pin configuration

Important Note: Infineon's SCLK/SDATA swap mode requires a "clean" MIPI RFFE clock signal to trigger a proper communication between SCLK RFFE Master device and BGSA143ML10. To guarantee "clean" MIPI RFFE clock signal reaching BGSA143ML10 digital input, SCLK line must have a pull-down resistor to ground. In case the RFFE Master does not provide an internal pull-down, Infineon recommends to add a 100kohm resistor pull-down to ground on the RFFE Master SCLK driver output line.
For more details please refer to the technical report "MIPI RFFE Device I/O Structures - IFX RF Switches and Antenna Tuners".

Table 14: Register Mapping

Register Address	Register Name	Data Bits	Function	Description	Default	Broadcast_ID Support	Trigger Support	R/W
0x0000	REGISTER_0	7:0	MODE_CTRL	Switch Path control	00000000	No	All	R/W
0x0001	REGISTER_1	7:0	MODE_CTRL	Switch Path control	00000000	No	All	R/W
0x001C	PM_TRIG	7	PWR_MODE(1), Operation Mode	0: Normal operation (ACTIVE)	1	Yes	No	R/W
				1: Low Power Mode (LOW POWER)				
		6	PWR_MODE(0), State Bit Vector	0: No action (ACTIVE)	0			
				1: Powered Reset (STARTUP to ACTIVE to LOW POWER)				
		5	TRIGGER_MASK_2	0: Data masked (held in shadow REG)	0	No		
				1: Data not masked (ready for transfer to active REG)				
		4	TRIGGER_MASK_1	0: Data masked (held in shadow REG)	0			
				1: Data not masked (ready for transfer to active REG)				
		3	TRIGGER_MASK_0	0: Data masked (held in shadow REG)	0			
				1: Data not masked (ready for transfer to active REG)				
		2	TRIGGER_2	0: No action (data held in shadow REG)	0	Yes		
				1: Data transferred to active REG				
		1	TRIGGER_1	0: No action (data held in shadow REG)	0			
				1: Data transferred to active REG				
		0	TRIGGER_0	0: No action (data held in shadow REG)	0			
				1: Data transferred to active REG				
0x001D	PRODUCT_ID	7:0	PRODUCT_ID	This is a read-only register. However, during the programming of the USID a write command sequence is performed on this register, even though the write does not change its value.	00110010	No	No	R
0x001E	MAN_ID	7:0	MANUFACTURER_ID [7:0]	This is a read-only register. However, during the programming of the USID, a write command sequence is performed on this register, even though the write does not change its value.	00011010	No	No	R
0x1F	MAN_USID	7:6	RESERVED	Reserved for future use. Set to all 0.	00	No	No	R
		5:4	MANUFACTURER_ID [9:8]	Manufacturer ID. These bits are read-only. However, during the programming of the USID, a write command sequence is performed on this register even though the write does not change its value.	01			
		3:0	USID[3:0]	These bits store the USID of the device. Performing a write to this register using the described programming sequences will re-program the USID. The default value shall not be fused.	See Tab. 13	No	No	R/W

Table 15: Register Mapping, Table II

Register Address	Register Name	Data Bits	Function	Description	Default	Broadcast_ID Support	Trigger Support	R/W
0x20	EXT_PROD_ID[1)]	7:0	EXT_PRODUCT_ID	Extension to PRODUCT_ID in register 0x1D. This is a read-only register. However, during the programming of the USID a write command sequence is performed on this register, even though the write does not change its value.	00000000	No	No	R
0x21	REV_ID	7:4	MAIN_REVISION	Chip Main Revision	0000	No	No	R/W
		3:0	SUB_REVISION	Chip Sub Revision	0000			
0x22	GSID[1)]	7:4	GSID0[3:0]	Primary Group Slave ID.	0000	No	No	R/W
		3:0	RESERVED	Reserved for secondary Group Slave ID. Set all to 0.	0000			
0x23	UDR_RST	7	UDR_RST	Reset all configurable non-RFFE Reserved registers to default values. The UDR_RST bit shall revert to default value of 0 after software reset is enabled.	0	No	No	R/W
		6:0	RESERVED	Reserved for future use. Set to all 0.	0000000			
0x24	ERR_SUM	7	RESERVED	Reserved for future error codes. The ERR_SUM register reports error codes until read.	0	No	No	R
		6	COMMAND_FRAME_PARITY_ERR	Command Sequence received with parity error — discard command.	0			
		5	COMMAND_LENGTH_ERR	Command length error.	0			
		4	ADDRESS_FRAME_ PAR_ERR	Address frame with parity error.	0			
		3	DATA_FRAME_PAR_ERR	Data frame with parity error.	0			
		2	READ_UNUSED_REG	Read command to an invalid address.	0			
		1	WRITE_UNUSED_REG	Write command to an invalid address.	0			
		0	BID_GID_ERR	Read command with a BROADCAST_ID or GROUP_ID.	0			

[1)] Only supported by MIPI 2.0 Standard

Warning: Users must not write register 1 when register 0 control logic selected. Writing both Registers simultaneously will lead to undefined behavior. The unused register must remain 0x00.

Table 16: Modes of Operation (Truth Table, Register_0)

State	Mode	D7	D6	D5	D4	D3	D2	D1	D0
0	ALL OFF (Isolation)	0	0	0	0	0	0	0	0
1	RF1 Series	0	0	0	0	0	0	0	1
2	RF2 Series	0	0	0	0	0	0	1	0
3	RF3 Series	0	0	0	0	0	1	0	0
4	RF4 Series	0	0	0	0	1	0	0	0
5	RF1 Shunt	0	0	0	1	0	0	0	0
6	RF2 Shunt	0	0	1	0	0	0	0	0
7	RF3 Shunt	0	1	0	0	0	0	0	0
8	RF4 Shunt	1	0	0	0	0	0	0	0

Mapping of Switch Rows to Bit: ON = 1 OFF = 0

Warning: Users must not write register 0 when register 1 control logic selected. Writing both Registers simultaneously will lead to undefined behavior. The unused register must remain 0x00.

Table 17: Modes of Operation (Truth Table, Register_1)

State	Mode	D7	D6	D5	D4	D3	D2	D1	D0
0	ALL OFF (Isolation)	0	0	0	0	0	0	0	0
1	RF1 Series	0	0	0	0	0	0	0	1
2	RF2 Series	0	0	0	0	0	0	1	0
3	RF3 Series	0	0	0	0	0	1	0	0
4	RF4 Series	0	0	0	0	1	0	0	0
5	RF1 Shunt	0	0	0	1	0	0	0	0
6	RF2 Shunt	0	0	1	0	0	0	0	0
7	RF3 Shunt	0	1	0	0	0	0	0	0
8	RF4 Shunt	1	0	0	0	0	0	0	0

Mapping of Switch Rows to Bit: ON = 1 OFF = 0

BGSA143ML10 truth table allows to connect any combination of above bits in one single register_0 (respectively register_1) write command. As an example RF1 series can be set ON while RF1 shunt is set OFF, RF2, RF3 and RF4 series set OFF and shunt set ON by using this single register_0 write command «0b:11100001».

7 Application Information

Pin Configuration and Function

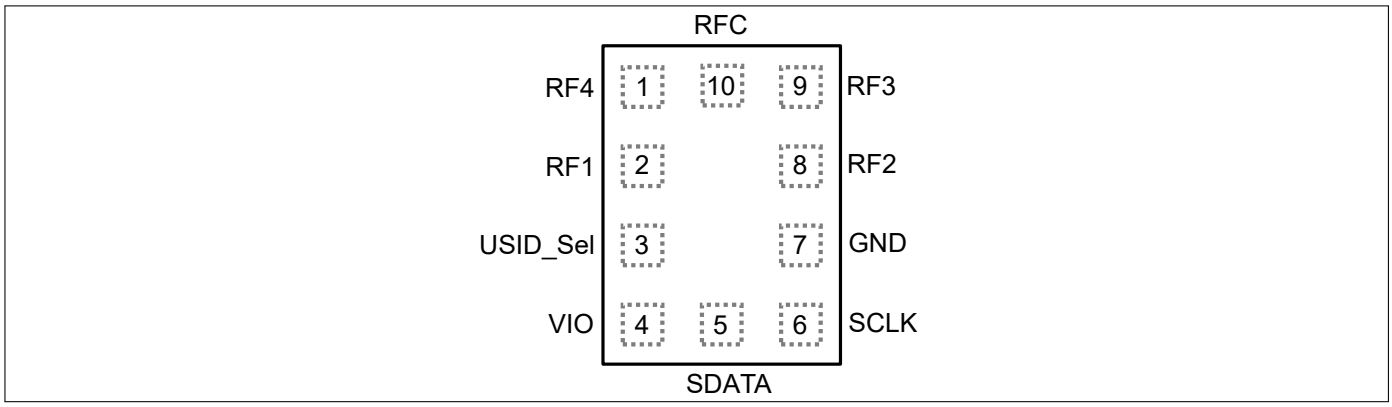

Figure 10: BGSA143ML10 Pin configuration (top view)

Table 18: Pin Definition and Function

Pin No.	Name	Function
1	RF4	RF4 port
2	RF1	RF1 port
3	USID_Sel	USID_Sel port
4	VIO	RFFE Power Supply
5	SDATA	MIPI RFFE DATA
6	SCLK	MIPI RFFE CLOCK
7	GND	Ground
8	RF2	RF2 port
9	RF3	RF3 port
10	RFC	Common RF port

8 Package Information

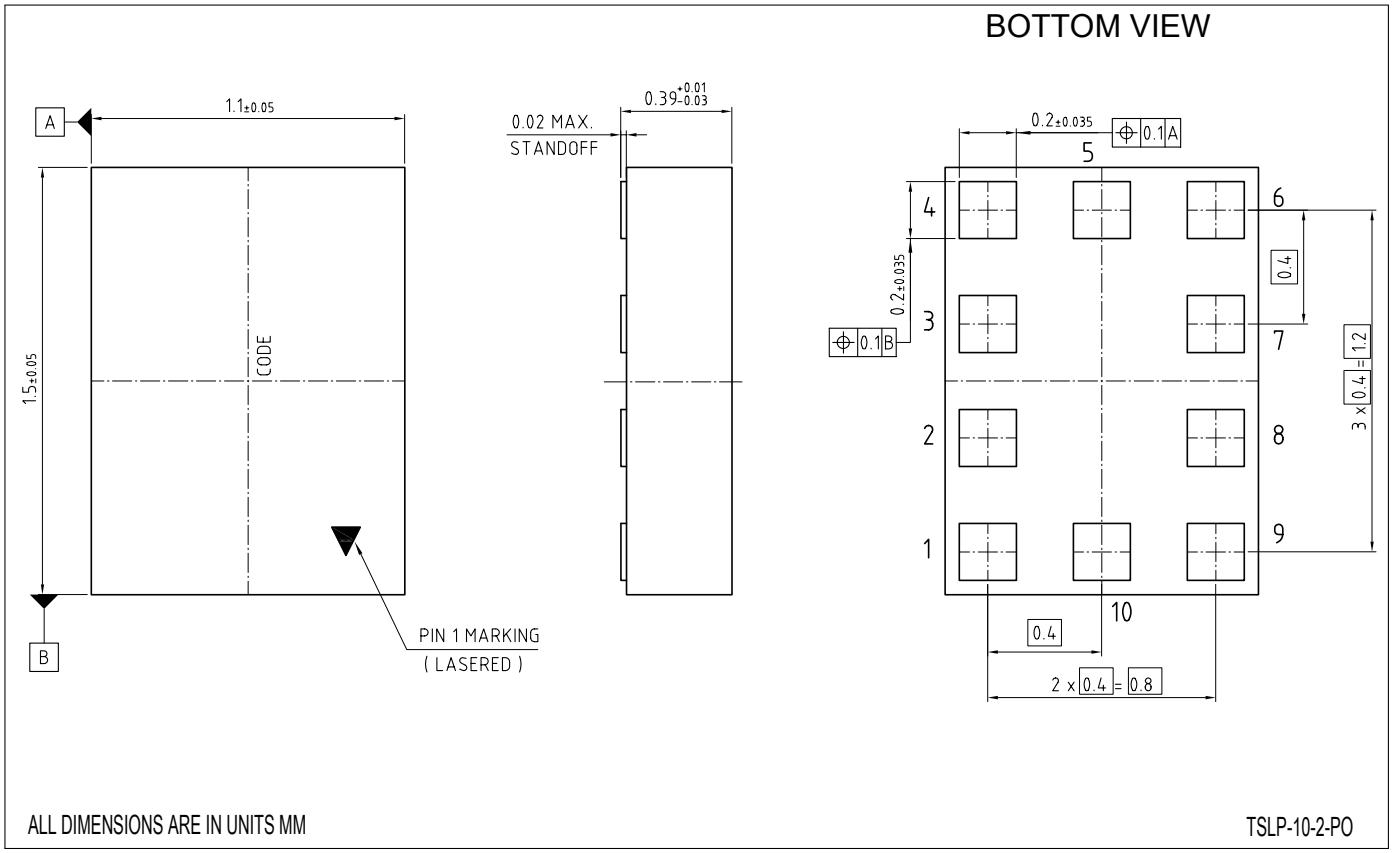

Figure 11: TSLP-10-2 Package outline (top, side and bottom views)

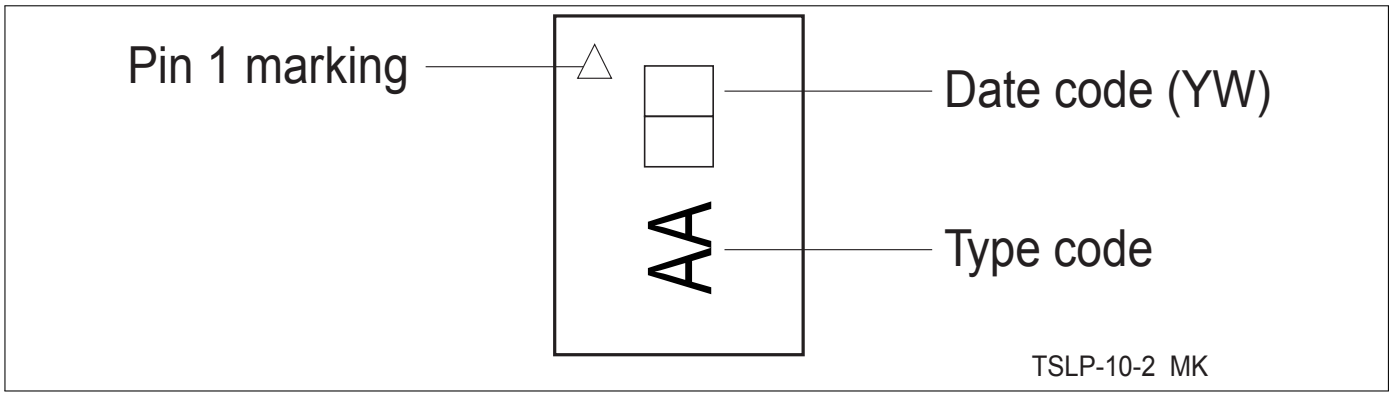

Figure 12: Marking specification (top view): Date code digits Y and W defined in Table 19/20

Table 19: Year date code marking - digit "Y"

Year	"Y"	Year	"Y"
2010	0	2020	0
2011	1	2021	1
2012	2	2022	2
2013	3	2023	3
2014	4	2024	4
2015	5	2025	5
2016	6	2026	6
2017	7	2027	7
2018	8	2028	8
2019	9	2029	9

Table 20: Week date code marking - digit "W"

Week	"W"	Week	"W"	Week	"W"	Week	"W"	Week	"W"
1	A	12	N	23	4	34	h	45	v
2	B	13	P	24	5	35	j	46	x
3	C	14	Q	25	6	36	k	47	y
4	D	15	R	26	7	37	l	48	z
5	E	16	S	27	a	38	n	49	8
6	F	17	T	28	b	39	p	50	9
7	G	18	U	29	c	40	q	51	2
8	H	19	V	30	d	41	r	52	3
9	J	20	W	31	e	42	s		
10	K	21	Y	32	f	43	t		
11	L	22	Z	33	g	44	u		

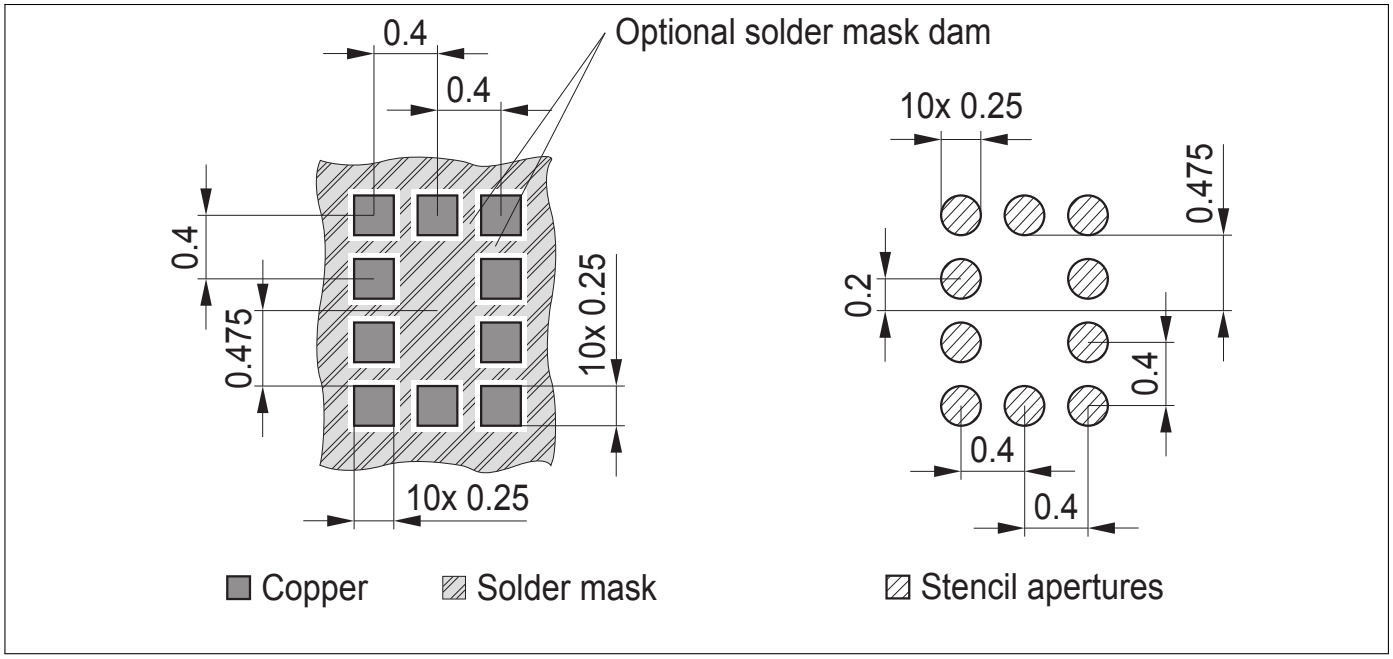

Figure 13: Footprint recommendation

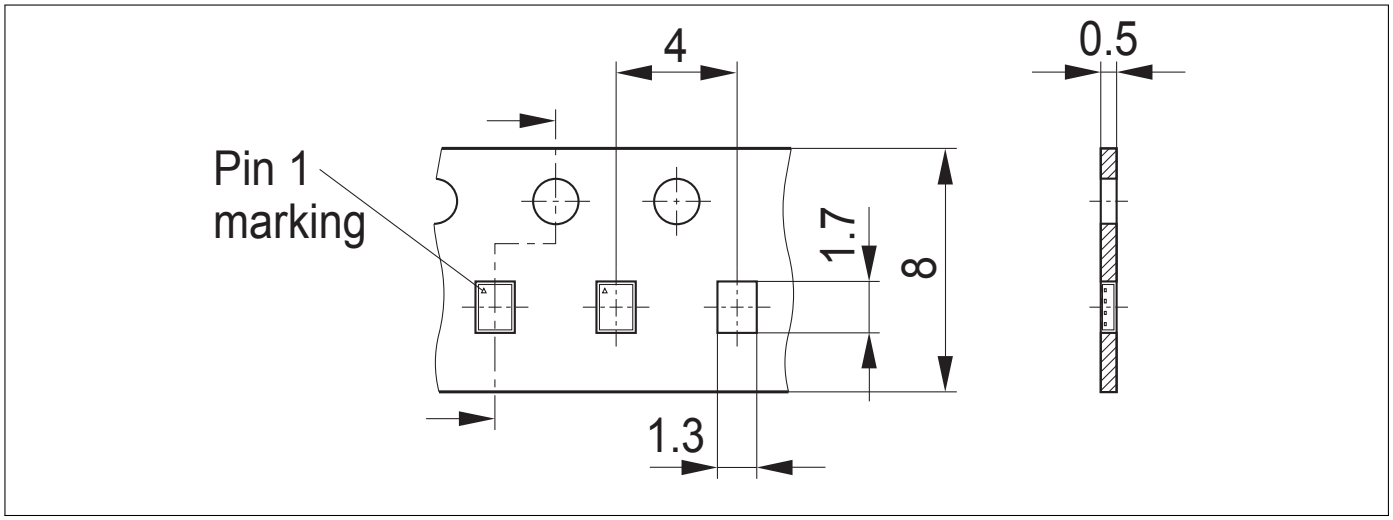

Figure 14: TSLP-10-2 Carrier tape

9 Revision History

Revision 2.1, 2019-11-29	
7,8,16	Updated Final Data Sheet on 1. S-Parameter updated 2. USID_Sel Swap Mode added

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