CS51221

Enhanced Voltage Mode PWM Controller

The CS51221 fixed frequency feed forward voltage mode PWM controller contains all of the features necessary for basic voltage mode operation. This PWM controller has been optimized for high frequency primary side control operation. In addition, this device includes such features as: Soft−Start, accurate duty cycle limit control, less than 50μA startup current, over and undervoltage protection, and bidirectional synchronization. The CS51221 is available in a 16 lead SOIC narrow surface mount package.

Features

- 1.0 MHz Frequency Capability
- Fixed Frequency Voltage Mode Operation, with Feed Forward
- Thermal Shutdown
- Undervoltage Lock−Out
- Accurate Programmable Max Duty Cycle Limit
- 1.0 A Sink/Source Gate Drive
- Programmable Pulse−By−Pulse Overcurrent Protection
- Leading Edge Current Sense Blanking
- 75 ns Shutdown Propagation Delay
- Programmable Soft−Start
- Undervoltage Protection
- Overvoltage Protection with Programmable Hysteresis
- Bidirectional Synchronization
- 25 ns GATE Rise and Fall Time (1.0 nF Load)
- 3.3 V 3% Reference Voltage Output
- Pb−Free Packages are Available*

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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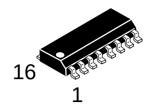
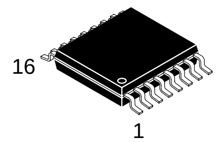
http://onsemi.com

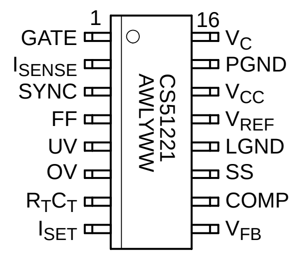


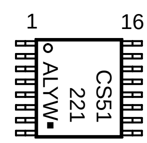
SOIC−16
D SUFFIX
CASE 751B



TSSOP−16
DTB SUFFIX
CASE 948F

PIN CONNECTIONS AND MARKING DIAGRAM





CS51221= Specific Device Code
A = Assembly Location
WL, L = Wafer Lot
YY, Y = Year
WW, W = Work Week
▪ = Pb−Free Package

ORDERING INFORMATION

Device	Package	Shipping†
CS51221ED16	SOIC−16	48 Units / Rail
CS51221ED16G	SOIC−16 (Pb−Free)	48 Units / Rail
CS51221EDR16	SOIC−16	2500 Tape & Reel
CS51221EDR16G	SOIC−16 (Pb−Free)	2500 Tape & Reel
CS51221EDTB16G	TSSOP−16 (Pb−Free)	96 Units / Rail
CS51221EDTB16R2G	TSSOP−16 (Pb−Free)	2500 Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

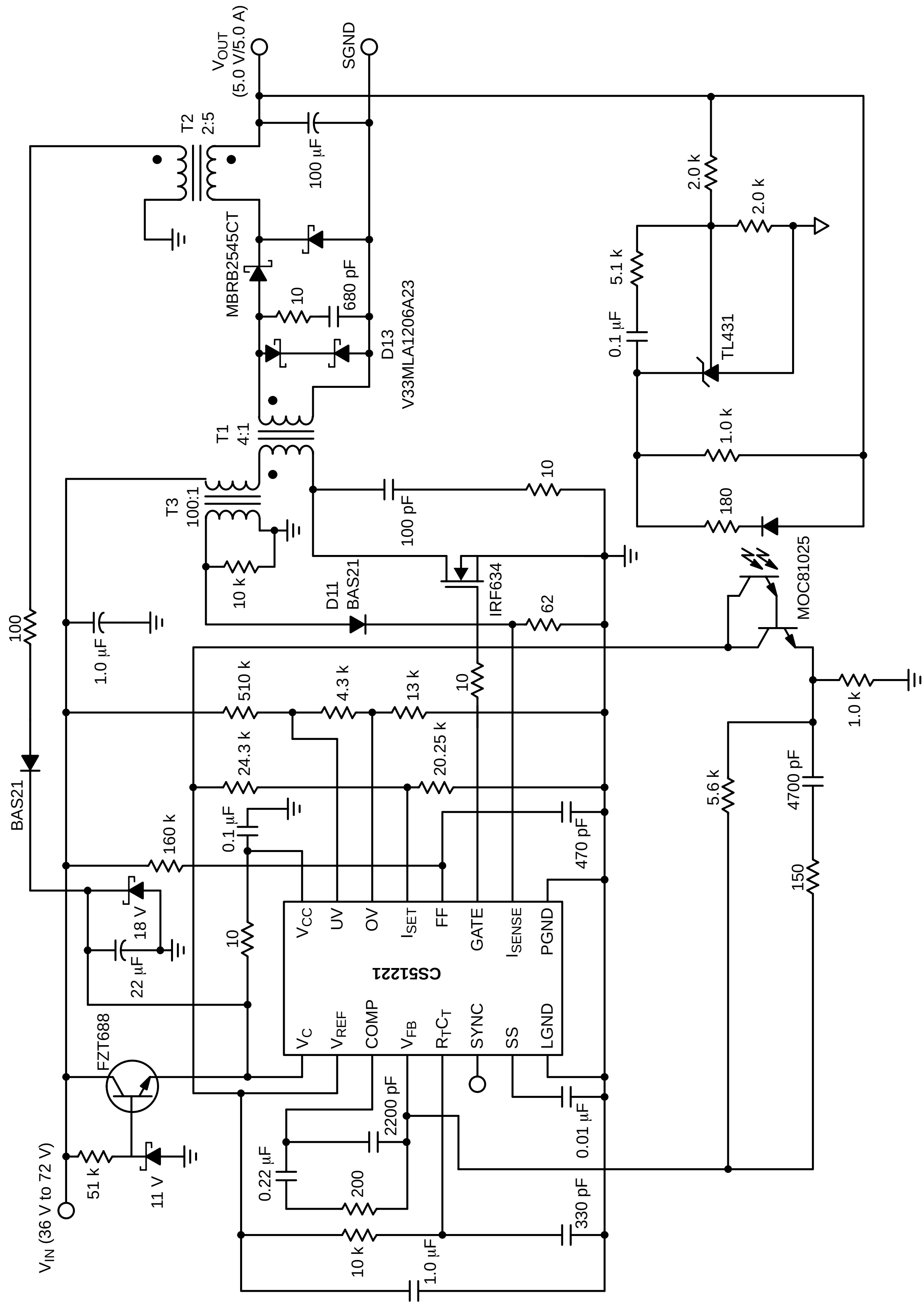


Figure 1. Application Diagram, 36 V−72 V to 5.0 V/5.0 A Converter

MAXIMUM RATINGS

Rating		Value	Unit
Operating Junction Temperature, T_J		Internally Limited	–
Lead Temperature Soldering:	Reflow: (SMD styles only) (Note 1)	230 peak	°C
Storage Temperature Range, T_S		−65 to +150	°C
ESD (Human Body Model)		2.0	kV

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

1. 60 second maximum above 183°C.

MAXIMUM RATINGS

Pin Name	Pin Symbol	V_{MAX}	V_{MIN}	I_{SOURCE}	I_{SINK}
Gate Drive Output	GATE	15 V	−0.3 V	1.0 A Peak, 200 mA DC	1.0 A Peak, 200 mA DC
Current Sense Input	I_{SENSE}	6.0 V	−0.3 V	1.0 mA	1.0 mA
Timing Resistor/Capacitor	R_TC_T	6.0 V	−0.3 V	1.0 mA	10 mA
Feed Forward	FF	6.0 V	−0.3 V	1.0 mA	25 mA
Error Amp Output	COMP	6.0 V	−0.3 V	10 mA	20 mA
Feedback Voltage	V_{FB}	6.0 V	−0.3 V	1.0 mA	1.0 mA
Sync Input	SYNC	6.0 V	−0.3 V	10 mA	10 mA
Undervoltage	UV	6.0 V	−0.3 V	1.0 mA	1.0 mA
Overvoltage	OV	6.0 V	−0.3 V	1.0 mA	1.0 mA
Current Set	I_{SET}	6.0 V	−0.3 V	1.0 mA	1.0 mA
Soft−Start	SS	6.0 V	−0.3 V	1.0 mA	10 mA
Logic Section Supply	V_{CC}	15 V	−0.3 V	10 mA	50 mA
Power Section Supply	V_C	15 V	−0.3 V	10 mA	1.0 A Peak, 200 mA DC
Reference Voltage	V_{REF}	6.0 V	−0.3 V	Internally Limited	10 mA
Power Ground	PGND	N/A	N/A	1.0 A Peak, 200 mA DC	N/A
Logic Ground	LGND	N/A	N/A	N/A	N/A

ELECTRICAL CHARACTERISTICS (−40°C < T_A < 85°C; −40°C < T_J < 125°C; 3.0 V < V_C < 15 V; 4.7 V < V_{CC} < 15 V; R_T = 12 k; C_T = 390 pF; unless otherwise specified.)

Characteristic	Test Conditions	Min	Typ	Max	Unit
Start/Stop Voltages					
Start Threshold	–	4.4	4.6	4.7	V
Stop Threshold	–	3.2	3.8	4.1	V
Hysteresis	Start−Stop	400	850	1400	mV
I_{CC} @ Startup	V_{CC} < UVL Start Threshold	–	38	75	μA
Supply Current					
I_{CC} Operating	–	–	9.5	14	mA
I_C Operating	1.0 nF Load on GATE	–	12	18	mA
I_C Operating	No Switching	–	2.0	4.0	mA

ELECTRICAL CHARACTERISTICS (−40°C < T_A < 85°C; −40°C < T_J < 125°C; 3.0 V < V_C < 15 V; 4.7 V < V_{CC} < 15 V; R_T = 12 k; C_T = 390 pF; unless otherwise specified.)

Characteristic	Test Conditions	Min	Typ	Max	Unit
Reference Voltage					
Total Accuracy	0 mA < I_{REF} < 2.0 mA	3.2	3.3	3.4	V
Line Regulation	–	–	6.0	20	mV
Load Regulation	0 mA < I_{REF} < 2.0 mA	–	6.0	15	mV
Noise Voltage	10 Hz < F < 10 kHz. Note 2	–	50	–	μV
Op Life Shift	T = 1000 Hrs. Note 2	–	4.0	20	mV
Fault Voltage	–	2.8	2.95	3.1	V
$V_{REF(OK)}$ Voltage	–	2.9	3.05	3.2	V
$V_{REF(OK)}$ Hysteresis	–	30	100	150	mV
Current Limit	–	2.0	40	100	mA
Error Amp					
Reference Voltage	V_{FB} = COMP	1.234	1.263	1.285	V
V_{FB} Input Current	V_{FB} = 1.2 V	–	1.3	2.0	μA
Open Loop Gain	Note 2	60	–	–	dB
Unity Gain Bandwidth	Note 2	1.5	–	–	MHz
COMP Sink Current	COMP = 1.4 V, V_{FB} = 1.45 V	3.0	12	32	mA
COMP Source Current	COMP = 1.4 V, V_{FB} = 1.15 V	1.0	1.6	2.0	mA
COMP High Voltage	V_{FB} = 1.15 V	2.8	3.1	3.4	V
COMP Low Voltage	V_{FB} = 1.45 V	75	125	300	mV
PSRR	Freq = 120 Hz. Note 2	60	85	–	dB
SS Clamp, V_{COMP}	SS = 1.4 V, V_{FB} = 0 V, I_{SET} = 2.0 V	1.3	1.4	1.5	V
COMP Max Clamp	Note 2	1.7	1.8	1.9	V
Oscillator					
Frequency Accuracy	–	260	273	320	kHz
Voltage Stability	–	–	1.0	2.0	%
Temperature Stability	−40°C < T_J < 125°C. (Note 2)	–	8.0	–	%
Max Frequency	Note 2	1.0	–	–	MHz
Duty Cycle	–	80	85	90	%
Peak Voltage	Note 2	1.94	2.0	2.06	V
Valley Clamp Voltage	–	0.9	0.95	1.0	V
Valley Voltage	Note 2	0.85	1.0	1.15	V
Discharge Current	–	0.85	1.0	1.15	mA
Synchronization					
Input Threshold	–	0.9	1.4	1.8	V
Output Pulse Width	–	200	320	450	ns
Output High Voltage	100 μA Load	2.1	2.5	2.8	V
Input Resistance	–	35	70	140	kΩ
SYNC to Drive Delay	Time from SYNC to GATE Shutdown	100	140	180	ns
Output Drive Current	R_{SYNC} = 1.0 Ω	1.0	1.5	2.25	mA

2. Guaranteed by design, not 100% tested in production.

ELECTRICAL CHARACTERISTICS ($-40°C < T_A < 85°C$; $-40°C < T_J < 125°C$; $3.0\ V < V_C < 15\ V$; $4.7\ V < V_{CC} < 15\ V$; $R_T = 12\ k$; $C_T = 390\ pF$; unless otherwise specified.)

Characteristic	Test Conditions	Min	Typ	Max	Unit
Gate Driver					
High Saturation Voltage	V_C − GATE, V_C = 10 V, I_{SOURCE} = 200 mA	−	1.5	2.0	V
Low Saturation Voltage	GATE − PGND, I_{SINK} = 200 mA	−	1.2	1.5	V
High Voltage Clamp	−	11	13.5	16	V
Output Current	1.0 nF Load. Note 3	−	1.0	1.25	A
Output UVL Leakage	GATE = 0 V	−	1.0	50	μA
Rise Time	1.0 nF Load, V_C = 20 V, 1.0 V < GATE < 9.0 V	−	60	100	ns
Fall Time	1.0 nF Load, V_C = 20 V, 9.0 V < GATE < 1.0 V	−	25	50	ns
Max Gate Voltage During UVL/Sleep	I_{GATE} = 500 μA	0.4	0.7	1.0	V
Feed Forward (FF)					
Discharge Voltage	I_{FF} = 2.0 mA	−	0.3	0.7	V
Discharge Current	FF = 1.0 V	2.0	16	30	mA
FF to GATE Delay	−	50	75	125	ns
Overcurrent Protection					
Overcurrent Threshold	I_{SET} = 0.5 V, Ramp I_{SENSE}	0.475	0.5	0.525	V
I_{SENSE} to GATE Delay	−	50	90	125	ns
External Voltage Monitors					
Overvoltage Threshold	OV Increasing	1.9	2.0	2.1	V
Overvoltage Hysteresis Current	OV = 2.15 V	10	12.5	15	μA
Undervoltage Threshold	UV Increasing	0.95	1.0	1.05	V
Undervoltage Hysteresis	−	25	75	125	mV
Soft−Start (SS)					
Charge Current	SS = 2.0 V	40	50	70	μA
Discharge Current	SS = 2.0 V	4.0	5.0	7.0	μA
Charge Voltage	−	2.8	3.0	3.4	V
Discharge Voltage	−	0.25	0.3	0.35	V
Soft−Start Clamp Offset	FF = 1.25 V	1.15	1.25	1.35	V
Soft−Start Fault Voltage	OV = 2.15 V or LV = 0.85 V	−	0.1	0.2	V
Blanking					
Blanking Time	−	50	150	250	ns
SS Blanking Disable Threshold	V_{FB} < 1.0	2.8	3.0	3.3	V
COMP Blanking Disable Threshold	V_{FB} < 1.0, SS > 3.0 V	2.8	3.0	3.3	V
Thermal Shutdown					
Thermal Shutdown	Note 3	125	150	180	°C
Thermal Hysteresis	Note 3	5.0	10	15	°C

3. Guaranteed by design, not 100% tested in production.

PACKAGE PIN DESCRIPTION

Package Pin #	Pin Symbol	Function
1	GATE	External power switch driver with 1.0 A peak capability. Rail to rail output occurs when the capacitive load is between 470 pF and 10 nF.
2	I_{SENSE}	Current sense comparator input.
3	SYNC	Bidirectional synchronization. Locks to highest frequency.
4	FF	PWM ramp.
5	UV	Undervoltage protection monitor.
6	OV	Overvoltage protection monitor.
7	R_TC_T	Timing resistor R_T and capacitor C_T determine oscillator frequency and maximum duty cycle, D_{MAX}.
8	I_{SET}	Voltage at this pin sets pulse−by−pulse overcurrent threshold.
9	V_{FB}	Feedback voltage input. Connected to the error amplifier inverting input.
10	COMP	Error amplifier output.
11	SS	Charging external capacitor restricts error amplifier output voltage during the power up or fault conditions.
12	LGND	Logic ground.
13	V_{REF}	3.3 V reference voltage output. Decoupling capacitor can be selected from 0.01 μF to 10 μF.
14	V_{CC}	Logic supply voltage.
15	PGND	Output power stage ground.
16	V_C	Output power stage supply voltage.

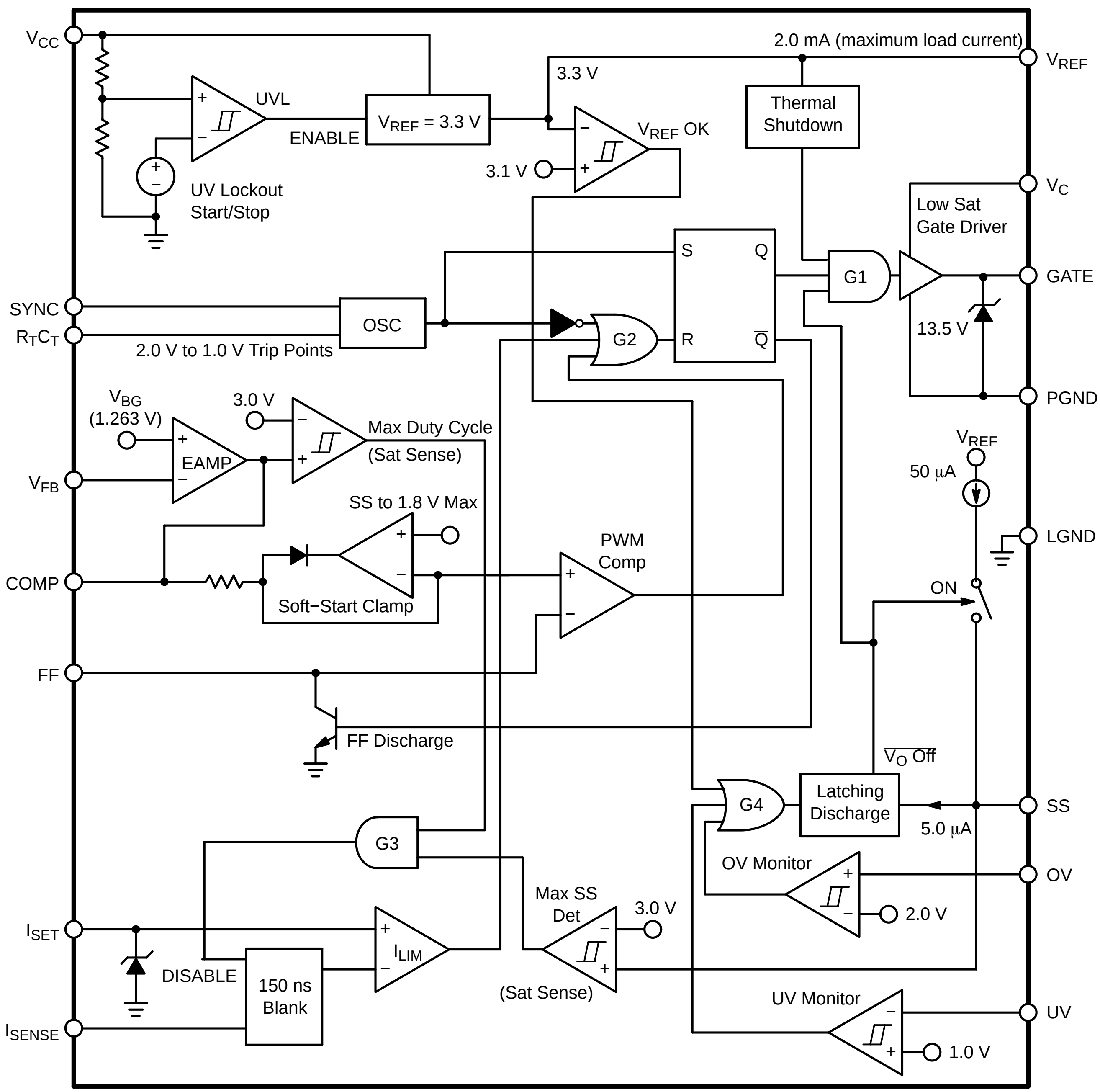


Figure 2. Block Diagram

APPLICATION INFORMATION

THEORY OF OPERATION

Feed Forward Voltage Mode Control

In conventional voltage mode control, the ramp signal has fixed rising and falling slope. The feedback signal is derived solely from the output voltage. Consequently, voltage mode control has inferior line regulation and audio susceptibility.

Feed forward voltage mode control derives the ramp signal from the input line, as shown in Figure 3. Therefore, the ramp of the slope varies with the input voltage. At the start of each switch cycle, the capacitor connected to the FF pin is charged through a resistor connected to the input voltage. Meanwhile, the Gate output is turned on to drive an external power switching device. When the FF pin voltage reaches the error amplifier output V_{COMP}, the PWM comparator turns off the Gate, which in turn opens the external switch. Simultaneously, the FF capacitor is quickly discharged to 0.3 V.

Overall, the dynamics of the duty cycle are controlled by both input and output voltages. As illustrated in Figure 4, with a fixed input voltage the output voltage is regulated solely by the error amplifier. For example, an elevated output voltage reduces V_{COMP} which in turn causes duty cycle to decrease. However, if the input voltage varies, the slope of the ramp signal will react immediately which provides a much improved line transient response. As an example shown in Figure 5, when the input voltage goes up, the rising edge of the ramp signal increases which reduces duty cycle to counteract the change.

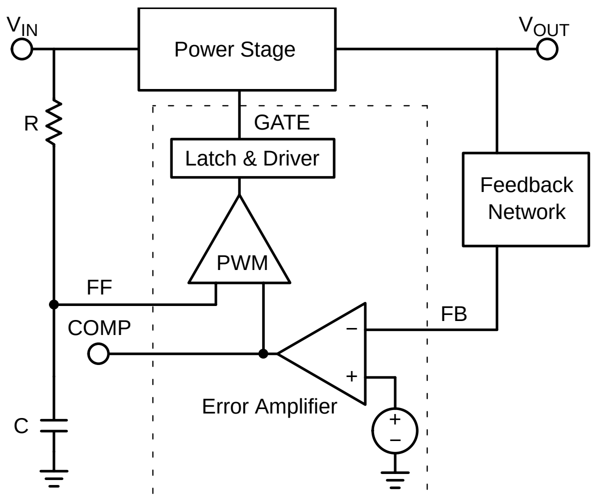


Figure 3. Feed Forward Voltage Mode Control

The feed forward feature can also be employed to provide a volt−second clamp, which limits the maximum product of input voltage and turn on time. This clamp is used in circuits, such as Forward and Flyback converter, to prevent the transformer from saturating. Calculations used in the design of the volt−second clamp are presented in the Design Guidelines section.

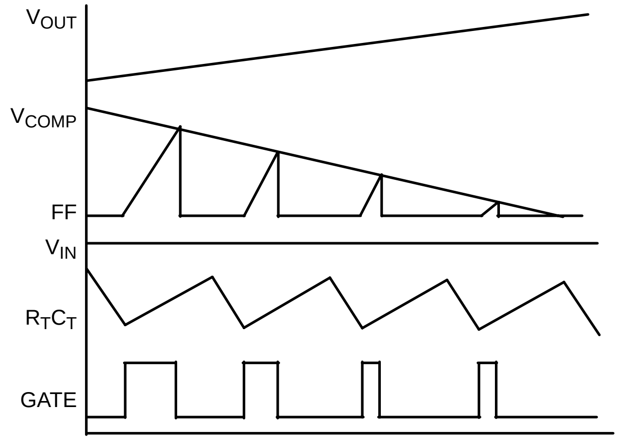


Figure 4. Pulse Width Modulated by Output Current with Constant Input Voltage

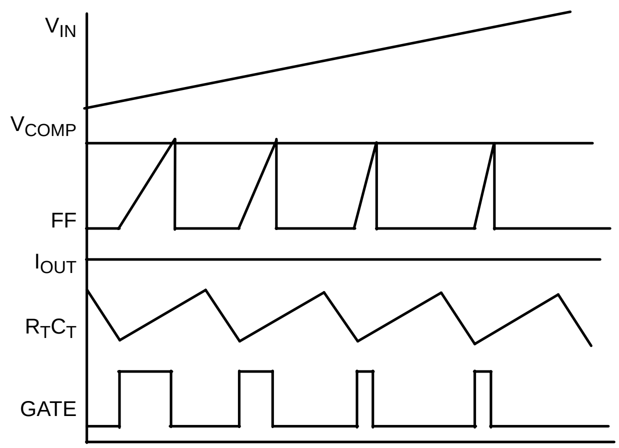


Figure 5. Pulse Width Modulated by Input Voltage with Constant Output Current

Powering the IC & UVL

The Undervoltage Lockout (UVL) comparator has two voltage references; the start and stop thresholds. During power−up, the UVL comparator disables V_{REF} (which in−turn disables the entire IC) until the controller reaches its V_{CC} start threshold. During power−down, the UVL comparator allows the controller to operate until the V_{CC} stop threshold is reached. The CS51221 requires only 50 μA during startup. The output stage is held at a low impedance state in lock out mode.

During power up and fault conditions, the Soft−Start clamps the Comp pin voltage and limits the duty cycle. The power up transition tends to generate temporary duty cycles much greater than the steady state value due to the low output voltage. Consequently, excessive current stresses often take place in the system. Soft−Start technique alleviates this problem by gradually releasing the clamp on the duty cycle to eliminate the in−rush current. The duration of the Soft−Start can be programmed through a capacitance connected to the SS pin. The constant charging current to the SS pin is 50 μA (typ).

The V_{REF} (ok) comparator monitors the 3.3 V V_{REF} output and latches a fault condition if V_{REF} falls below 3.1 V. The fault condition may also be triggered when the OV pin voltage rises above 2.0 V or the UV pin voltage falls below 1.0 V. The undervoltage comparator has a built−in hysteresis of 75 mV (typ). The hysteresis for the OV comparator is programmable through a resistor connected to the OV pin. When an OV condition is detected, the overvoltage hysteresis current of 12.5 μA (typ) is sourced from the pin.

In Figure 6, the fault condition is triggered by pulling the UV pin to the ground. Immediately, the SS capacitor is discharged with 5.0 μA of current (typ) and the GATE output is disabled until the SS voltage reaches the discharge voltage of 0.3 V (typ). The IC starts the Soft−Start transition again if the fault condition has recovered as shown in Figure 6. However, if the fault condition persists, the SS voltage will stay at 0.1 V until the removal of the fault condition.

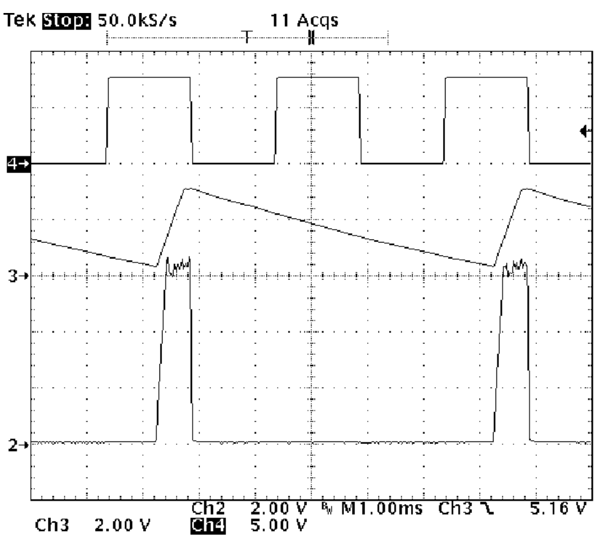


Figure 6. The Fault Condition Is Triggered when the UV Pin Voltage Falls Below 1.0 V. The Soft−Start Capacitor Is Discharged and the GATE Output Is Disabled. CH2: Envelop of GATE Output, CH3: SS Pin with 0.01 μF Capacitor, CH4: UV Pin

Current Sense and Overcurrent Protection

The current can be monitored by the I_{SENSE} pin to achieve pulse by pulse current limit. Various techniques, such as a using current sense resistor or current transformer, can be adopted to derive current signals. The voltage of the I_{SET} pin sets the threshold for maximum current. As shown in Figure 7, when the I_{SENSE} pin voltage exceeds the I_{SET} voltage, the current limit comparator will reset the GATE latch flip−flop to terminate the GATE pulse.

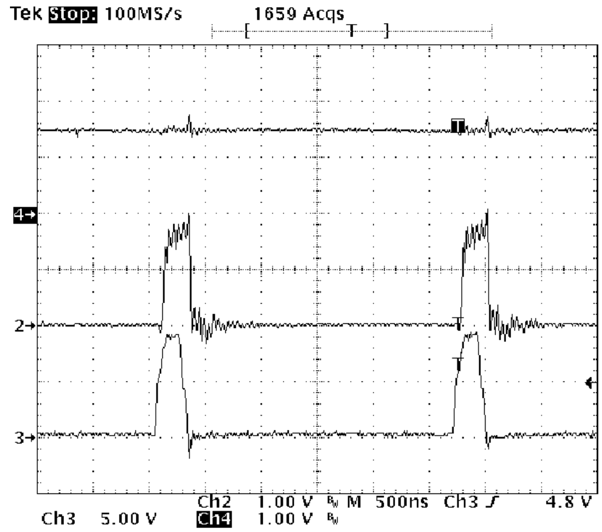


Figure 7. The GATE Output Is Terminated When the I_{SENSE} Pin Voltage Reaches the Threshold Set By the I_{SET} Pin. CH2: I_{SENSE} Pin, CH4: I_{SET} Pin, CH3: GATE Pin

The current sense signal is prone to leading edge spikes caused by the switching transition. A RC low−pass filter is usually applied to the current signals to avoid premature triggering. However, the low pass filter will inevitably change the shape of the current pulse and also add cost. The CS51221 uses leading edge blanking circuitry that blocks out the first 150 ns (typ) of each current pulse. This removes the leading edge spikes without altering the current waveform. The blanking is disabled during Soft−Start and when the V_{COMP} is saturated high so that the minimum on−time of the controller does not have the additional blanking period. The max SS detect comparator keeps the blanking function disabled until SS charges fully. The output of the max Duty Cycle detector goes high when the error amplifier output gets saturated high, indicating that the output voltage has fallen well below its regulation point and the power supply may be underload stress.

Oscillator and Synchronization

The switching frequency is programmable through a RC network connected to the R_TC_T Pin. As shown in Figure 8, when the R_TC_T pin reaches 2.0 V, the capacitor is discharged by a 1.0 mA current source and the Gate signal is disabled. When the R_TC_T pin decreases to 1.0 V, the Gate output is turned on and the discharge current is removed to let the R_TC_T pin ramp up. This begins a new switching cycle. The C_T charging time over the switch period sets the maximum duty cycle clamp which is programmable through the R_T value as shown in the Design Guidelines. At the beginning of each switching cycle, the SYNC pin generates a 2.5 V, 320 nS (typ) pulse. This pulse can be utilized to synchronize other power supplies.

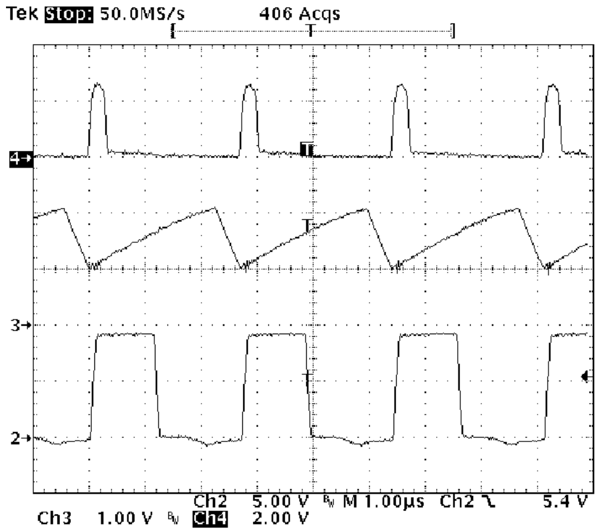


Figure 8. The SYNC Pin Generates a Sync Pulse at the Beginning of Each Switching Cycle. CH2: GATE Pin, CH3: R_TC_T, CH4: SYNC Pin

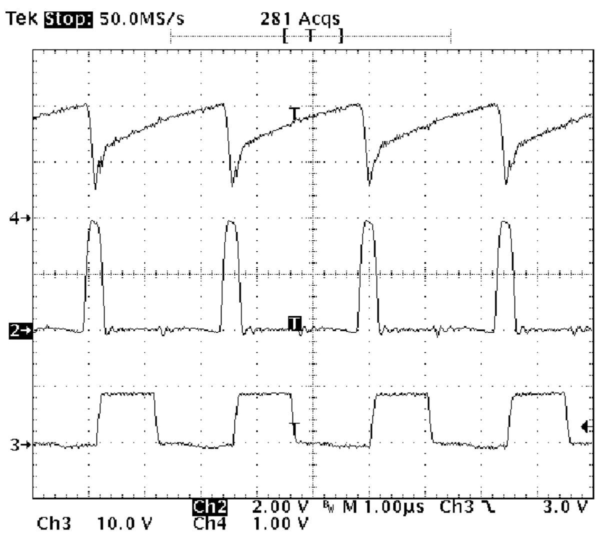


Figure 9. Operation with External Sync. CH2: SYNC Pin, CH3: GATE Pin, CH4: R_TC_T Pin

An external pulse signal can feed to the bidirectional SYNC pin to synchronize the switch frequency. For reliable operation, the sync frequency should be approximately 20% higher than free running IC frequency. As show in Figure 9, when the SYNC pin is triggered by an incoming signal, the IC immediately discharges C_T. The GATE signal is turned on once the R_TC_T pin reaches the valley voltage. Because of the steep falling edge, this valley voltage falls below the regular 1.0 V threshold. However, the R_TC_T pin voltage is then quickly raised by a clamp. When the R_TC_T pin reaches the 0.95 V (typ) Valley Clamp Voltage, the clamp is disconnected after a brief delay and C_T is charged through R_T.

DESIGN GUIDELINES

Switch Frequency and Maximum Duty Cycle Calculations

Oscillator timing capacitor, C_T, is charged by V_{REF} through R_T and discharged by an internal current source. During the discharge time, the internal clock signal sets the Gate output to the low state, thus providing a user selectable maximum duty cycle clamp. Charge and discharge times are determined by following general formulas;

$$t_C = R_TC_T \ln\left(\frac{(V_{REF} - V_{VALLEY})}{(V_{REF} - V_{PEAK})}\right)$$

$$t_d = R_TC_T \ln\left(\frac{(V_{REF} - V_{PEAK} - I_dR_T)}{(V_{REF} - V_{VALLEY} - I_dR_T)}\right)$$

where:

t_C = charging time;
t_d = discharging time;
V_{VALLEY} = valley voltage of the oscillator;
V_{PEAK} = peak voltage of the oscillator.

Substituting in typical values for the parameters in the above formulas, V_{REF} = 3.3 V, V_{VALLEY} = 1.0 V, V_{PEAK} = 2.0 V, I_d = 1.0 mA:

$$t_C = 0.57R_TC_T$$

$$t_d = R_TC_T \ln\left(\frac{1.3 - 0.001R_T}{2.3 - 0.001R_T}\right)$$

$$D_{max} = \frac{0.57}{0.57 + \ln\left(\frac{1.3-0.001R_T}{2.3-0.001R_T}\right)}$$

It is noticed from the equation that for the oscillator to function properly, R_T has to be greater than 2.3 k.

Select RC for Feed Forward Ramp

If the line voltage is much greater than the FF pin Peak Voltage, the charge current can be treated as a constant and is equal to V_{IN}/R. Therefore, the volt−second value is determined by:

$$V_{IN} \times T_{ON} = (V_{COMP} - V_{FF(d)}) \times R \times C$$

where:

V_{COMP} = COMP pin voltage;
$V_{FF(d)}$ = FF pin discharge voltage.

As shown in the equation, the volt−second clamp is set by the V_{COMP} clamp voltage which is equal to 1.8 V. In Forward or Flyback circuits, the volt−second clamp value is designed to prevent transformers from saturation.

In a buck or forward converter, volt−second is equal to

$$V_{IN} \times T_{ON} = \left(\frac{V_{OUT} \times T_S}{n}\right)$$

n = transformer turns ratio, which is a constant determined by the regulated output voltage, switching period and transformer turns ration (use 1.0 for buck converter). It is interesting to notice from the aforementioned two equations

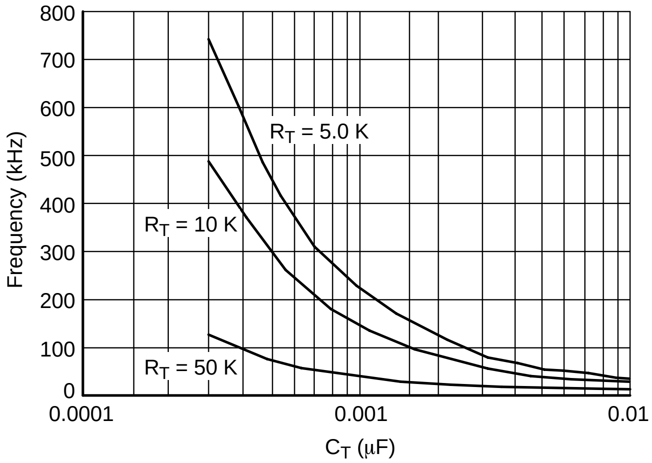


Figure 10. Typical Performance Characteristics, Oscillator Frequency vs. C_T

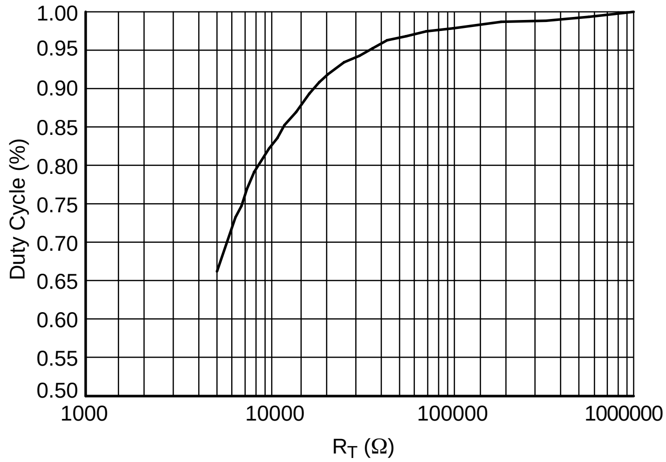


Figure 11. Typical Performance Characteristics, Oscillator Duty Cycle vs. R_T

that during steady state, V_{COMP} doesn't change for input voltage variations. This intuitively explains why FF voltage mode control has superior line regulation and line transient response. Knowing the nominal value of V_{IN} and T_{ON}, one can also select the value of RC to place V_{COMP} at the center of its dynamic range.

Select Feedback Voltage Divider

As shown in Figure 12, the voltage divider output feeds to the FB pin, which connects to the inverting input of the error amplifier. The non−inverting input of the error amplifier is connected to a 1.27 V (typ) reference voltage. The FB pin has an input current which has to be considered for accurate DC outputs. The following equation can be used to calculate the R1 and R2 value

$$\left(\frac{R2}{R1 + R2}\right) V_{OUT} = 1.27 - \nabla$$

where ∇ is the correction factor due to the existence of the FB pin input current Ier.

$$\nabla = (Ri + R1//R2)Ier$$

Ri = DC resistance between the FB pin and the voltage divider output.

Ier = V_{FB} input current, 1.3 μA typical.

Design Voltage Dividers for OV and UV Detection

In Figure 13, the voltage divider uses three resistors in series to set OV and UV threshold seen from the input voltage. The values of the resistors can be calculated from the following three equations, where the third equation is derived from OV hysteresis requirement.

$$V_{IN(LOW)} \times \left(\frac{R2 + R3}{R2 + R3 + R1}\right) = 1.0\ V \qquad (A)$$

$$V_{IN(HIGH)} \times \left(\frac{R3}{R2 + R3 + R1}\right) = 2.0\ V \qquad (B)$$

$$12.5\ \mu A \times (R1 + R2) = V_{HYST} \qquad (C)$$

where:

$V_{IN(LOW)}$, $V_{IN(HIGH)}$ = input voltage OV and UV threshold;

V_{HYST} = OV hysteresis seen at V_{IN}

It is self−evident from equation A and B that to use this design, $V_{IN(HIGH)}$ has to be two times greater than $V_{IN(LOW)}$. Otherwise, two voltage dividers have to be used to program OV and UV separately.

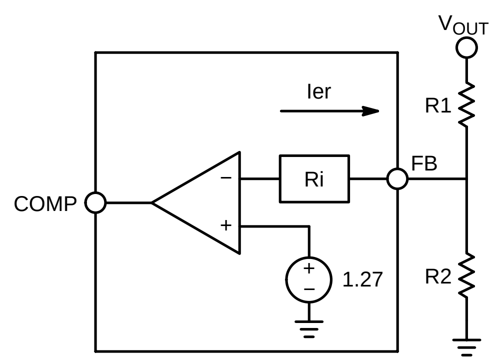


Figure 12. The Design of Feedback Voltage Divider Has to Consider the Error Amplifier Input Current

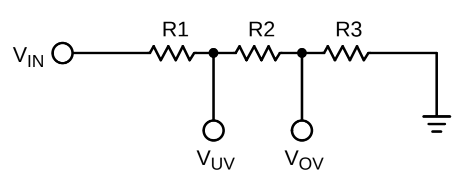
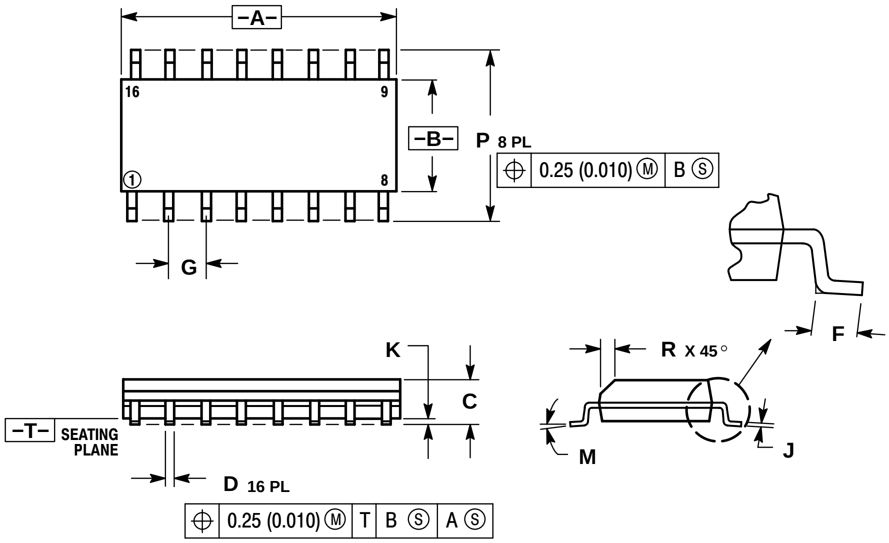


Figure 13. OV/UV Monitor Divider

PACKAGE DIMENSIONS

SOIC−16
D SUFFIX
CASE 751B−05
ISSUE J



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

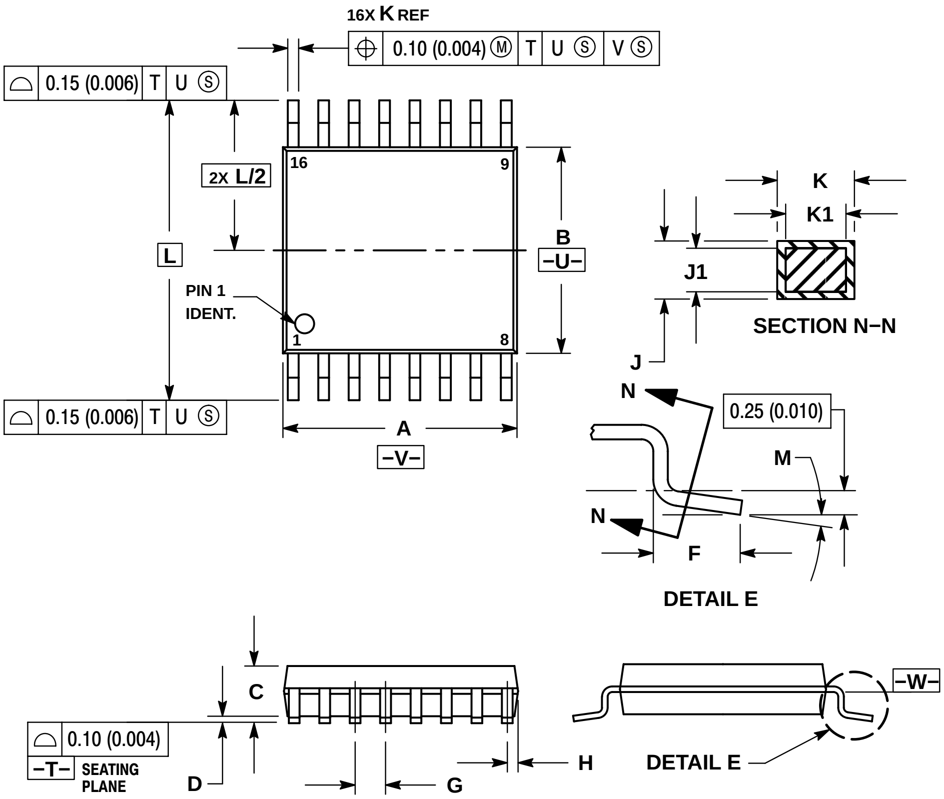
	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	9.80	10.00	0.386	0.393
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

PACKAGE THERMAL DATA

Parameter		SOIC−16	Unit
$R_{\theta JC}$	Typical	28	°C/W
$R_{\theta JA}$	Typical	115	°C/W

PACKAGE DIMENSIONS

TSSOP−16
CASE 948F−01
ISSUE A



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH. PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE −W−.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.90	5.10	0.193	0.200
B	4.30	4.50	0.169	0.177
C	−−−	1.20	−−−	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.18	0.28	0.007	0.011
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0 °	8 °	0 °	8 °

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