



## 14-Bit, Parallel Input Multiplying Digital-to-Analog Converter

### FEATURES

- $\pm 0.5$  LSB DNL
- $\pm 1$  LSB INL
- 14-Bit Monotonic
- Low Noise:  $10 \text{ nV}/\sqrt{\text{Hz}}$
- Low Power:  $I_{DD} = 2 \mu\text{A}$
- Analog Power Supply:  $+2.7 \text{ V}$  to  $+5.5 \text{ V}$
- 1.66 mA Full-Scale Current, with  $V_{REF} = 10 \text{ V}$
- Settling Time:  $0.5 \mu\text{s}$
- 4-Quadrant Multiplying Reference
- Reference Bandwidth: 8 MHz
- Reference Input:  $\pm 15 \text{ V}$
- Reference Dynamics:  $-105 \text{ dB THD}$
- SSOP-28 Package
- Industry-Standard Pin Configuration

### APPLICATIONS

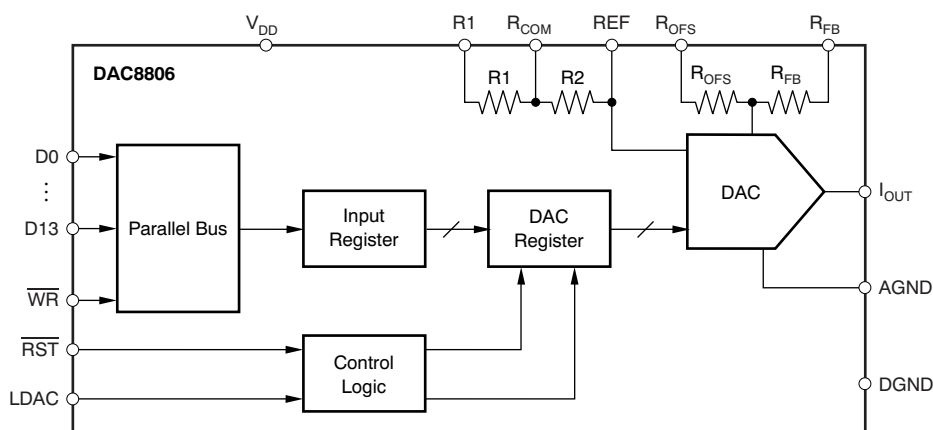
- Automatic Test Equipment
- Instrumentation
- Digitally Controlled Calibration
- Industrial Control PLCs

### DESCRIPTION

The DAC8806, a multiplying digital-to-analog converter (DAC), is designed to operate from a single 2.7 V to 5.5 V supply.

The applied external reference input voltage  $V_{REF}$  determines the full-scale output current. An internal feedback resistor ( $R_{FB}$ ) provides temperature tracking for the full-scale output when combined with an external, current-to-voltage (I/V) precision amplifier.

A parallel interface offers high-speed communications. The DAC8806 is packaged in a space-saving SSOP-28 package and has an industry-standard pinout.



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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

**ORDERING INFORMATION<sup>(1)</sup>**

PRODUCT	MINIMUM RELATIVE ACCURACY (LSB)	DIFFERENTIAL NONLINEARITY (LSB)	PACKAGE-LEAD (DESIGNATOR)	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
DAC8806I	±1	±1	DB-28 (SSOP)	–40°C to +85°C	DAC8806	DAC8806IDB	Tubes, 48
						DAC8806IDBR	Tape and Reel, 2000

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or see the TI web site at [www.ti.com](http://www.ti.com).

**ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>**

Over operating free-air temperature range (unless otherwise noted)

	DAC8806	UNIT
V <sub>DD</sub> to GND	–0.3 to +7	V
Digital input voltage to GND	–0.3 to +V <sub>DD</sub> + 0.3	V
V (I <sub>OUT</sub> ) to GND	–0.3 to +V <sub>DD</sub> + 0.3	V
Operating temperature range	–40 to +85	°C
REF, R <sub>OFS</sub> , R <sub>FB</sub> , R1, R <sub>COM</sub> to AGND, and DGND	±25	V
Storage temperature range	–65 to +150	°C
Junction temperature range (T <sub>J</sub> max)	+125	°C
Power dissipation	(T <sub>J</sub> max – T <sub>A</sub> )/R <sub>θJA</sub>	W
Thermal impedance, R <sub>θJA</sub>	55	°C/W
ESD rating	Human body model (HBM)	4000
	Charged device model (CDM)	1000

(1) Stresses above those listed under absolute maximum ratings may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability.

## ELECTRICAL CHARACTERISTICS

All specifications at  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ ,  $V_{\text{DD}} = +2.7\text{ V}$  to  $+5.5\text{ V}$ ,  $I_{\text{OUT}} = \text{virtual GND}$ ,  $\text{GND} = 0\text{ V}$ ,  $V_{\text{REF}} = 10\text{ V}$ , and  $T_{\text{A}}$  = full operating temperature, unless otherwise noted.

PARAMETER	CONDITIONS	DAC8806			UNITS
		MIN	TYP	MAX	
<b>STATIC PERFORMANCE</b>					
Resolution		14			Bits
Relative accuracy	DAC8806				$\pm 1$ LSB
Differential nonlinearity		$\pm 0.5$			$\pm 1$ LSB
Output leakage current	Data = 0000h, $T_{\text{A}} = +25^{\circ}\text{C}$				5 nA
Output leakage current	Data = 0000h, $T_{\text{A}} = T_{\text{MAX}}$				10 nA
Full-scale gain error	Unipolar, data = 3FFFh	1			$\pm 4$ LSB
	Bipolar, data = 3FFFh	1			$\pm 4$ LSB
Full-scale temperature coefficient		1			2 ppm/ $^{\circ}\text{C}$
Bipolar zero scale error		$\pm 1$			$\pm 3$ LSB
PSRR	Power-supply rejection ratio; $V_{\text{DD}} = 5\text{ V} \pm 10\%$	$\pm 0.1$			$\pm 1$ LSB/V
<b>OUTPUT CHARACTERISTICS<sup>(1)</sup></b>					
Output current		1.66			mA
Output capacitance	Code dependent	50			pF
<b>REFERENCE INPUT</b>					
$V_{\text{REF}}$ range		–15			15 V
$R_{\text{REF}}$	Input resistance (unipolar)	4.5			6 7.5 k $\Omega$
Input capacitance		5			pF
R1/R2	R1/R2 resistance (bipolar)	9			12 15 k $\Omega$
$R_{\text{OFS}}$ , $R_{\text{FB}}$	Feedback and offset resistance	9			12 15 k $\Omega$
<b>LOGIC INPUTS AND OUTPUT<sup>(1)</sup></b>					
Input low voltage	$V_{\text{IL}}$	$V_{\text{DD}} = +2.7\text{ V}$			0.6 V
	$V_{\text{IL}}$	$V_{\text{DD}} = +5\text{ V}$			0.8 V
Input high voltage	$V_{\text{IH}}$	$V_{\text{DD}} = +2.7\text{ V}$	2.1		V
	$V_{\text{IH}}$	$V_{\text{DD}} = +5\text{ V}$	2.4		V
Input leakage current	$I_{\text{IL}}$		0.001		1 $\mu\text{A}$
Input capacitance	$C_{\text{IL}}$				8 pF
<b>INTERFACE TIMING, <math>V_{\text{DD}} = +5.0\text{V}</math><sup>(1)</sup> (See Figure 40 and Table 1)</b>					
	$t_{\text{DS}}$	Data to $\overline{\text{WR}}$ setup time	20		ns
	$t_{\text{DH}}$	Data to $\overline{\text{WR}}$ hold time	0		ns
	$t_{\text{WR}}$	$\overline{\text{WR}}$ pulse width	20		ns
	$t_{\text{LDAC}}$	LDAC pulse width	20		ns
Data setup time	$t_{\text{RST}}$	$\overline{\text{RST}}$ pulse width	20		ns
Data hold time	$t_{\text{LWD}}$	$\overline{\text{WR}}$ to LDAC delay time	0		ns
<b>INTERFACE TIMING, <math>V_{\text{DD}} = +2.7\text{V}</math><sup>(1)</sup> (See Figure 40 and Table 1)</b>					
	$t_{\text{DS}}$	Data to $\overline{\text{WR}}$ setup time	35		ns
	$t_{\text{DH}}$	Data to $\overline{\text{WR}}$ hold time	0		ns
	$t_{\text{WR}}$	$\overline{\text{WR}}$ pulse width	35		ns
	$t_{\text{LDAC}}$	LDAC pulse width	35		ns
Data setup time	$t_{\text{RST}}$	$\overline{\text{RST}}$ pulse width	35		ns
Data hold time	$t_{\text{LWD}}$	$\overline{\text{WR}}$ to LDAC delay time	0		ns

(1) Specified by design and characterization; not production tested.

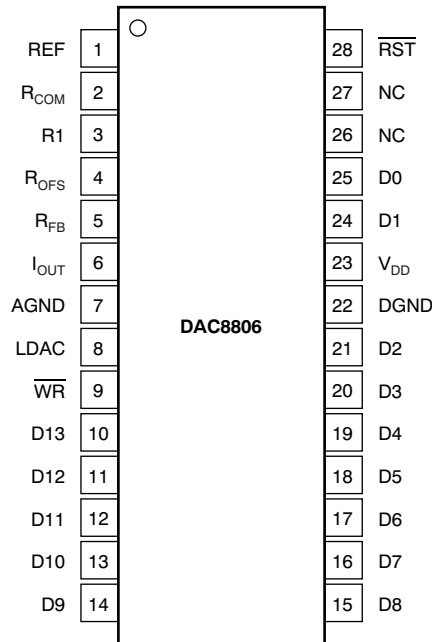
**ELECTRICAL CHARACTERISTICS (continued)**

All specifications at  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ ,  $V_{\text{DD}} = +2.7\text{ V}$  to  $+5.5\text{ V}$ ,  $I_{\text{OUT}} = \text{virtual GND}$ ,  $\text{GND} = 0\text{ V}$ ,  $V_{\text{REF}} = 10\text{ V}$ , and  $T_{\text{A}} = \text{full operating temperature}$ , unless otherwise noted.

PARAMETER	CONDITIONS	DAC8806			UNITS
		MIN	TYP	MAX	
<b>POWER REQUIREMENTS</b>					
$V_{\text{DD}}$		2.7		5.5	V
$I_{\text{DD}}$ (normal operation)	Logic inputs = 0V			5	$\mu\text{A}$
$V_{\text{DD}} = +4.5\text{ V}$ to $+5.5\text{ V}$	$V_{\text{IH}} = V_{\text{DD}}$ and $V_{\text{IL}} = \text{GND}$		3	5	$\mu\text{A}$
$V_{\text{DD}} = +2.7\text{ V}$ to $+3.6\text{ V}$	$V_{\text{IH}} = V_{\text{DD}}$ and $V_{\text{IL}} = \text{GND}$		1	2.5	$\mu\text{A}$
<b>AC CHARACTERISTICS<sup>(2)</sup></b>					
Output current settling time			0.5		$\mu\text{s}$
Reference multiplying BW	$V_{\text{REF}} = 5\text{ V}_{\text{PP}}$ , Data = 3FFFh		8		MHz
DAC glitch impulse	$V_{\text{REF}} = 0\text{ V}$ to $10\text{ V}$ , Data = 1FFFh to 2000h to 1FFFh		2		nV–s
Feedthrough error $V_{\text{OUT}}/V_{\text{REF}}$	Data = 0000h, $V_{\text{REF}} = 10\text{ kHz}$ ; $\pm 10\text{ V}_{\text{PP}}$		-70		dB
Digital feedthrough	$L_{\text{DAC}} = \text{logic low}$ , $V_{\text{REF}} = -10\text{ V}$ to $+10\text{ V}$ Any code change		2		nV–s
Total harmonic distortion	$V_{\text{REF}} = 6\text{ V}_{\text{RMS}}$ , Data = 3FFF, $f = 1\text{ kHz}$		-105		dB
Output spot noise voltage			10		$\text{nV}/\sqrt{\text{Hz}}$

(2) Specified by design and characterization; not production tested.

**PIN ASSIGNMENTS**



**TERMINAL FUNCTIONS**

PIN #	NAME	DESCRIPTION
1	REF	Reference input and 4-quadrant Resistor (R2).
2	R <sub>COM</sub>	Center tap of two 4-quadrant resistors (R1 and R2).
3	R1	4-quadrant resistor (R1).
4	R <sub>OFS</sub>	Bipolar offset resistor
5	R <sub>FB</sub>	Internal matching feedback resistor
6	I <sub>OUT</sub>	DAC current output
7	AGND	Analog ground
8	LDAC	Digital input load DAC control. When LDAC is high, data is loaded from input register into a DAC register, updating the DAC output.
9	WR	Write control digital input. Active low. When WR is taken to logic low, data is loaded from the digital input pins (D0–D13) into a14-bit input register.
10–21	D13–D2	Digital input data bits. D13 is MSB.
22	DGND	Digital ground
23	V <sub>DD</sub>	Positive power supply
24, 25	D1, D0	Digital Input data bits. D0 is LSB.
26, 27	NC	No connection
28	RST	Reset. Active low. When RST is taken to logic low, the DAC register is set to zero code, resulting in the DAC output being set to 0 V.

**TYPICAL CHARACTERISTICS:  $V_{DD} = +5V$**

At  $T_A = +25^\circ\text{C}$ , unless otherwise noted.

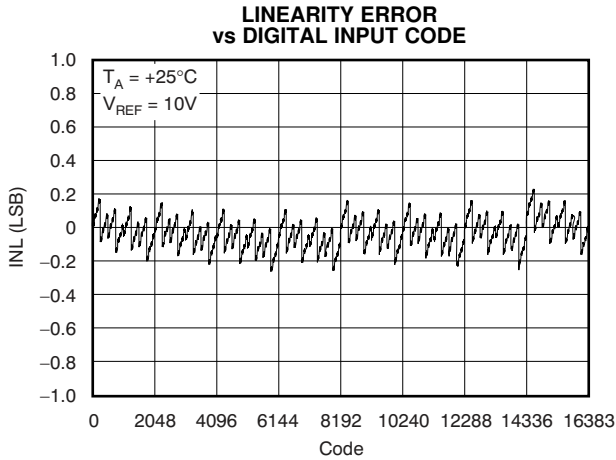


Figure 1.

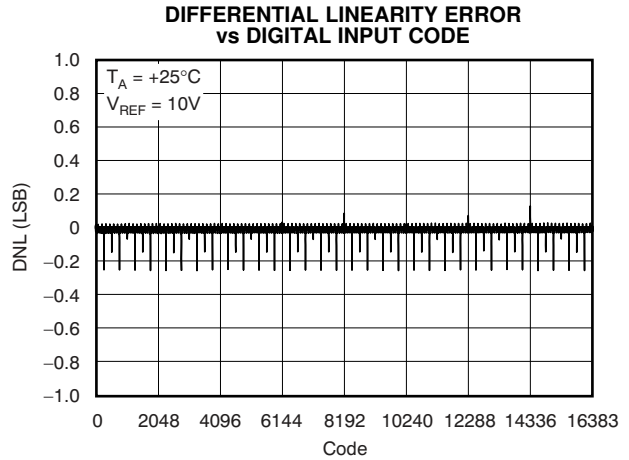


Figure 2.

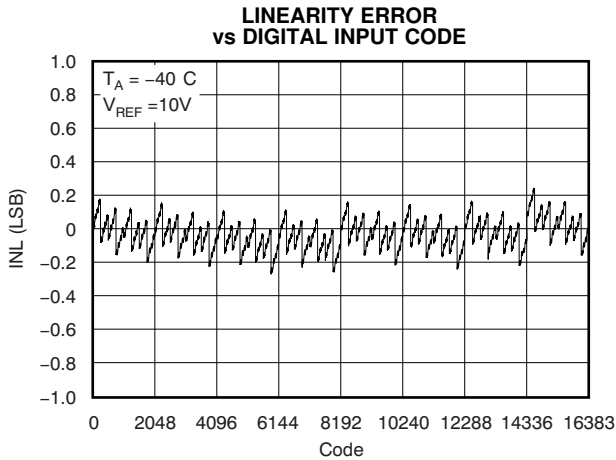


Figure 3.

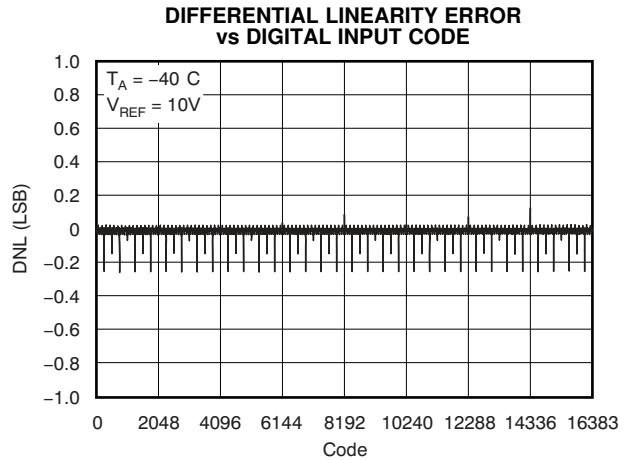


Figure 4.

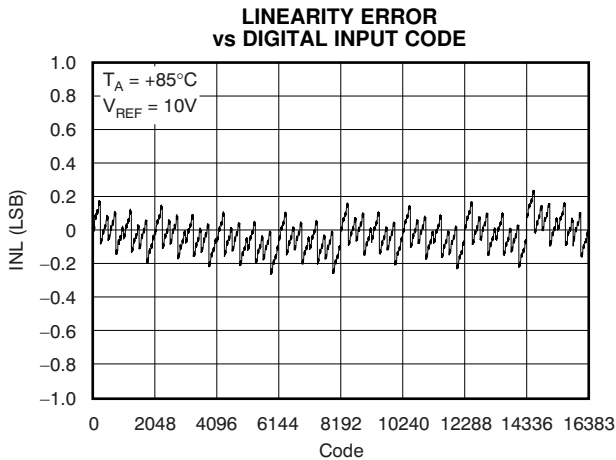


Figure 5.

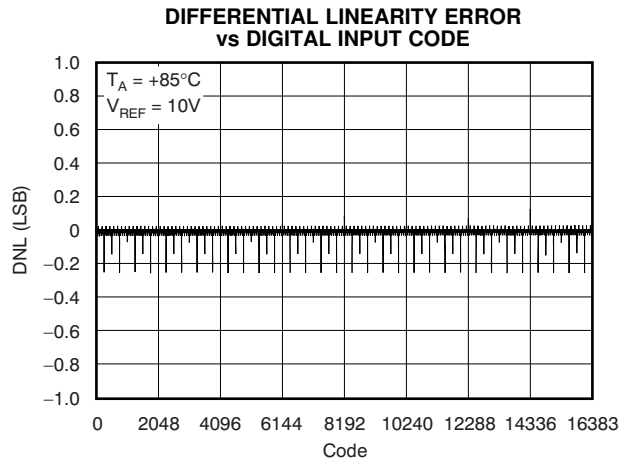


Figure 6.

**TYPICAL CHARACTERISTICS:  $V_{DD} = +5V$  (continued)**

At  $T_A = +25^\circ C$ , unless otherwise noted.

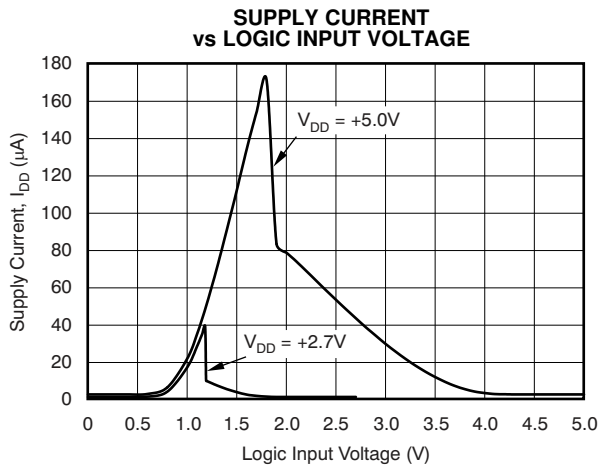


Figure 7.

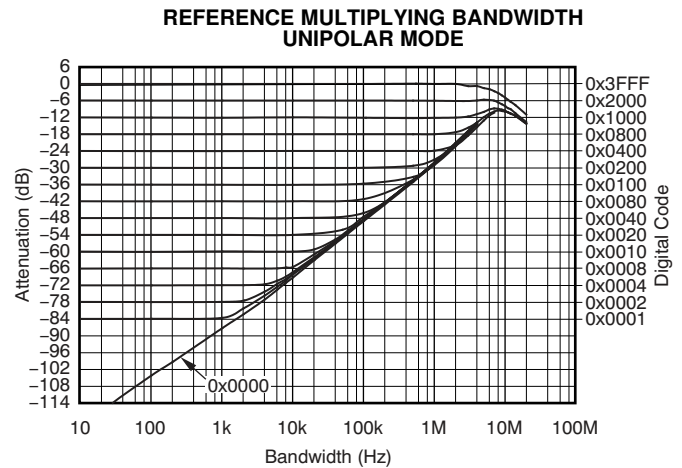


Figure 8.

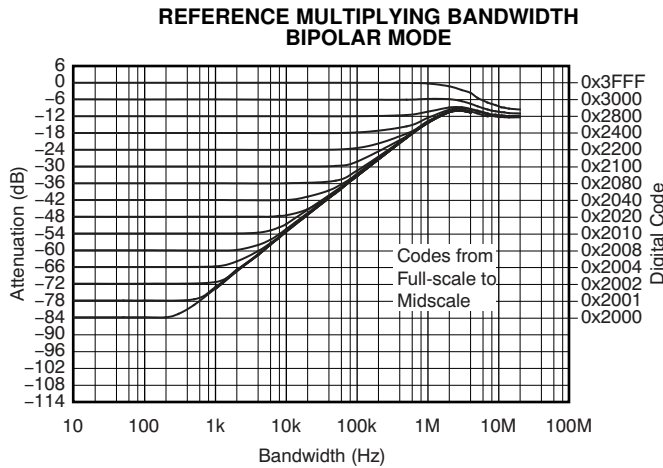


Figure 9.

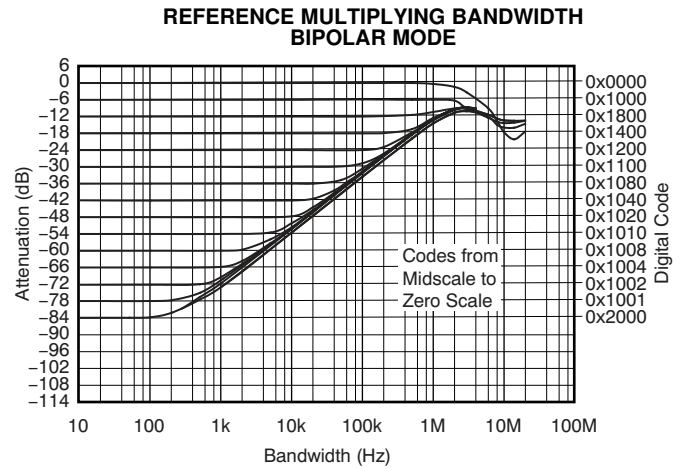


Figure 10.

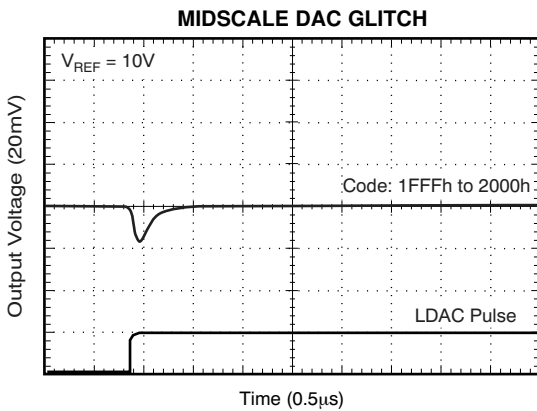


Figure 11.

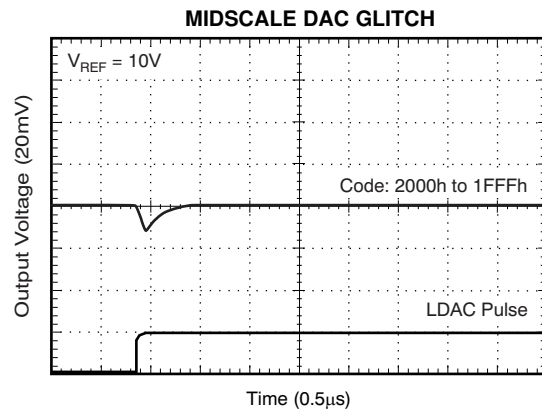
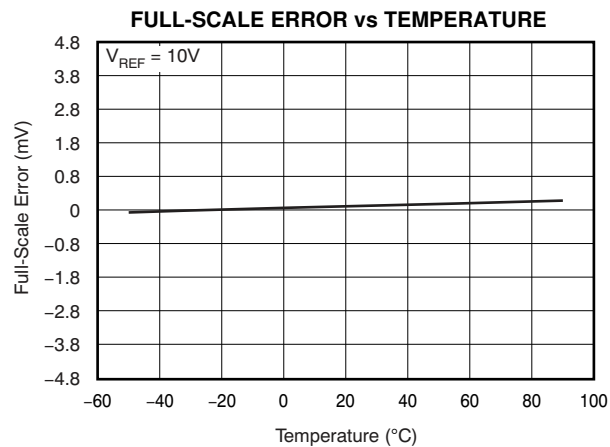


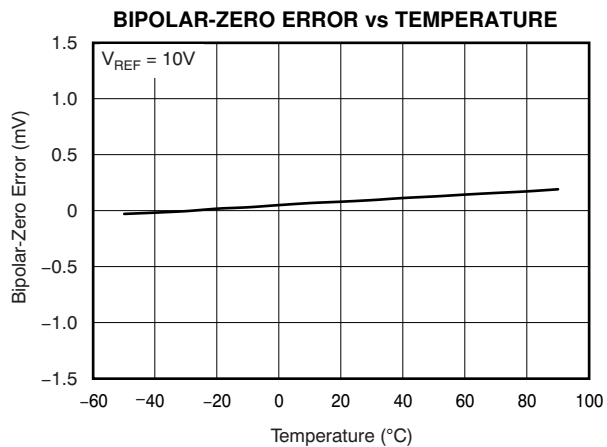
Figure 12.

**TYPICAL CHARACTERISTICS:  $V_{DD} = +5V$  (continued)**

At  $T_A = +25^\circ C$ , unless otherwise noted.



**Figure 13.**



**Figure 14.**

**TYPICAL CHARACTERISTICS:  $V_{DD} = +2.7V$**

At  $T_A = +25^\circ C$ , unless otherwise noted.

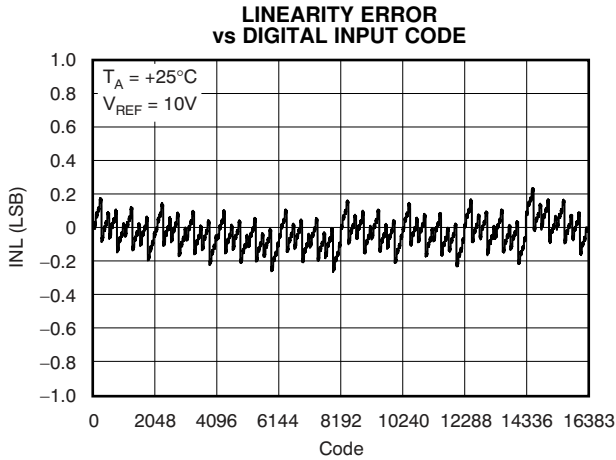


Figure 15.

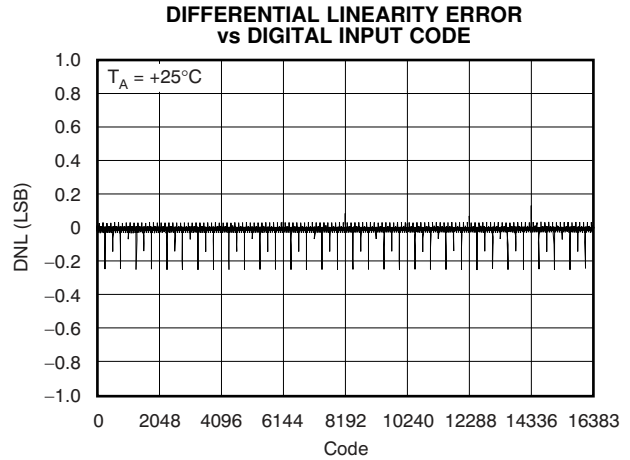


Figure 16.

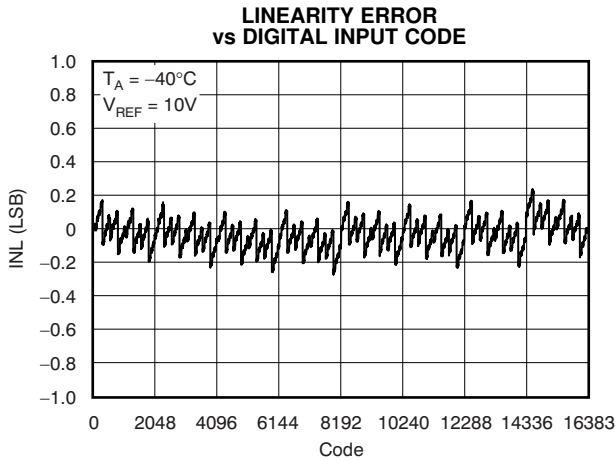


Figure 17.

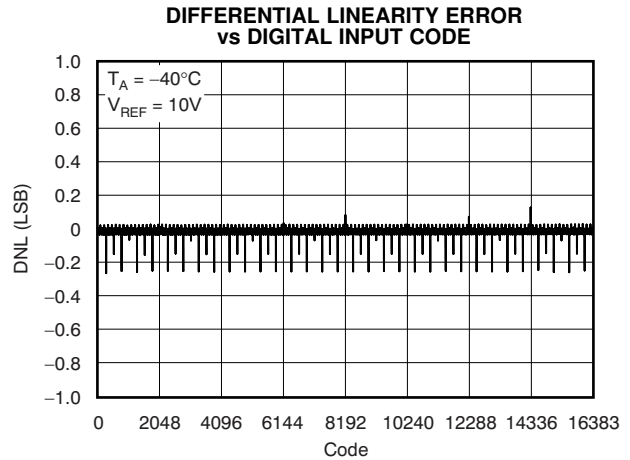


Figure 18.

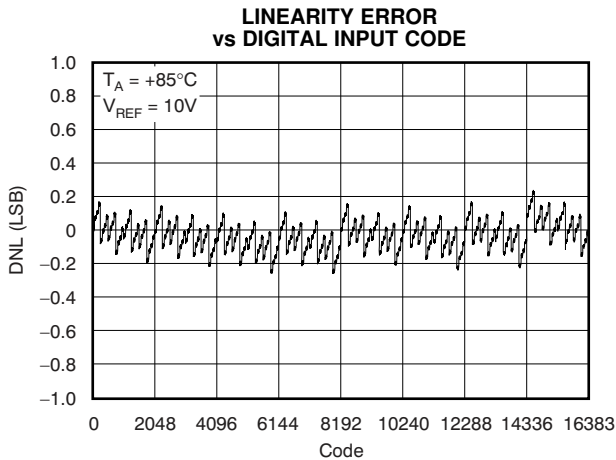


Figure 19.

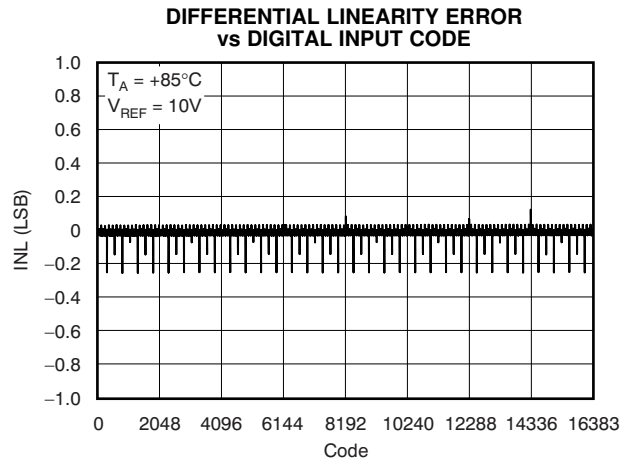
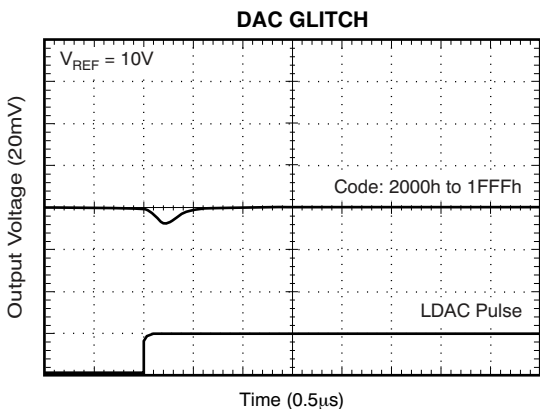


Figure 20.

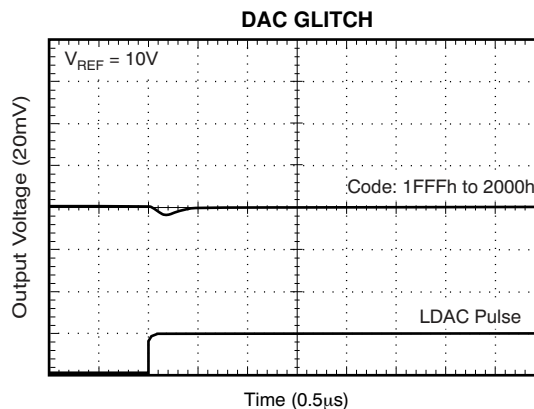


**TYPICAL CHARACTERISTICS:  $V_{DD} = +2.7V$  (continued)**

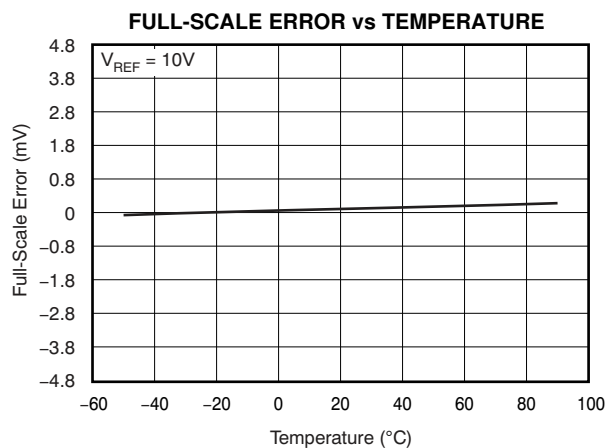
At  $T_A = +25^\circ C$ , unless otherwise noted.



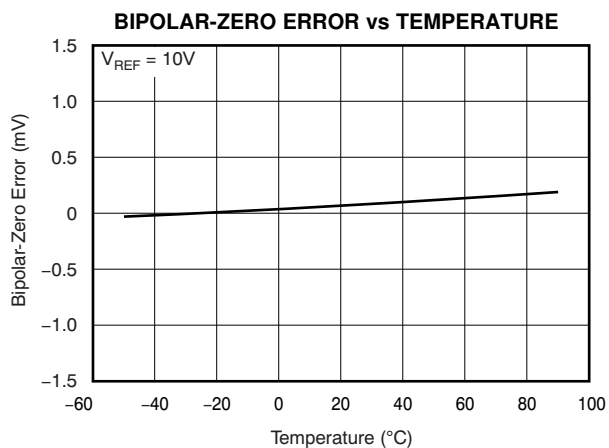
**Figure 21.**



**Figure 22.**



**Figure 23.**



**Figure 24.**

**TYPICAL CHARACTERISTICS**

At  $T_A = +25^\circ\text{C}$ , unless otherwise noted.

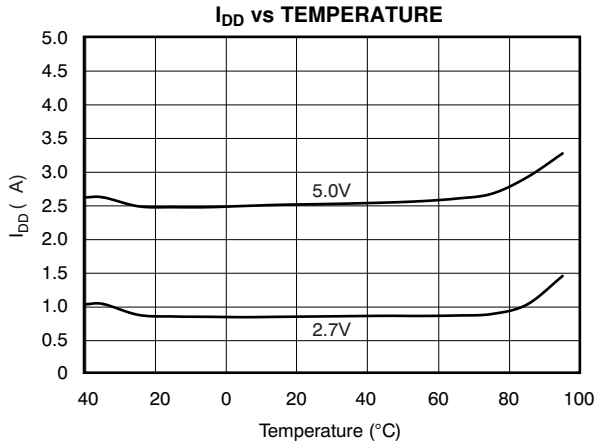


Figure 25.

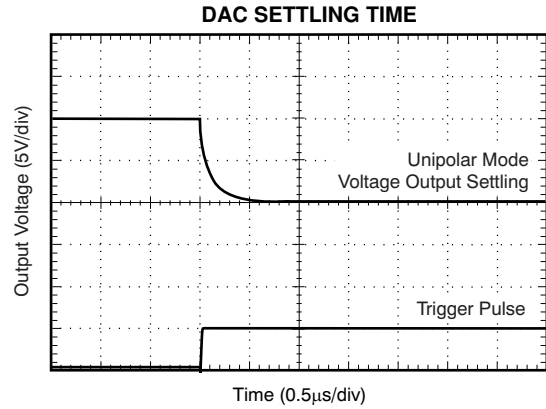


Figure 26.

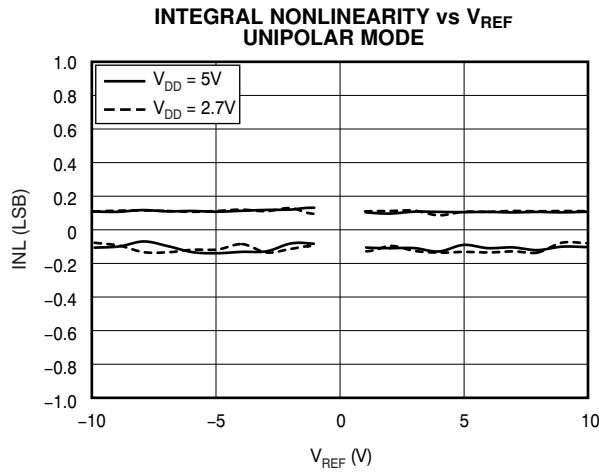


Figure 27.

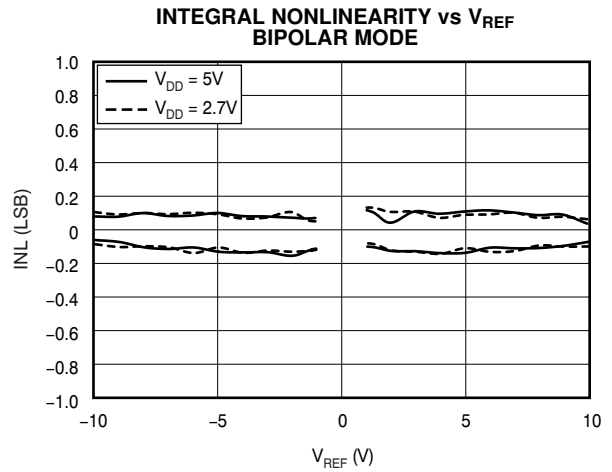


Figure 28.

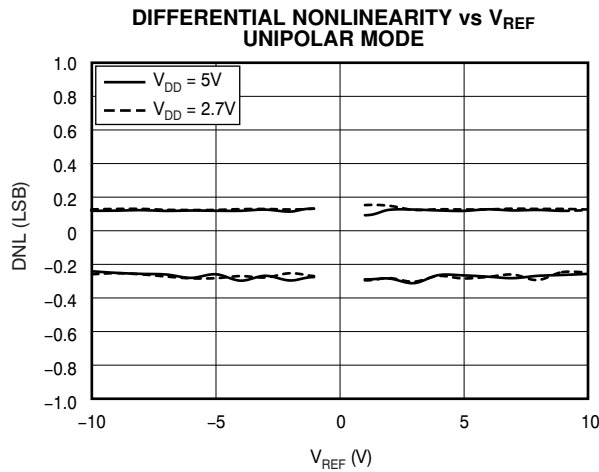


Figure 29.

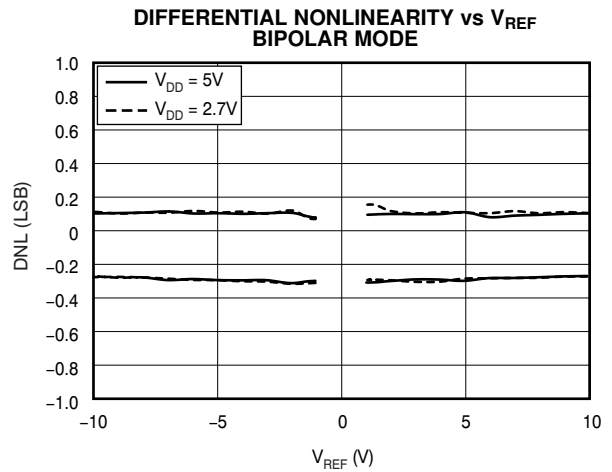


Figure 30.

TYPICAL CHARACTERISTICS (continued)

At  $T_A = +25^\circ\text{C}$ , unless otherwise noted.

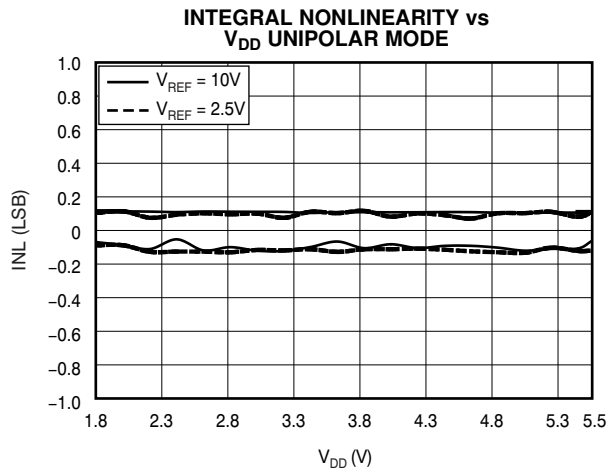


Figure 31.

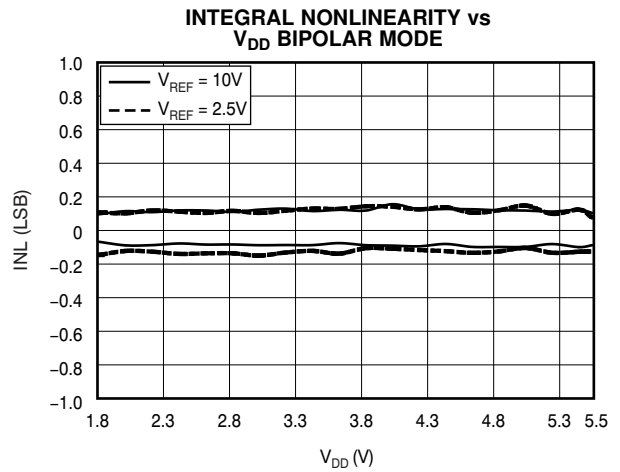


Figure 32.

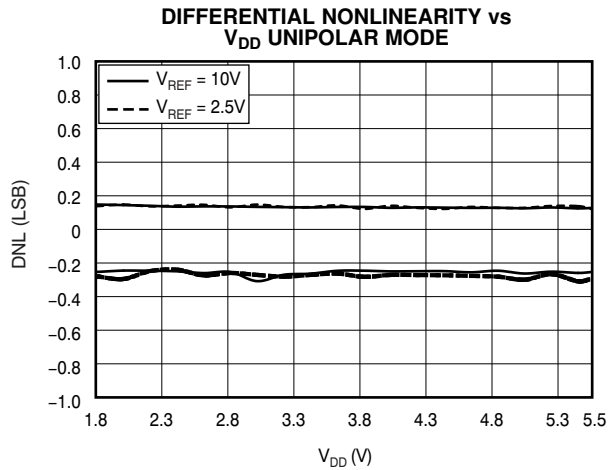


Figure 33.

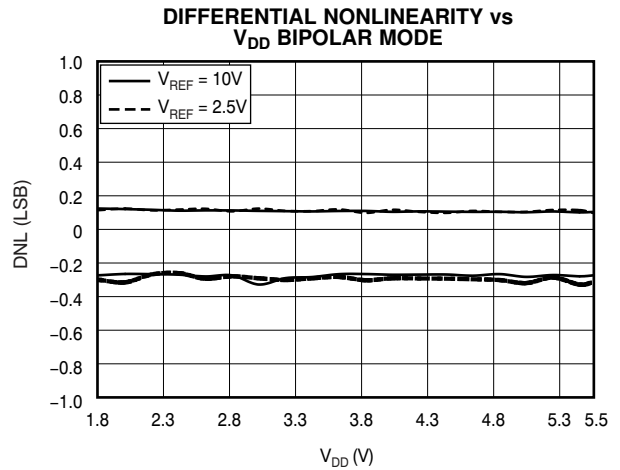


Figure 34.

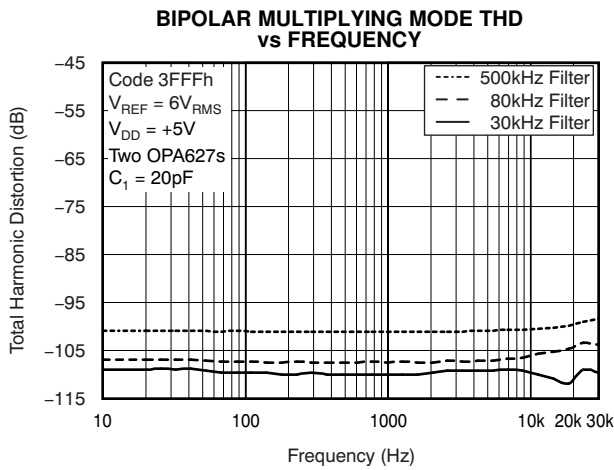


Figure 35.

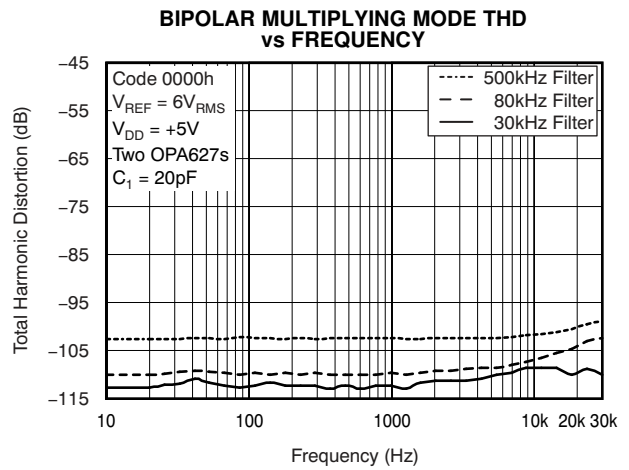


Figure 36.

**TYPICAL CHARACTERISTICS (continued)**

At T<sub>A</sub> = +25°C, unless otherwise noted.

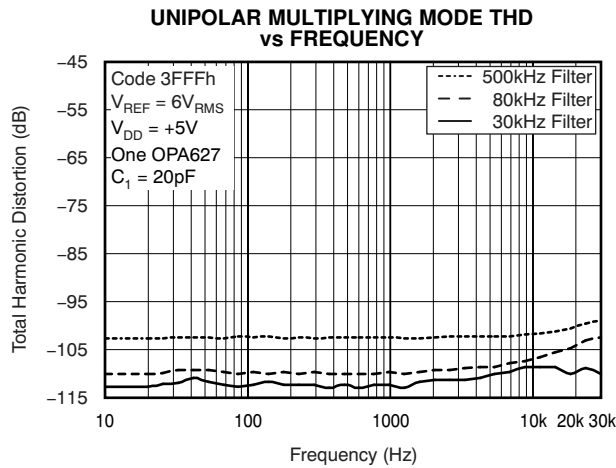


Figure 37.

**THEORY OF OPERATION**

The DAC8806 is a multiplying, single-channel current output, 14-bit DAC. The architecture, illustrated in Figure 38, is an R-2R ladder configuration with the three MSBs segmented. Each 2R leg of the ladder is either switched to GND or to the I<sub>OUT</sub> terminal. The I<sub>OUT</sub> terminal of the DAC is held at a virtual GND potential by the use of an external I/V converter op amp. The R-2R ladder is connected to an external reference input (V<sub>REF</sub>) that determines the DAC full-scale current. The R-2R ladder presents a code independent load impedance to the external reference of 6 kΩ ±25%. The external reference voltage can vary in a range of –10 V to +10 V, thus providing bipolar I<sub>OUT</sub> current operation. By using an external I/V converter op amp and the R<sub>FB</sub> resistor in the DAC8806, an output voltage range of –V<sub>REF</sub> to +V<sub>REF</sub> can be generated.

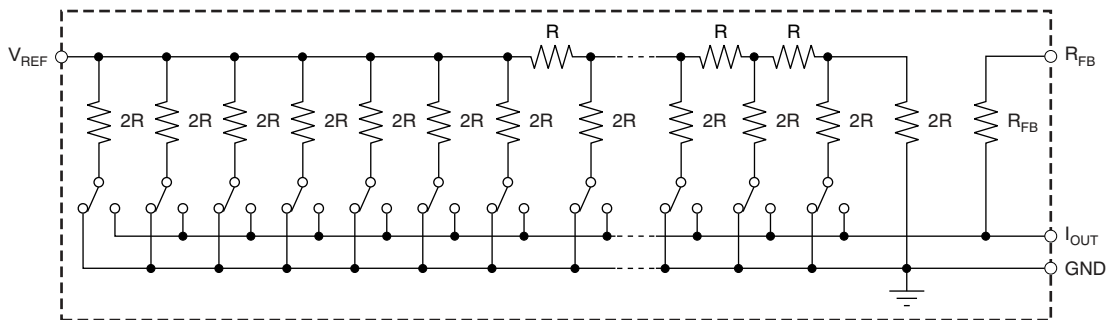


Figure 38. Equivalent R-2R DAC Circuit

The DAC output voltage is determined by V<sub>REF</sub> and the digital data (D) according to Equation 1:

$$V_{OUT} = -V_{REF} \times \frac{D}{16384} \tag{1}$$

Each DAC code determines the 2R-leg switch position to either GND or I<sub>OUT</sub>. The external I/V converter op amp noise gain will also change because the DAC output impedance (as seen looking into the I<sub>OUT</sub> terminal) changes versus code. Because of this, the external I/V converter op amp must have a sufficiently low offset voltage such that the amplifier offset is not modulated by the DAC I<sub>OUT</sub> terminal impedance change. External op amps with large offset voltages can produce INL errors in the transfer function of the DAC8806 because of offset modulation versus DAC code. For best linearity performance of the DAC8806, an op amp (OPA277) is recommended; see Figure 39. This circuit allows V<sub>REF</sub> to swing from –10 V to +10 V.

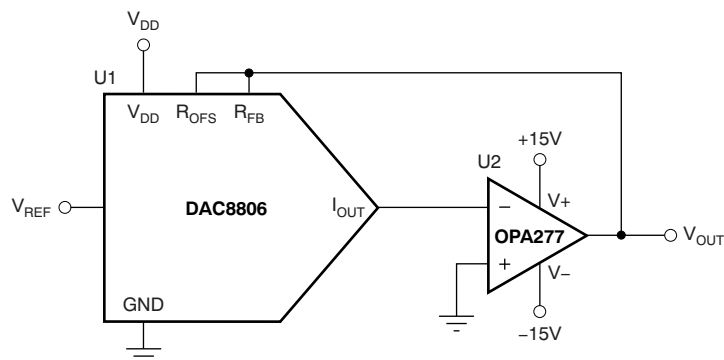


Figure 39. Voltage Output Configuration

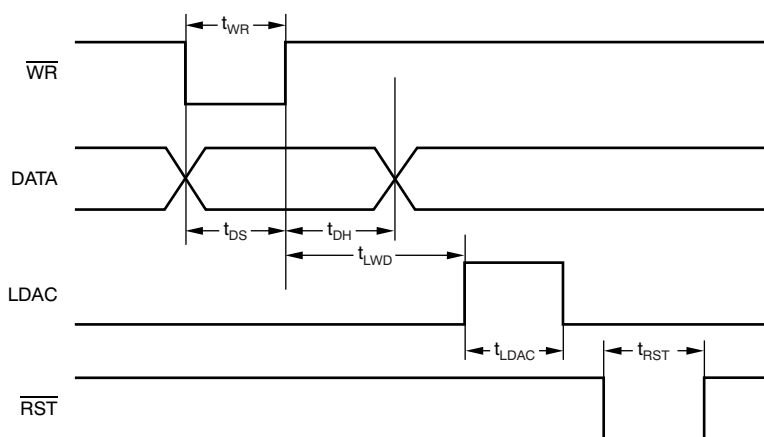


Figure 40. DAC8806 Timing Diagram

Table 1. Function of Control Inputs

CONTROL INPUTS			REGISTER OPERATION
RST	WR	LDAC	
0	X	X	Asynchronous operation. The DAC register is set to zero code, resulting in the DAC output being set to 0 V. The DAC input register contents are not reset by the RST signal.
1	0	0	Load the input register with all 14 data bits.
1	1	1	Load the DAC register with the contents of the input register.
1	0	1	The input and DAC register are transparent.
1			LDAC and WR are tied together and programmed as a pulse. The 14 data bits are loaded into the input register on the falling edge of the pulse and then loaded into the DAC register on the rising edge of the pulse.
1	1	0	No register operation.

## APPLICATION INFORMATION

### Multiplying Mode THD versus Frequency

Figure 35 and Figure 36 show the DAC8806 bipolar 4-quadrant multiplying mode total harmonic distortion (THD) versus frequency. Figure 35 shows the bipolar mode THD with the DAC8806 set to a full-scale code of 3FFFh. Figure 36 shows the bipolar multiplying mode THD with the DAC8806 set to a minus full-scale code of 0000h. In both graphs, two OPA627s are used for both the DAC output op amp and the reference inverting amplifier. A 6 V<sub>RMS</sub> sine wave is used for the reference input V<sub>REF</sub> and is swept in frequency from 10 Hz to 30 kHz. The THD levels versus frequency are illustrated at various DAC output filtering levels using an external ac-coupled low-pass filter.

Figure 37 illustrates the DAC8806 unipolar 2-quadrant multiplying mode THD versus frequency. The DAC8806 is set to a full-scale code of 3FFFh. A single OPA627 is used for the DAC output op amp.

### Stability Circuit

For a current-to-voltage (I/V) design, as shown in Figure 41, the DAC8806 current output (I<sub>OUT</sub>) and the connection with the inverting node of the op amp should be as short as possible and laid out according to correct printed circuit board (PCB) layout design. For each code change there is a step function. If the gain bandwidth product (GBP) of the op amp is limited and parasitic capacitance is excessive at the inverting node, then gain peaking is possible. Therefore, a compensation capacitor C1 (4 pF to 20 pF, typ) can be added to the design for circuit stability, as shown in Figure 41.

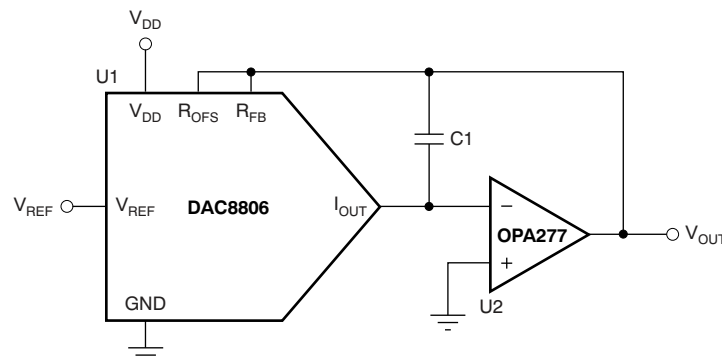


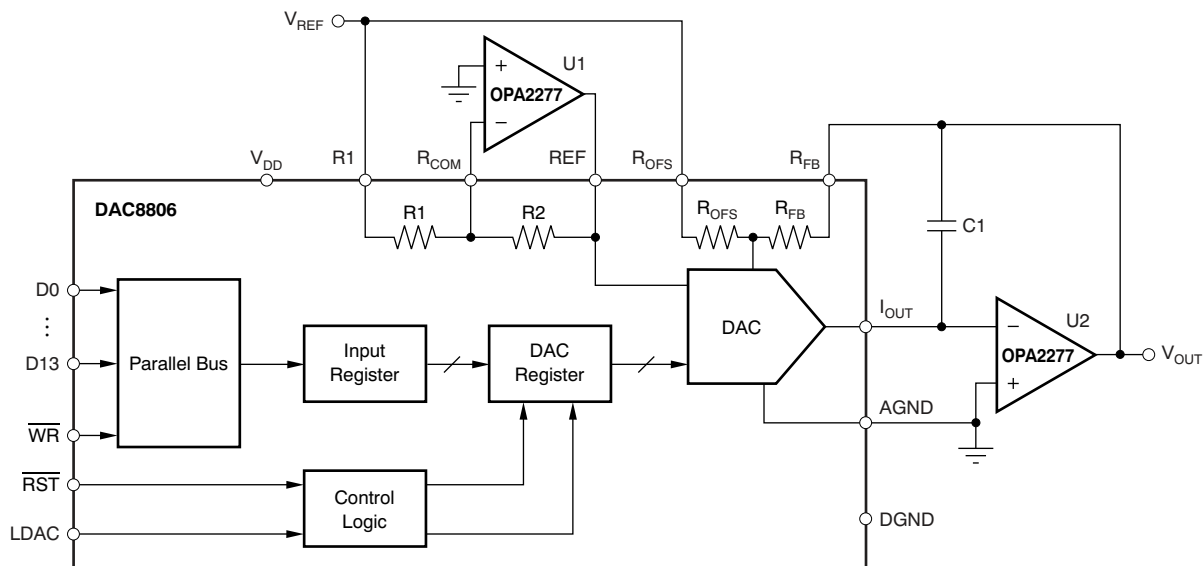
Figure 41. Gain Peaking Prevention Circuit with Compensation Capacitor

### Bipolar Output Circuit

The DAC8806, as a 4-quadrant multiplying DAC, can be used to generate a bipolar output. The polarity of the full-scale output (I<sub>OUT</sub>) is the inverse of the input reference voltage at V<sub>REF</sub>.

Using a dual op amp, such as the OPA2277, full 4-quadrant operation can be achieved with minimal components. Figure 42 demonstrates a ±10 V<sub>OUT</sub> circuit with a fixed +10 V reference.

$$V_{OUT} = \left( \frac{D}{8192} - 1 \right) \times V_{REF} \quad (2)$$



**Figure 42. Bipolar Output Circuit**

### Programmable Current Source Circuit

A DAC8806 can be integrated into the circuit in [Figure 43](#) to implement an improved Howland current pump for precise V/I conversions. Bidirectional current flow and high-voltage compliance are two features of the circuit. With a matched resistor network, the load current of the circuit is shown by [Equation 3](#):

$$I_L = \frac{(R_2 + R_3)/R_1}{R_3} \times V_{REF} \times D \quad (3)$$

The value of  $R_3$  in the previous equation can be reduced to increase the output current drive of  $U_3$ .  $U_3$  can drive  $\pm 20$  mA in both directions with voltage compliance limited up to 15 V by the  $U_3$  voltage supply. Elimination of the circuit compensation capacitor ( $C_1$ ) in the circuit is not suggested as a result of the change in the output impedance ( $Z_O$ ), according to [Equation 4](#):

$$Z_O = \frac{R_1' R_3 (R_1 + R_2)}{R_1 (R_2' + R_3') - R_1' (R_2 + R_3)} \quad (4)$$

As shown in [Equation 4](#),  $Z_O$  with matched resistors is infinite and the circuit is optimum for use as a current source. However, if unmatched resistors are used,  $Z_O$  is positive or negative with negative output impedance being a potential cause of oscillation. Therefore, by incorporating  $C_1$  into the circuit, possible oscillation problems are eliminated. The value of  $C_1$  can be determined for critical applications; for most applications, however, a value of several pF is suggested.

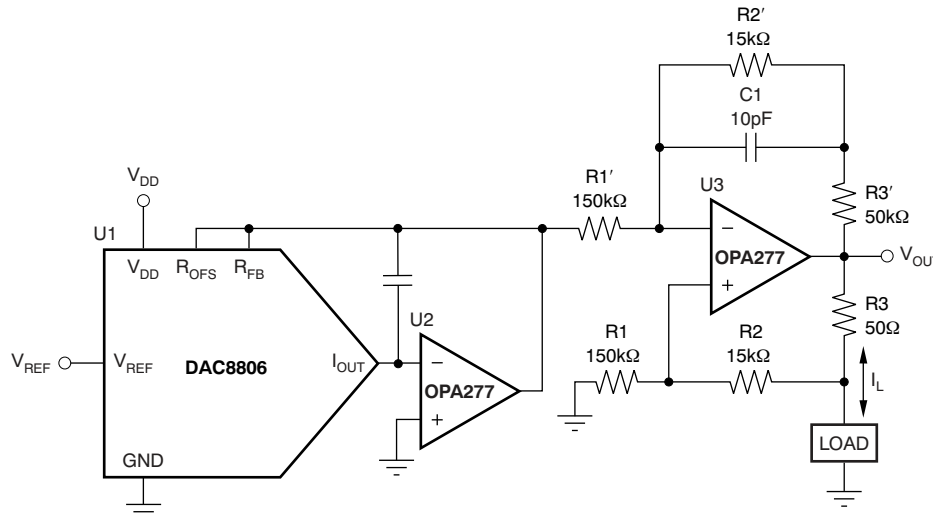


Figure 43. Programmable Bidirectional Current Source Circuit

**Cross-Reference**

The DAC8806 has an industry-standard pinout. [Table 2](#) provides the cross-reference information.

**Table 2. Cross-Reference**

PRODUCT	BIT	INL (LSB)	DNL (LSB)	SPECIFIED TEMPERATURE RANGE	PACKAGE DESCRIPTION	PACKAGE OPTION	CROSS-REFERENCE PART
DAC8806IDB	14	±1	±1	–40°C to +85°C	SSOP-28	SSOP-28	LTC1591AIG



## Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (June 2006) to Revision B	Page
• Changed front page block diagram.....	1
• Fixed typo on 2nd <i>Interface Timing</i> subheader; changed from 5.0V to 2.7V .....	3
• Changed pin 28 description text in <i>Terminal Functions</i> table.....	4
• Changed first row description text in <a href="#">Table 1</a> .....	13
• Changed <a href="#">Figure 42</a> .....	15

Changes from Original (April 2006) to Revision A	Page
• Changed from "voltage-to-current" to "current-to-voltage".....	1
• Changed from (V/I) to (I/V) .....	14

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DAC8806IDB	ACTIVE	SSOP	DB	28	50	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	DAC8806	<a href="#">Samples</a>
DAC8806IDBR	ACTIVE	SSOP	DB	28	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	DAC8806	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

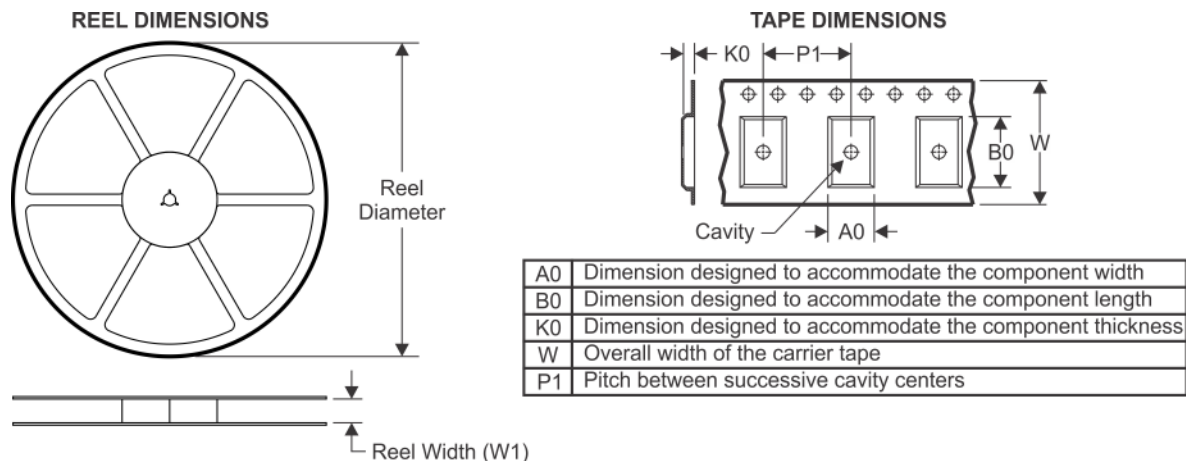
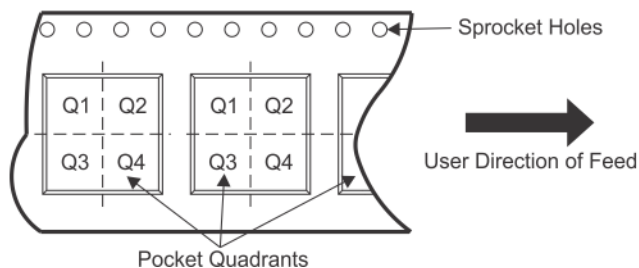
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DAC8806IDBR	SSOP	DB	28	2000	330.0	16.4	8.1	10.4	2.5	12.0	16.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DAC8806IDBR	SSOP	DB	28	2000	350.0	350.0	43.0

**TUBE**


\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
DAC8806IDB	DB	SSOP	28	50	530	10.5	4000	4.1

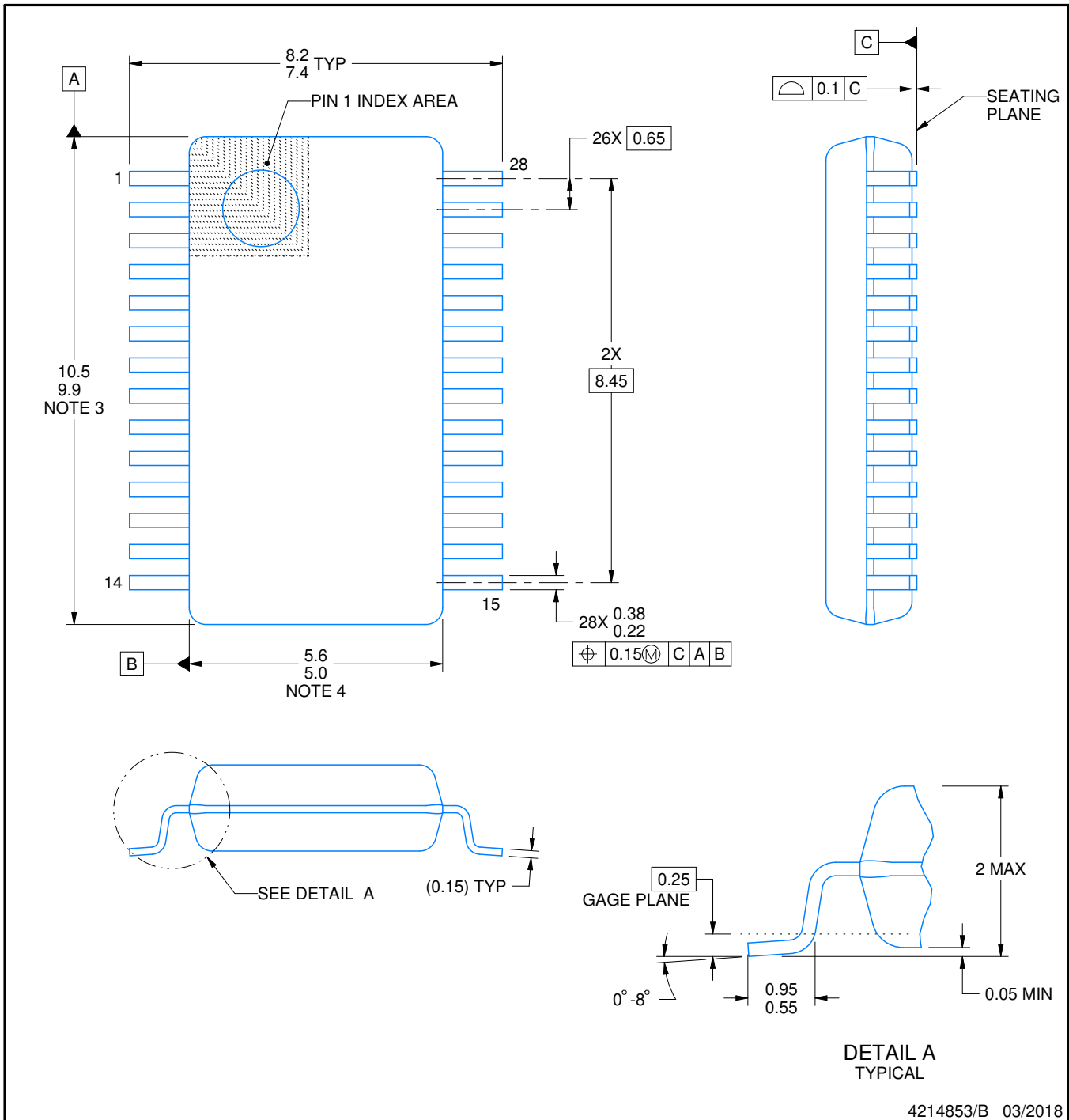
# DB0028A



# PACKAGE OUTLINE

## SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



4214853/B 03/2018

### NOTES:

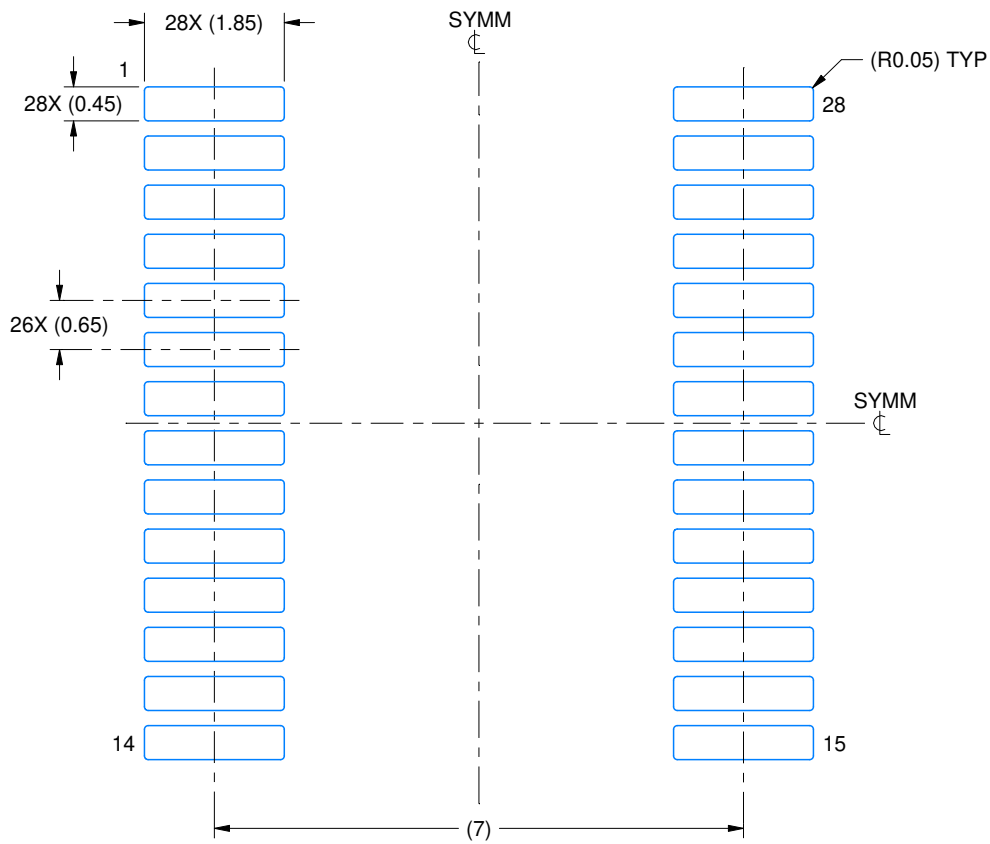
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-150.

# EXAMPLE BOARD LAYOUT

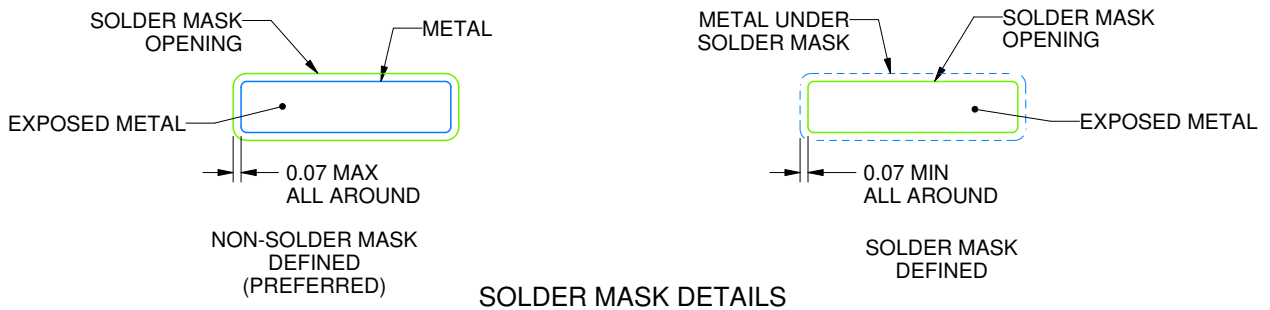
DB0028A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



4214853/B 03/2018

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

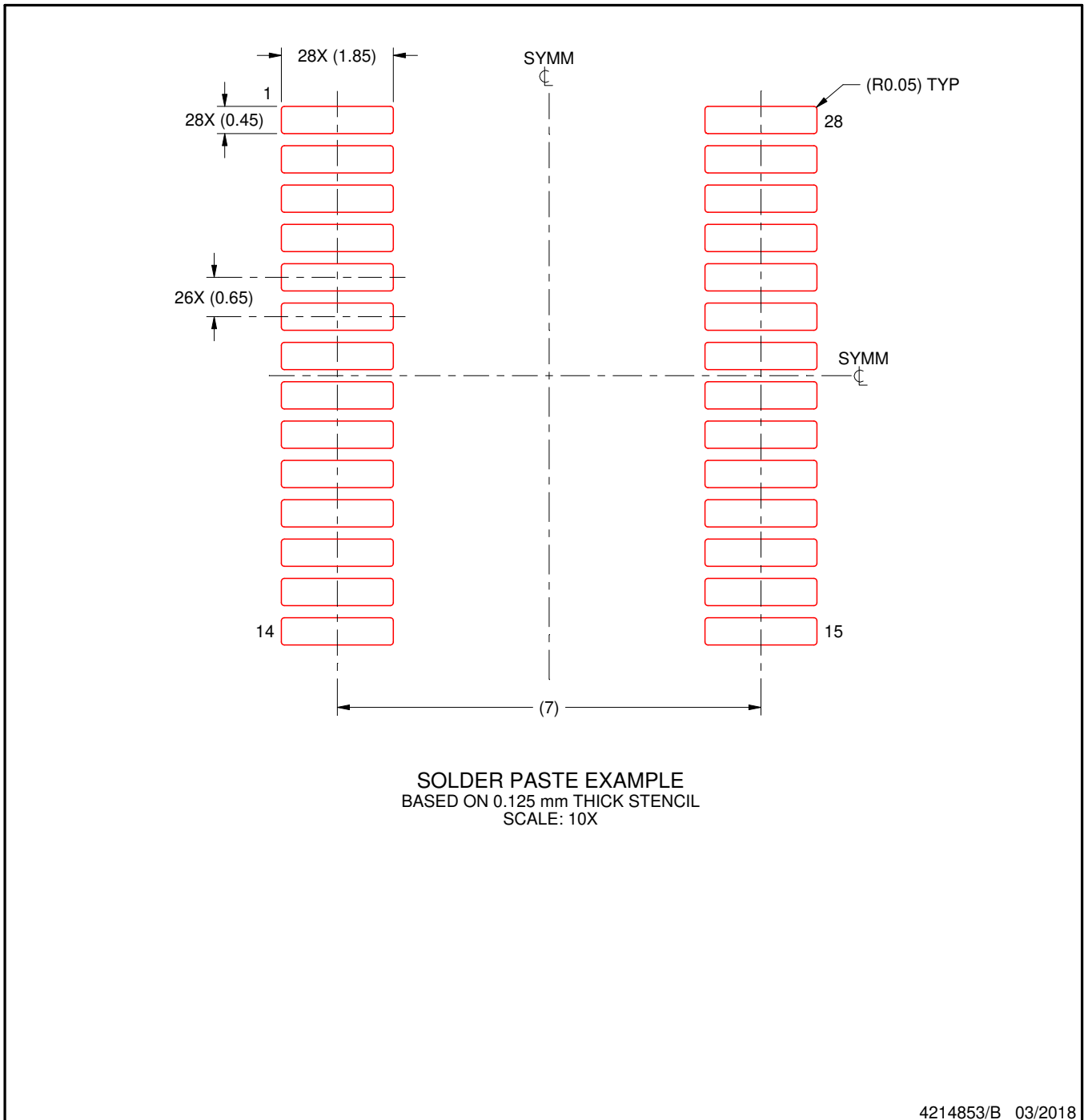


# EXAMPLE STENCIL DESIGN

DB0028A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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